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The Influence of Thyristor Controlled Phase Shifting Transformer on Balance Fault Analysis

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ABSTRACT: *This paper analyses the method to limit fault currents and pre fault bus voltage by the use of Thyristor Controlled phase Shifting transformer (TCPST). The mathematical model of power system equipped with TCPST was systematically derived. The magnitude of the series reactance plays a very important role to limit the short circuit current, as well as TCPST inject a series voltage which reduces the pre fault bus voltage. The total fault current of the system get reduced with respect to the total fault current of the system without introducing TCPST. The effectiveness of TCPST in the proposed method is investigated in the phase fault.*

Keywords: *Balance Fault, FACTS, TCPST*

I. INTRODUCTION

Flexible AC transmission systems (FACTS) devices are being increasingly used in a modern power system to improve both steady state and dynamic performances of the system. There are many types of FACTS devices, such as Unified Power Flow Controller (UPFC), Static Synchronous Compensator (STATCOM), Static Synchronous Series Compensator (SSSC), Thyristor Controlled Phase Shifter (TCPS), Static Var Compensator (SVC), etc. TCPST consists of a shunt transformer, a series transformer and a converter. The converter can be of ac-ac bridge type, pulse-width modulation (PWM) type, ac controller type, etc. The possibility of controlling electric power flow in a transmission system by using controllable solid state devices like TCSC and TCPST is well known. These series connected FACTS devices inject a series voltage with the line and thereby modulate the line reactance or the phase shift between the two end voltages. Recent advances in solid-state power electronics technology have made it possible to implement the above devices using power switching voltage source converters.

On the other hand, short-circuit current levels increase with the addition of new lines, generators and transformers. This may surpass the short circuit current ratings of equipment, like for example circuit breakers, a frequent problem in power systems.

In today's security assessment tools the calculation of the fault level is a well established function. A fault level that exceeds the upper limit endangers the ability of circuit breakers to interrupt the short circuit current. If the fault level is beneath the lower limit, the connection of a major load results in unacceptable voltage drop.

The fault current limitation offered by modern controllers, characterized by their fast responses, may become an important assistance in the task to diminish such large currents. Since the fault clearing time is not instantaneous, depending on the operating time imposed by protection and breaker operation delays, adequate control actions can be performed by this equipment

Although significant flexible features may be introduced in power control by those new devices, they still can be very expensive, and additional benefits like protection improvement should be investigated in order to verify the possibility of their application in the development of more secure and reliable networks

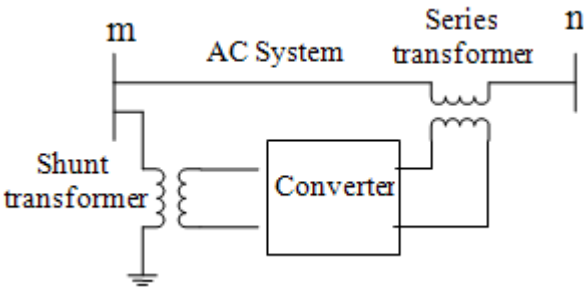
In this paper TCPST is analysis and proper modeling in a power system is discussed.

The fault limitation approach presented here explores this new technology and additional functionality offered by the series-connected FACTS controllers.

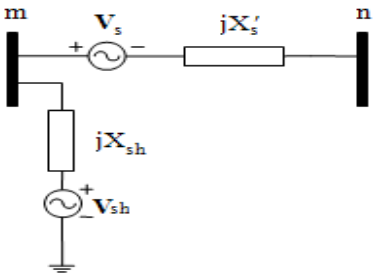
II. MODELING OF TCPST

Mathematical model: Figure 1a shows the schematic diagram of the Thyristor Controlled Phase Shifter (TCPS). The series transformer injects the voltage in series in the system. The active and reactive power injected by the series transformer is taken from the shunt transformer. For sake simplicity of analysis, the insignificant losses from transformer and converter is neglected. Thus the net complex power (real and reactive power) exchange between the TCPS and the system is zero. The injection of this complex power depends on the injection of a series voltage controlled by a converter.

Figure 1b shows the equivalent circuit of Fig. 1a. Vs and Vsh are represented by the synchronous voltage sources in series and shunt, respectively. X_{sh} is the leakage reactance of the shunt transformer. X_s' is the leakage reactance seen from primary side of series transformer is given by $X_s' = X_s + n^2 X_{sh}$ where n is the turn ratio number of the shunt transformer and Xs is the leakage reactance of the series transformer [2]



(a)



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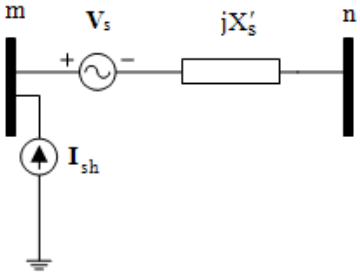

(c)

Figure 1: TCPST; (a) Schematic diagram of a TCPST; (b) a series and shunt synchronous voltage source equivalent; (c) a series injected voltage source and a shunt injected current source

The TCPST consists of two transformers; a shunt transformer or magnetizing transformer connected in parallel and a series transformer or booster transformer in series to the line (Fig.1***).*** The current through the magnetizing transformer induces a voltage on the primary side of the booster transformer. The turn ratio of the shunt transformer is 1: n, and the turn ratio of the series transformer is 1:1. Compared to conventional phase shifting transformers, the mechanical tap changer is replaced by a thyristor controlled equivalent. The purpose of the TCPST is to control the power flow by shifting the transmission angle. In general, phase shifting is obtained by adding a perpendicular voltage vector in series with a phase. This vector is derived from the other two phases via shunt connected transformers. The perpendicular series voltage is made variable with a variety of power electronics topologies. A circuit concept that can handle voltage reversal can provide phase shift in either direction. This Controller is also referred to as Thyristor-Controlled Phase Angle Regulator (TCPAR). A phase shifter model can be represented by an equivalent circuit, which is shown in Fig 2. It consists of admittance in series with an ideal transformer having a complex turns ratio. [4]

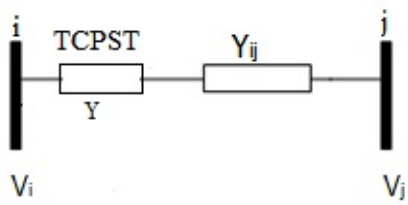

Figure 2: Admittance diagram of a system containing TCPST

The mathematical model of TCPST can be derived from Fig. 2.

$$\begin{bmatrix} Ii \\ Ij \end{bmatrix} = \begin{bmatrix} Yij + Y & -Yij \\ -Yij & Yij + Y \end{bmatrix} \begin{bmatrix} Vi \\ Vj \end{bmatrix}$$

Where Y_{ij} is the admittance of the line and Y is the admittance of the TCPST. The admittance of the TCPST is equal to the reciprocal of the reactance of the TCPST.

So, $Y=1/ (X_s^{/})$. Where $X_s^{/}= X_s + n^2 X_{sh}$. the turn ratio n is actually a complex quantity. Turn ratio equal to $n\angle\varphi$.

III. FAULT VOLTAGE AND FAULT CURRENT LIMITATION

The fault current limitation is based on impedance control. Three phase faults can be controlled with limiting reactor. However, quiet small information exists on fault limitation with series voltage injection, in view of their recent introduction on networks. [1]

Since the series voltages are introduced through series coupling transformers or booster transformer, their respective leakage reactance contribute for fault current limitation, and this aspect must be considered in the analysis.

A. Fault Voltage Limitation

The most important factor that we are analyzing is the possibility of series voltage insertion, which can also be understood as an emulated reactance or capacitance inserted into the line. If a capacitive mode of compensation is in operation with voltage leading current, line fault current would be increased, and in the inductive mode of operation with voltage lagging current, the fault current could be substantially limited. The fast control action of series voltage with the introduction of power-electronics, could be significant in current limitation.

The insertion of series voltage is means of we want to reduce the voltage of the fault point. Which is in fact in agreement with the thevenin pre-fault bus voltage.

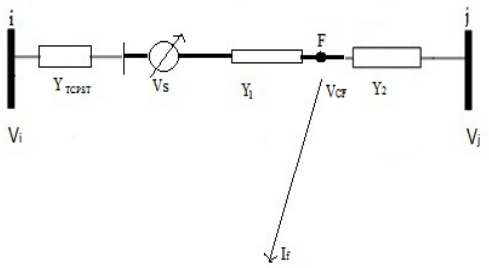

Figure 3: Fault occurring at the system containing TCPST

Now consider resistance of the line tends to zero, so $Y_{TCPST} = 1 / [X_{TCPST}]$ and $Y_1= 1/ Z_1$.

Let's consider $X_0= X_{TCPST} + X_1$
So, $Y_0= 1 / (R+jX_0) = 1 / [(1/Y1)+(1/Y_{TCPST})]$
In the simple configuration of Fig 3, let's suppose the short circuit occurring at the point F. In the configuration it is

seen that TCPST is connected in the system. At the left of the fault the injecting source is Vs is opposition to the left equivalent source, having no effect in the line contribution.

So let's consider the fault point in Fig 3 and the admittance Y_{TCPST} added to the equivalent system admittance. The admittance to the left hand side of the fault point is considered Y_1, and admittance right hand side of the fault point F is considered as Y_2.

The voltage at the point F due to Vi and Vj without the presence of Vs is called uncompensated fault voltage V_F. the series voltage contribution is calculated applying the superposition theorem with the following network.

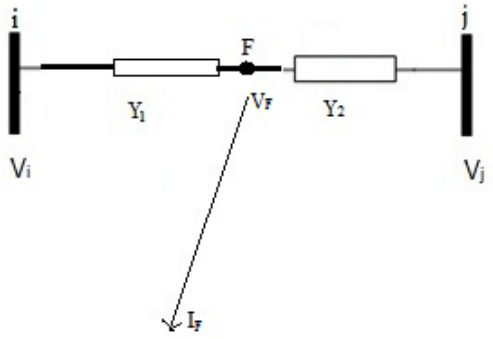

Figure 4: Uncompensated line with fault at point F.

Now applying the superposition theorem:

Consider the voltage V_{F1} at fault point when only source Vi is present, and V_{F2} when only source Vj is present.

$$V_{F1} = \frac{\frac{1}{Y_2}}{\frac{1}{Y_1} + \frac{1}{Y_2}} V_i \qquad \text{(When only Vi is present.)}$$

$$V_{F2} = \frac{\frac{1}{Y_1}}{\frac{1}{Y_1} + \frac{1}{Y_2}} V_j \qquad \text{(When only Vj is present)}$$

So uncompensated fault voltage at point F

$$V_F = V_{F1} + V_{F2}$$

$$V_F = \frac{\frac{1}{Y_2}}{\frac{1}{Y_1} + \frac{1}{Y_2}} V_i + \frac{\frac{1}{Y_1}}{\frac{1}{Y_1} + \frac{1}{Y_2}} V_j$$

$$V_F = \frac{V_i Y_1 + V_j Y_2}{Y_1 + Y_2}$$

Now to calculate the compensated line fault voltage we have to apply superposition theorem, so consider a network where only series connected voltage source is present.

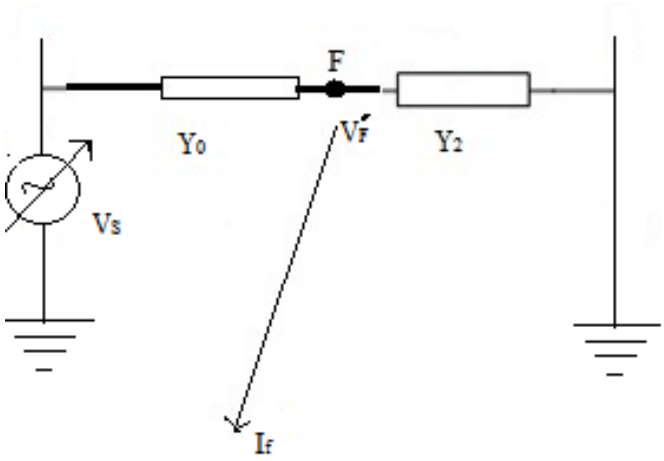

Figure 5: series voltage contribution to the fault voltage

Now the compensated fault voltage $V_F/$.

$$V_{F1}' = \frac{\frac{1}{Y_2}}{\frac{1}{Y_0} + \frac{1}{Y_2}} V_s$$

$$= \frac{Y_0}{Y_0 + Y_2} V_s$$

Now compensated fault voltage V_{CF}

$$V_{CF} = V_F + V_F'$$

$$= \frac{V_i Y_1 + V_j Y_2}{Y_1 + Y_2} + \frac{Y_0}{Y_0 + Y_2} V_s$$

To minimize the fault voltage ,the compensation term $V_F/$ has to be in opposition to V_F, with the series voltage inserted at its maximum magnitude during the fault period.

B Fault Current Limitation

The calculation of the three phase fault is well established in today's security assessment. For solving this problem the admittance matrix Y, used for power flow calculation, must be expanded to $Y^{/}$ by the transient reactance of generators

The impedance matrix Z= inv(Y)

Short Circuit current $I_f = V_{CF} * Y$

Now uncompensated fault current I_f

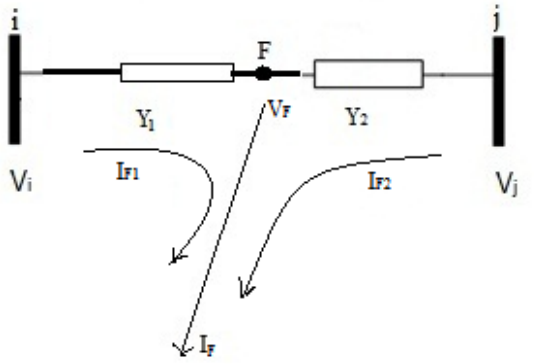

Figure 6: fault current through a network without TCPST

$I_F = I_{F1} + I_{F2}$

$= V_F Y_1 + V_F Y_2$

$= V_F (Y_1 + Y_2)$

After connecting TCPST in the network fault current I_{CF}

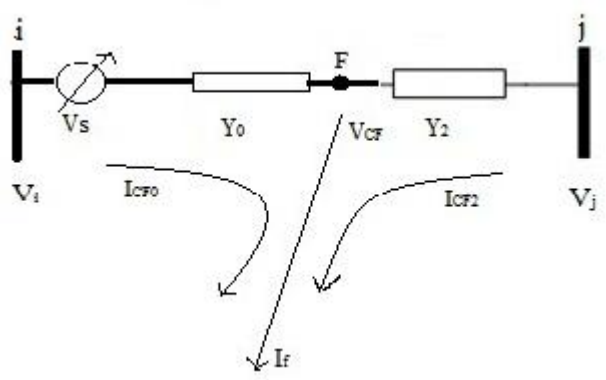

Figure 7: fault current through TCPST connected network.

Now, $I_{CF} = I_{CF0} + I_{CF2}$

$= V_{CF} . Y_0 + V_{CF} . Y_2$

Where $Y_0 = 1/X_0 = 1/[(1/Y_1)+(1/Y_{TCPST})]$

$= 1/[X_{TCPST} + X_1]$

X_{TCPST} is the reactance of TCPST. So after connecting the TCPST reactance will be increased, so Y_0 will be less. So I_{CFO} will be less. V_{CF} will less due to series voltage injection, so I_{CF2} will be less. Therefore the fault current I_{CF} will be limited

IV. PROBLEM FORMULATION AND SIMULATION RESULT

The above proposed method is tested in a power system network is shown in the diagram. The system tested in MATLAB platform. The power system network model is a 10 bus system. In the taken system TCPST is connected between bus no 7 and 9. The fault occurs in the line between bus no 7 and bus no 9. For simplification in calculation the fault point is considered as a bus and the no of the bus is 8. So TCPST is connected now in between bus no 7 and fault point or bus no 8.
. The transient reactance of the generators on a 100 MVA base are given below.

Table 2: Transient reactance of generators

Generator transient reactance in p.u		
Generator no.	R_a	$X_d^{/}$
1	0	0.20
10	0	0.15
11	0	0.25

The line data containing the series resistance and reactance is in per unit, and one half of the total capacitance is in per unit susceptance on a 100 MVA base.

Table 1: Line data of the system are given below

Line Data				
Bus no	Bus no	R (p.u)	X (p.u)	½ B (p.u)
1	2	0.00	0.06	0.0000
2	3	0.08	0.30	0.0004
2	5	0.04	0.15	0.0002
2	6	0.12	0.45	0.0005
3	4	0.10	0.40	0.0005
3	6	0.04	0.40	0.0005
4	6	0.15	0.60	0.0008
4	9	0.18	0.70	0.0009
4	10	0.00	0.08	0.0000
5	7	0.05	0.43	0.0003
7	8	0.06	0.35	0.0004
7	11	0.00	0.10	0.0000
8	9	0.052	0.48	0.0000

The system diagram given below

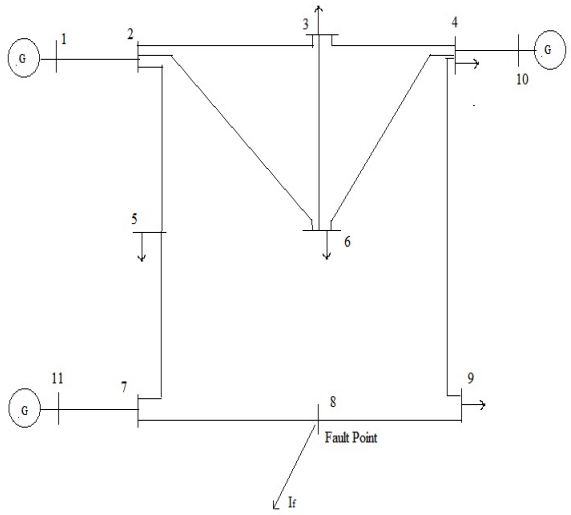

Figure 8: Single line diagram of tested system

The TCPST is connected is in 40% compensation.

Now the system is simulated in MATLAB platform. The system is tested with and without having TCPST in the system.

Without having TCPST it is seen that the pre-fault bus voltage at the fault point or bus no 8 is 1 p.u. it is seen that after connecting TCPST the pre fault voltage of the fault point is 0.81 p.u. So it is cleared that after connecting TCPST the pre fault voltage decreased by 19%.

The limitation has strong dependence on the maximum dependence on the maximum series voltage developed by the converter and the following cases the maximum value adopted is 0.4.

From the simulation result we see that line without having TCPST the total fault current is 2.3622 p.u. and the compensating total fault current is decreased to 2.0515. so fault current decreased by 0.31 p.u. As the pre-fault voltage and post fault current is limited by series compensated line having TCPST, so it is clearly observed that series compensated line having TCPST can decrease the fault level.

Figure captions appear below the figure, are flush left, and are in lower case letters. When referring to a figure in the body of the text, the abbreviation "Fig." is used. Figures should be numbered in the order they appear in the text.

Table captions appear centered above the table in upper and lower case letters. When referring to a table in the text, no abbreviation is used and "Table" is capitalized.

V. CONCLUSION

The influence of TCPST in three phase fault voltage and fault current limitation is discussed in this paper. Here TCPST insert a series connected voltage source in the line which actually opposing the bus voltage. So the pre-fault voltage of the fault point is reduced with the presence of TCPST. We have also seen that TCPST also limit the fault current. So fault level will decrease due to decrease of pre-fault voltage and post fault current. Due to reduction in fault level the dynamic nature as well as transient stability of the system will increase. As the fault current in the system is in limit the thermal equilibrium condition will not hampered.

The future research work will be on optimal location of TCPST in a power system and control of TCPST in both balanced and unbalanced fault analysis.

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