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Closed Loop Control of High Efficiency Voltage Clamped Dc-Dc Converter with Reduced Reverse Recovery Current and Switch

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Abstract: This paper investigates a Closed loop Control of high-efficiency clamped voltage dc–dc converter with reduced reverse-recovery current and switch-voltage stress. In the circuit topology, it is designed by way of the combination of inductor and transformer to increase the corresponding voltage gain. Moreover, one additional inductor provides the reverse-current path of the transformer to enhance the utility rate of magnetic core. In addition, the voltage-clamped technology is used to reduce the switch-voltage stress so that it can select the Schottky diode in the output terminal for alleviating the reverse-recovery current and decreasing the switching and conduction losses. Furthermore, the closed-loop control methodology is utilized in the proposed scheme to overcome the voltage-drift problem of power source under the variation of loads. Thus, the proposed converter topology has a favourable voltage-clamped effect and superior conversion efficiency.

Index Terms: *Converter, Schottky diode, closed loop, reverse recovery, voltage clamped.*

I. Introduction

IN RECENT years, dc–dc converters with steep voltage ratio are usually required in many industrial applications, e.g., the front-end stage for clean energy sources, the dc backup energy system for an uninterruptible power supply (UPS), high intensity discharge (HID) lamps for automobile headlamps, and the telecommunication industry [1]–[3]. The conventional boost converters cannot provide such a high dc-voltage ratio due to the losses associated with the inductor, filter capacitor, main switch, and output diode. Even for an extreme duty cycle, it will result in serious reverse-recovery problems and increase the rating of the output diode. As a result, the conversion efficiency is degraded, and the electromagnetic interference (EMI) problem is severe under this situation to increase the conversion efficiency and voltage gain, many modified boost-converter topologies have been investigated in the past decade [5]–[10]. Although voltage-clamped techniques are manipulated in the converter design to overcome the severe reverse-recovery problem of the output diode in high-level voltage applications, there still exist overlarge switch-voltage stresses, and the voltage gain is limited by the turn-ON time of the auxiliary switch [5], [6] presented a boost soft-single-switch converter, which has only one single active switch. It is able to operate with soft switching in a pulse width modulation (PWM) way without high voltage and current stresses. Unfortunately, the voltage gain is limited below four in order to achieve the function of soft switching. In [8] and [9], coupled inductors were employed to provide a high step-up ratio and to reduce the switch-voltage stress substantially, and the reverse-recovery problem of the output diode was also alleviated efficiently. In this case, the leakage energy of the coupled inductor is another
problem as the main switch was turned OFF. It will result in a high-voltage ripple across the main switch due to the resonant phenomenon induced by the leakage current. In order to protect the switch devices, either a high-voltage-rated device with higher *R*DS(ON) or a snubber circuit is usually adopted to deplete The leakage energy. Consequently, the power-conversion efficiency will be degraded. Zhao and Lee [10] introduced a family of high-efficiency high-step-up dc–dc converters by only adding one addition diode and a small capacitor. However, a snubber circuit is energy losses.

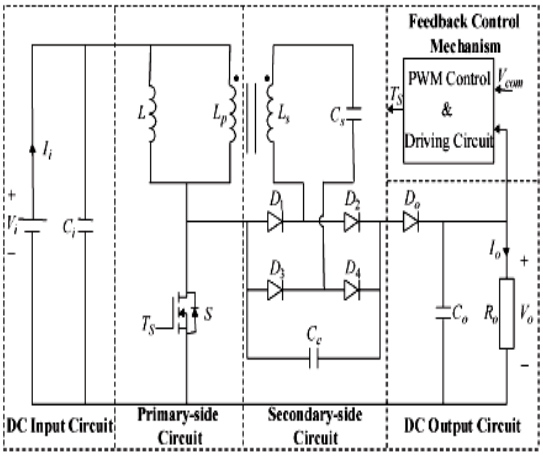

Fig. 1. System configuration of a high-efficiency voltage-clamped dc–dc converter.

II. Converter Design And Analyses

A newly designed converter topology is depicted in Fig. 1, where it contains five parts including a dc-input circuit, a primary-side circuit, a secondary-side circuit, a dc-output circuit, and a feedback-control mechanism. The major symbol representations are summarized as follows. *V*i and *I*i denote the dc-input voltage and current, and *C*i is the input filter capacitor in the dc-input circuit. *L*p represents the primary inductor of the transformer; *L* is the additional inductor in

the primary-side circuit; and *S* is the main switch. *L*s denotes the secondary inductor of the transformer; *C*s and *C*c are the balanced capacitor and clamped capacitor in the secondary-side circuit; and *D*1, *D*2, *D*3, and *D*4 are the rectifier diodes. *V*o and *I*o describe the output voltage and current; *R*o is the output load; *D*o, and *C*o are the output diode and filter capacitor in the output circuit. *V*com and *T*S are the output-voltage command and switch-driving signal in the feedback-control mechanism, respectively.

The equivalent circuit and state definition of the newly designed converter is depicted in Fig. 2, where the transformer is modelled as an ideal transformer with a secondary leakage

Inductor (*L*k). The turns ratio of this ideal transformer is defined as

$$n = \frac{N_2}{N_1} \qquad (1)$$

Where *N*1 and *N*2 are the primary and secondary winding turns. The additional inductor (*L*) is located in parallel with the

primary side of the transformer. Moreover, the rectifier diodes (*D*1, *D*2, *D*3, and *D*4) are connected between the primary and

Secondary sides of the transformer. The voltages across the additional inductor, the main switch, the ideal transformer primary

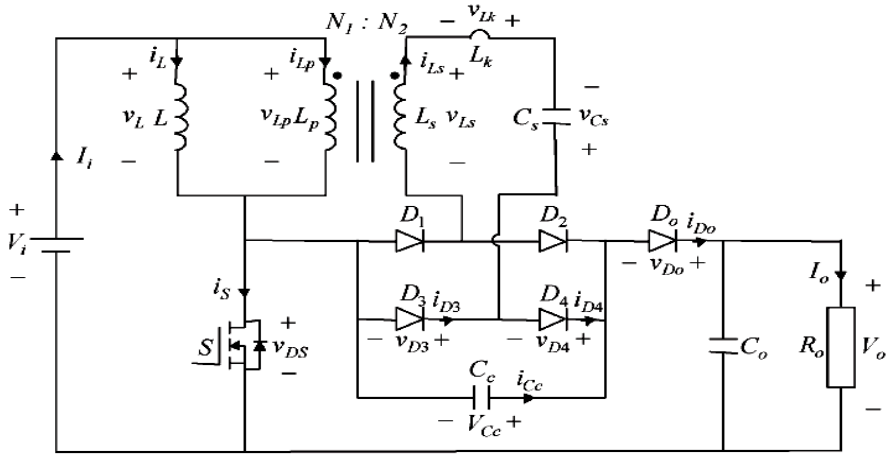

Fig. 2. Equivalent circuit.

and secondary winding, the secondary leakage inductor, the balanced capacitor, and the output diode are *vL*, *v*DS, *vL*p , *vL*s , *vL*k , *vC*s , and *v*Do, respectively. The clamped capacitor *C*c is assumed to be large enough to be viewed as a constant voltage source, *VC*c . The conductive voltage drops of the main switch (*S*) and all diodes (*D*1, *D*2, *D*3, *D*4, and *D*o) are neglected to simplify the circuit analyses. The characteristic waveforms of the proposed high-efficiency converter are depicted in Fig. 3. In addition, Fig. 4 illustrates the operational modes in one switching cycle, and the detailed operation stages are described as follows.

A. Mode 1 (*t*0 − *t*1) *[Fig. 4(a)]*

At time *t* = *t*0, the main switch (*S*) is turned ON. At the same time, the diodes (*D*1 and *D*4) become conducted, and other diodes (*D*2, *D*3, and *D*o) are reverse biased. The additional

inductor (*L*) and clamped capacitor (*C*c) are linearly charged by the input-voltage source (*V*i) through the transformer. Applying

Kirchhoff's law [4], the voltages of *vL*, *vL*p , *vL*s , and *vL*k during this period can be expressed as

$$v_L = v_{L_p} = V_i \qquad (2)$$

$$v_{L_s} = nV_i \qquad (3)$$

$$v_{L_k} = V_{C_c} - nV_i - v_{C_s}. \qquad (4)$$

According to (2)–(4), the rate of change of the additional inductor current (*iL*), the primary-side current (*iL*p), and the N secondary-side current (*iL*s) of the transformer can be representedas

$$\frac{di_L}{dt} = \frac{V_i}{L} \qquad (5)$$

$$\frac{di_{L_p}}{dt} = \frac{V_{C_c} - nV_i - v_{C_s}}{L_k} + \frac{V_i}{L_p} \qquad (6)$$

$$\frac{di_{L_s}}{dt} = \frac{V_{C_c} - nV_i - v_{C_s}}{L_k}. \qquad (7)$$

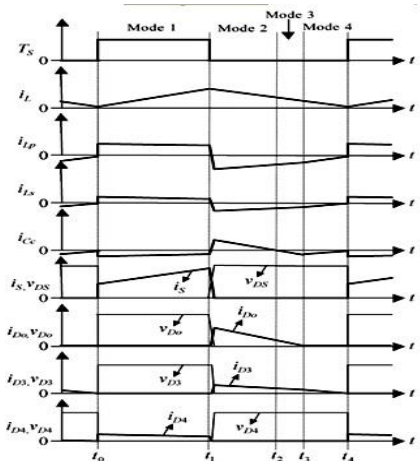

Fig. 3. Characteristic waveforms.

B. Mode 2 (t1 − t2) [Fig. 4(b)]

At time $t = t1$, the main switch (S) is turned OFF. At this time, the diodes ($D2$, $D3$, and Do) become forward biased to start conducting, and other diodes ($D1$ and $D4$) are reverse biased. The stored energy of the additional inductor (L) and

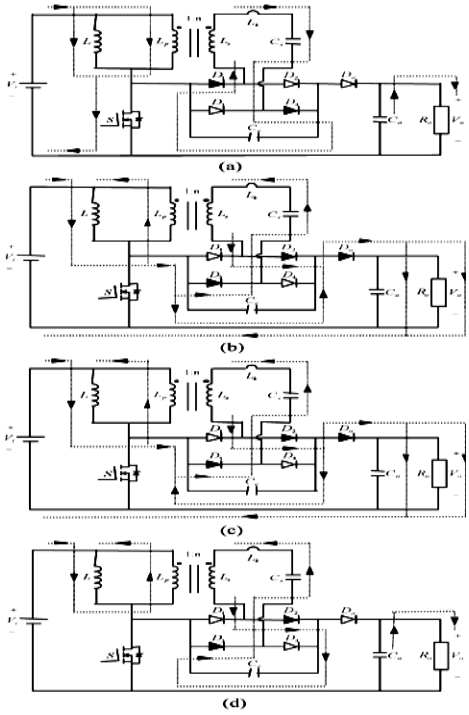

Fig. 4. Operational modes: (a) mode 1 $[t_0 - t_1]$; (b) mode 2 $[t_1 - t_2]$; (c) mode 3 $[t_2 - t_3]$; (d) mode 4 $[t_3 - t_4]$.

clamped capacitor (Cc) in Mode 1 is released to output loads. Moreover, the transformer can be operated at four quadrants to enhance the utility rate of the magnetic core and to keep the clamped voltage (Vcs), since the additional inductor (L) supplies energy to the output terminal by way of the transformer. Applying Kirchhoff's law [4], the voltage and current relations of each element during this mode can be described by

$$v_L = v_{L_p} = V_i + V_{C_c} - V_o \tag{8}$$

$$v_{L_s} = n(V_i + V_{C_c} - V_o) \tag{9}$$

$$v_{L_k} = -V_{C_c} - v_{C_s} - n(V_i + V_{C_c} - V_o) \tag{10}$$

$$v_{DS} = V_i - V_L = V_o - V_{C_c} < V_o \tag{11}$$

$$i_{D_o} = i_L + i_{L_p} = i_{C_c} - i_{L_s} \tag{12}$$

Where iDo is the current of the output diode Do; iCc is the current of the clamped capacitor Cc. According to (11), the cutoff voltage of the main switch (S) is clamped at $Vo - VCc$. Moreover, the main switch (S) with low-voltage-rated capacity can be selected since the switch-voltage stress (vDS) is smaller than the output voltage (Vo). The selection of a low-voltage rated device with lower RDS(ON) is useful for improving the conversion efficiency. Referring to (8)–(10), the rate of change of iL, iLp and iLs is given by

$$\frac{di_L}{dt} = \frac{V_i + V_{C_c} - V_o}{L} \tag{13}$$

$$\frac{di_{L_p}}{dt} = \frac{-V_{C_c} - v_{C_s} - n(V_i + V_{C_c} - V_o)}{L_k} + \frac{V_i + V_{C_c} - V_o}{L_p} \tag{14}$$

$$\frac{di_{L_s}}{dt} = \frac{-V_{C_c} - v_{C_s} - n(V_i + V_{C_c} - V_o)}{L_k}. \tag{15}$$

C. Mode 3 (t2 − t3) [Fig. 4(c)]

At time $t = t2$, the residual energy of the clamped capacitor (Cc) is discharged entirely, i.e., iCc ($t2$) = 0. Immediately, the clamped capacitor (Cc) is charged by the energy of the additional inductor (L) through the transformer, and the rate of change of the clamped-capacitor current (iCc) can be denoted as

$$\frac{di_{C_c}}{dt} = \frac{V_i + V_{C_c} - V_o}{L} + \frac{V_i + V_{C_c} - V_o}{L_p} + 2\left[\frac{-V_{C_c} - v_{C_s} - n(V_i + V_{C_c} - V_o)}{L_k}\right]. \tag{16}$$

Moreover, the stored energy of the additional inductor (L) is released continuously to the output terminal by way of the transformer. The rate of charge of iDo is given by

$$\frac{di_{D_o}}{dt} = \frac{V_i + V_{C_c} - V_o}{L} + \frac{V_i + V_{C_c} - V_o}{L_p} + \frac{-V_{C_c} - v_{C_s} - n(V_i + V_{C_c} - V_o)}{L_k}. \quad (17)$$

D. Mode 4 (t3 − t4) [Fig. 4(d)]

At time $t = t3$, the clamped-capacitor current (iCc) equals to the secondary-side current (iLs) of the transformer, and the output diode current (iDo) decays to 0, i.e., $iDo\ (t3) = 0$. During this period, the voltage of the output diode (vDo) maintains the zero status until the main switch (S) is turned ON. Moreover, the magnitude of the additional inductor current (iL) is equal to the one of the primary-side current (iLp). According to (13) and (14), the rate of change of iLp and iLs can be represented as

$$\frac{di_{L_p}}{dt} = -\frac{di_L}{dt} = -\frac{V_i + V_{C_c} - V_o}{L} \quad (18)$$

$$\frac{di_{L_s}}{dt} = -\frac{V_i + V_{C_c} - V_o}{L} - \frac{V_i + V_{C_c} - V_o}{L_p}. \quad (19)$$

Since the secondary leakage inductor (Lk) and the change rate of iLs in the transformer are very small, the voltage of the secondary leakage inductor (vLk) can be neglected. According to the concept of the zero average voltage across the inductor over one period [4], the voltages of vCs , VCc , and Vo for steadystate operation can be described via (2), (4), (8), and (10) as

$$v_{C_s} = \frac{nV_i(2d-1)}{2(1-d)} \quad (20)$$

$$V_{C_c} = \frac{nV_i}{2(1-d)} \quad (21)$$

$$V_o = \frac{2+n}{2(1-d)}V_i \quad (22)$$

where d is the duty ratio of the main switch (S). Continuously, the main switch (S) is turned ON at time $t = t4$ to begin the next switching cycle.

Since the voltage difference may be caused by the secondary inductor of the transformer, as $d \neq 0.5$, , the major function of the balanced capacitor (Cc) is used for keeping the cutoff voltages of the rectifier diodes ($D1$, $D2$, $D3$, and $D4$) balanced. Moreover, it also can avoid the overlarge current that passed through the rectifier diodes. According to (22), the voltage gain can be tuned by regulating the turns ratio (n) in the transformer to overcome the boost-ratio limitation of the conventional converter. In addition, the switch-voltage stress (vDS) can be calculated via (11), (21), and (22) as

$$v_{DS} = \frac{V_i}{(1-d)}. \quad (23)$$

According to (22) and (23), one can obtain

$$v_{DS} = \frac{2V_o}{(2+n)}. \quad (24)$$

By analyzing (24), the switch-voltage stress (vDS) is not related to the dc-input voltage (Vi) and duty cycle (d) if the values of the output voltage (Vo) and the turns ratio (n) are fixed. Thus, it can ensure that the sustainable voltage of the main switch (S) is constant. As long as the dc-input voltage is not higher than the

rated voltage of the main switch, the high-efficiency voltage clamped dc–dc converter can be applied well to the low-voltage power sources even with large voltage variations, e.g., fuel cell, solar cell, etc.

Fuel-cell generation systems have been receiving more attention in the last years due to the advantages of high-conversion efficiency, low aggression to the environment, no moving parts, and superior reliability and durability. Owing to the electrochemical reaction, fuel cell has the power quality of low voltage and high current. However, the fuel-cell stack with high output voltage is difficult to fabricate and it may be failure when any single cell is inactive. Besides, the output voltage is varied easily with respect to the load variations. In order to satisfy the requirement of high-voltage demand, a stable boost converter with high voltage gain and superior conversion efficiency is necessary to utilize the fuel-cell energy more efficiently. The validity of the proposed converter is verified by the following experimental results via an example of a PEMFC power source.

III. Experimental Results

In experimentation, the high-efficiency voltage-clamped dc–dc converter is designed to operate from the fuel-cell variability dc input, $Vi = 27–37.5$ V, to deliver a constant dc output, $Vo = 200$ V, with the maximal capability of output power, $Po,max = 330$ W. If the maximal value of main switch voltage (vDS) is arranged for clamping at 50 V, the turns ratio can be determined as $n=(2Vo/vDS(max)) − 2 = 6$ according to (24). As can be seen from Figs. 3 and 4, the voltage stress of the output diode (vDo) is the same as the switch-voltage stress. In addition, the voltage stresses of rectifier diodes ($vD1$, $vD2$, $vD3$, and $vD4$) can be calculated via (21) and (23) as $nvDS/2 = 150$ V. For conservative consideration, the main switch (FQI90N08, 80 V), the output diode (Schottky diode SR20100, 100 V), and the rectifier diodes (Schottky diode SR20200, 200 V) are adopted in the experimental converter. In order to solve the problem of the fuel-cell output voltage varied with the variations of loads, the proposed converter with dc-voltage feedback

control is utilized to ensure the system stability, and a PWM control IC TL494 is adopted to achieve this goal of feedback control. The prototype with the following specifications is designed in this section to illustrate the design procedure given in Section II:

switching frequency	fs = 100 kHz;
turns ratio	n = 6;
Additional inductor	L = 5.9 μH;
primary inductor of transformer	Lp = 213.6μH;
secondary inductor of transformer	L=7689.6μH;
secondary leakage inductor	Lk = 0.6 μH;
balanced capacitor	Cs = 4× 6.8μF;
clamped capacitor	Cc = 6× 4.7 μF;
input filter capacitor	Ci = 3300 μF;
output filter capacitor	Co = 3× 4.7 μF;
main switch S:	FQI90N08 (80 V, DS (ON) = 16 mΩ);
Output diode	Do: Schottky diode SR20100 (100 V, 20 A);
Rectifier diodes	D1, D2, D3, D4: Schottky diode SR20200 (200 V, 20 A).

Fig. 5 depicts the results voltage and current curves of the main switch (S) at 310-W output power. As can be seen from this figure, the shaken switch voltage at the beginning is caused by the line inductor when the switch is turned OFF. Fortunately, the steady state of this switch-voltage stress is about 50 V due to the utilization of voltage-clamped technique, and it is much smaller than the output voltage, Vo = 200 V. It has the merit of selecting a low-voltage-rated device in order to reduce the conduction loss of the switch.The simulated current waveforms of the additional inductor (L), in parallel with the transformer, primary inductor of transformer (Lp), and secondary inductor of transformer (Ls) at 310-W output power, are depicted in Fig. 6, the balanced capacitor (Cs) can be used for balancing the current and cutoff voltage of the diodes (D3 and D4) when the condition of $d \neq 0.5$, holds.

For verifying the voltage-clamped property, the experimental voltage responses of the output voltage (Vo), clamped capacitor (Cc), and main switch (S) at 310-W output power are depicted . As can be seen from this figure, the output voltage, Vo = 200 V, is strode mainly across the clamped capacitor in the secondary-side circuit (i.e., VCc = 150 V). Thus, the switch-voltage stress and the cutoff voltageof the output diode are clamped at about 50 V. In order to examine the robust performance of the proposed converter scheme, the experimental results of the converter output voltage (Vo), and the PEMFC output current (Ii) under the step load variation between no load (0 W) and full load (310 W) are depicted . the converter output voltage, Vo = 200 V, is insensitive to the variation of loads due to the closed-loop control, and the output current ripple is also slightly extreme as a result of the high switching frequency.

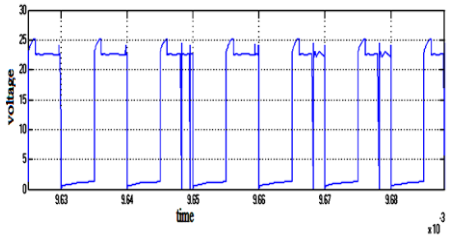

Fig.5.Simulated voltage wave forms of main switch S.

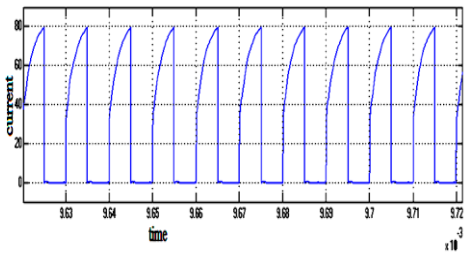

Fig.5.Simulated voltage and current wave forms of main switch S

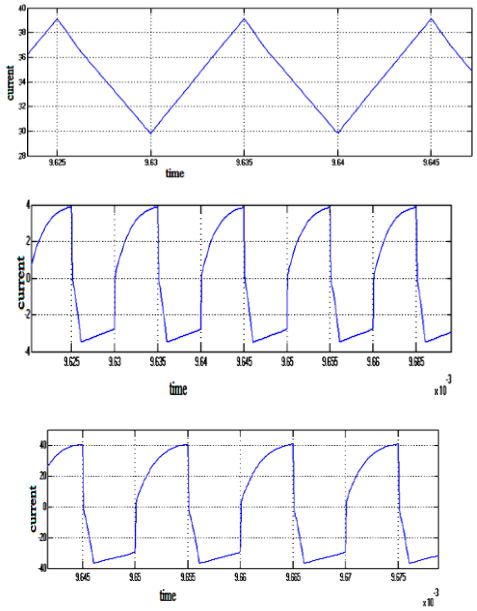

Fig.6. Simulated current response of additional inductor L, transformer primary inductor Lp and transformer secondary inductor Ls.

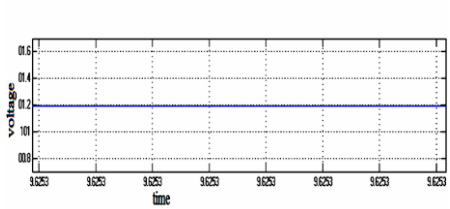

Fig.7.Simulated voltage response of output voltage V0.

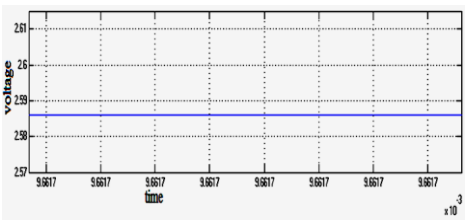

Fig.7. Simulated voltage response of,clamped capacitor Cc.

IV. CONCLUSION

This project has developed a voltage-clamped dc–dc converter with reduced reverse recovery current and switch-voltage stress, with a power quality of low voltage and high current. The newly designed converter circuit has the following improvements compared to the previous work.

1) Proposed converter can select the main switch with lower sustainable voltage for alleviating the switch conduction loss due to the utilization of voltage-clamped technique.
2) All diodes in this circuit topology are Schottky diodes with the reduction of switching and conduction losses.
3) The additional inductor is used for providing the reverse current path of the transformer to raise the utility rate of the magnetic core.
4) Additional snubber circuits for absorbing the voltage spikes in the diodes are not required to further cut down the manufacture cost.
5) There is no circulating current to overcome the problem of degenerate efficiency under slight loads.
6) The voltage-drift problem of power source under the variation of loads can be solved by the closed-loop control methodology.

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