A Novel Approach to Design High Speed Arithmetic Logic Unit Based On Ancient Vedic Multiplication Technique

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***Abstract**: This paper is devoted for designing high speed arithmetic logic unit. All of us know that ALU is a module which can perform arithmetic and logic operations. The reason behind choosing this topic as a research work is that, ALU is the key element of digital processors like as microprocessors, microcontrollers, central processing unit etc. Every digital domain based technology depends upon the operations performed by ALU either partially or whole. That's why it highly required designing high speed ALU, which can enhance the efficiency of those modules which lies upon the operations performed by ALU. The speed of ALU greatly depends upon the speed of multiplier. There are so many multiplication algorithms exist now-a-days at algorithmic and structural level. Our work proved that Vedic multiplication technique is the best algorithm in terms of speed. Further we have seen that the conventional Vedic multiplication hard wares have some limitations. So to overcome those limitations a novel approach has been proposed to design the Vedic multiplier with the use of unique addition tree structure, which is used to add partially generated products. For designing the two bit Vedic multiplier conventional hardware of Vedic multiplier has been used. For designing the four and eight bit level Vedic multiplier divide and conquer approach has been used. After designing the proposed Vedic multiplier, it has been integrated into an eight bit module of arithmetic logic unit along with the conventional adder, subtractor, and basic logic gates. The proposed ALU is able to perform three different arithmetic and eight different logical operations at high speed. All of these operational sub-modules (adder, subtractor, multiplier and logical gates) have been designed as the combinatorial circuit. And for the synchronization of these operational sub-modules, the multiplexers which have been used to integrate these sub-modules in a single unit have been triggered by positive edge clock To design proposed arithmetic logic unit verilog hardware description language (HDL) has been used. For designing operational sub-modules data flow modeling and for integration purpose behavioral modeling style has been used. For this design the target FPGA which we have takes belongs to Virtex-2P (family), XC2VP2 (device), FG256 (package) with speed grade of -7. For synthesis purpose Xilinx synthesis tool (XST) of Xilinx ISE-9.2i has been used. The behavioral simulation purpose ISE simulator has been used.*

The maximum combinational path delay of proposed multiplier is 11.886 ns. And the ALU that has been designed can operate at the maximum frequency of 741.455 MHZ.

***Keywords:** - Vedic Urdhva Triyambakam multiplication algorithm, Arithmetic Unit, Arithmetic Logic Unit, Addition tree structure.*

I. Introduction

As all of us know that the Computation unit is main unit of any technology, which performs different arithmetic operations like as addition, subtraction and multiplication etc. also in some places it performs logical operations also like as and, or, invert, x-or etc. which is dominant feature in the digital domain based applications. ALU is the execution unit which does not only performs Arithmetic operations but also Logical operations. And that's why ALU is called as the heart of Microprocessor, Microcontrollers, and CPUs. No technology can exist, without those operations which are performed by ALU. Every technology uses works upon those operations either fully or partially which are performed by ALU. The block diagram of ALU is given below, where ALU has been implemented on FPGA tool

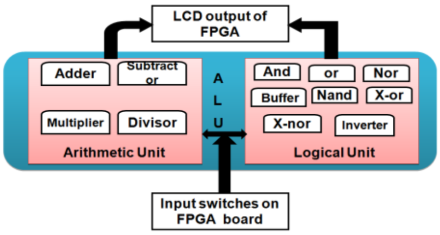


Figure 1.1 Block Diagram of ALU

Here the input interface to access ALU module is input switches on FPGA board, and after processing on the data the result can be seen from LCD output of FPGA. For multiplication purpose vedic Urdhva Triyambakam multiplication scheme has been used. Urdhva Triyakbhyam Sutra is a general multiplication formula applicable to all cases of multiplication. It literally means "Vertically and Crosswise". To illustrate this multiplication scheme, let us consider the multiplication of two decimal numbers (32 × 44). The conventional methods already know to us will require 16 multiplications and 15 additions. An alternative method of multiplication using Urdhva Triyakbhyam Sutra is shown in following figure. The Vedic multiplication algorithm for 2 digit decimal numbers is shown below:-

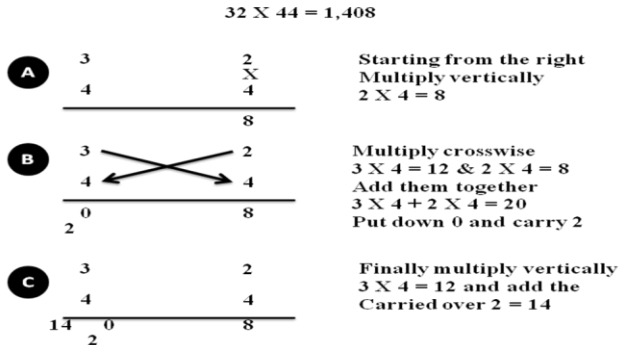


Figure 1.2 Vedic Multiplication Technique

On the basis of this the conventional vedic Multiplier hardware has been designed which is shown below for 4x4 Bit, Using the same approach N-Bit Multiplier can be introduced[10]:-

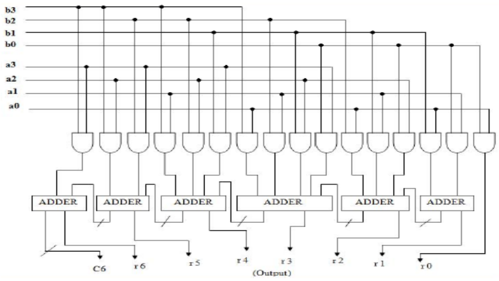


Figure 1.3 Conventional Four Bit Vedic Multiplier

But it has large carry propagation path delay which limits the speed of it. So to overcome this problem many methodologies have been introduced in which the latest and popular technique is to replace the conventional addition structure with carry save addition (CSA) structure. But we have seen that its speed is also limited because of intermediate processes followed by the CSA to convert three operands into two operands addition. Diagram of this is given following for 4-Bit level Multiplication [4]:

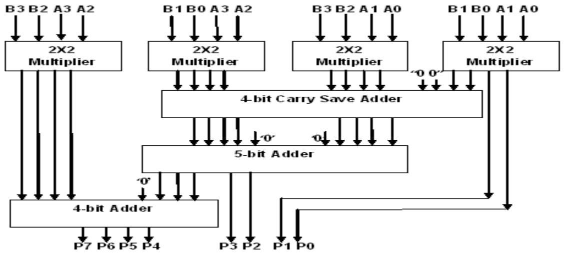


Figure 1.4 Four Bit Vedic Multiplier with CSA

II. Proposed ALU Module

Our Proposed 8x8 bit Arithmetic Unit is shown in the following:-

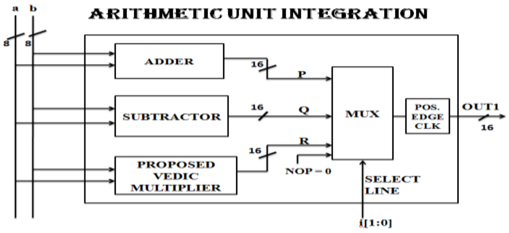
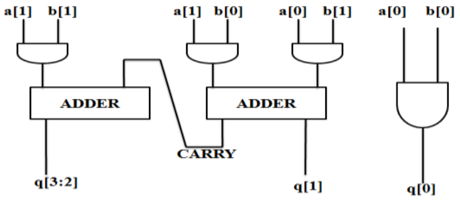


Figure 2.1 Proposed Arithmetic Unit Integration

Here a and b are the two 8 bit inputs of our Arithmetic Unit. And other sections of the design are self-explanatory.

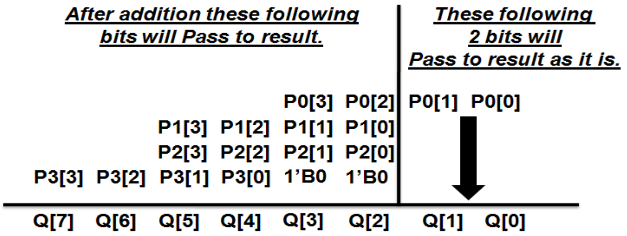
For 2-Bit multiplication Conventional Vedic multiplication Hardware has been used. As at 2 bit level multiplication we have not to worry about the carry propagation path.



Here inputs are a [1:0] and b[1:0], and output is q[3:0].

Figure 2.2 Two Bit Conventional Vedic Multiplier

Diagram for Unique addition tree structure for partial product addition for 4 bit is given in the following:-



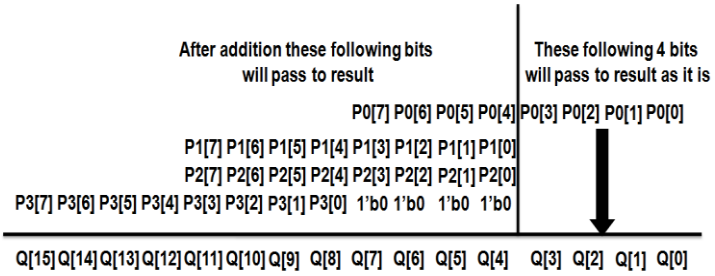
After addition these following bits will Pass to result.

These following 2 bits will Pass to result as it is.

P0[3] P0[2] | P0[1] P0[0]
P1[3] P1[2] P1[1] P1[0]
P2[3] P2[2] P2[1] P2[0]
P3[3] P3[2] P3[1] P3[0] 1'B0 1'B0
Q[7] Q[6] Q[5] Q[4] Q[3] Q[2] Q[1] Q[0]

Figure 2.3 Proposed Addition Tree Structure of 4-Bit Multiplier

Diagram for Unique addition tree structure for partial product addition for 8 bit is given in the following:-



After addition these following bits will pass to result

These following 4 bits will pass to result as it is

P0[7] P0[6] P0[5] P0[4] | P0[3] P0[2] P0[1] P0[0]
P1[7] P1[6] P1[5] P1[4] P1[3] P1[2] P1[1] P1[0]
P2[7] P2[6] P2[5] P2[4] P2[3] P2[2] P2[1] P2[0]
P3[7] P3[6] P3[5] P3[4] P3[3] P3[2] P3[1] P3[0] 1'b0 1'b0 1'b0 1'b0
Q[15] Q[14] Q[13] Q[12] Q[11] Q[10] Q[9] Q[8] Q[7] Q[6] Q[5] Q[4] Q[3] Q[2] Q[1] Q[0]

Figure 2.4 Proposed Addition Tree Structure of 8-Bit Multiplier

Here the assignment of partial products P0, P1, P2, P3 has given from right to left at output of vedic N/2-Bit Vedic multiplier, where N shows the no. of bits in one input of multiplier. And also which addition tree structure we have designed is very simple to understand, design and implement. Here for the addition purpose the unique addition tree structure. The block diagram for 4 bit level multiplication shown below.

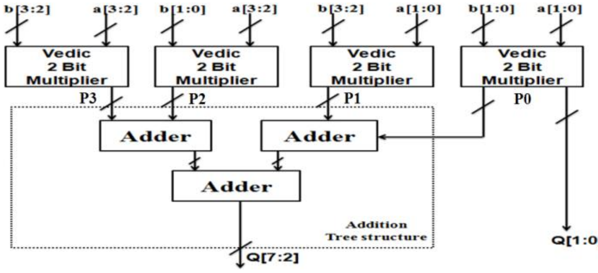


Figure 2.5 Block Diagram of Proposed 4-Bit Vedic Multiplier

Block diagram of 8-Bit Vedic Multiplier is shown below:-

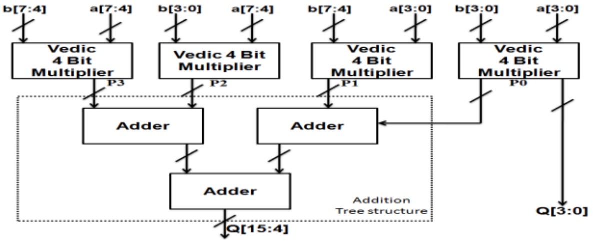


Figure 2.6 Block Diagram of Proposed 8-Bit Vedic Multiplier

After designing the Arithmetic Unit, it has been incorporated into the ALU module. The block diagram of proposed ALU is given following, which is self explanatory in itself:-

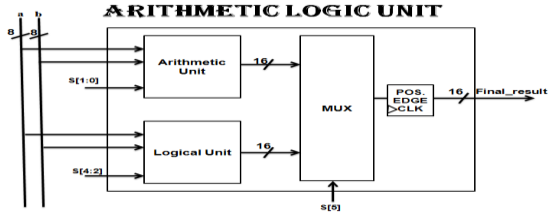


Figure 2.7 Proposed ALU

For designing the Logical unit we have used the simple conventional logic gates and multiplexer has been used for integration purpose. It can be easily built by referring any standard book of digital electronics so it has not been discussed here.Control word for the proposed ALU is:-

CONTROL WORD OF ALU

S [5]	S [4]	S [3]	S [2]	S [1]	S [0]

S[5]	S[4]	S[3]	S[2]	S[1]	S[0]	OPERATIONS PERFORMED
0	x	x	x	0	0	ADDITION (a,b)
0	x	x	x	0	1	SUBTRACTION (a,b)
0	x	x	x	1	0	MULTIPLICATION (a,b)
0	x	x	x	1	1	NOP = 0
1	0	0	0	x	x	AND (a,b)
1	0	0	1	x	x	OR (a,b)
1	0	1	0	x	x	NOR (a,b)
1	0	1	1	x	x	DATA BUFFER (a)
1	1	0	0	x	x	NAND (a,b)
1	1	0	1	x	x	X-OR (a,b)
1	1	1	0	x	x	X-NOR (a,b)
1	1	1	1	x	x	NOT (a)

Figure 2.8 Control Word

III. QUANTITATIVE RESULTS

Following table shows the area and timing constraints of proposed Vedic multiplier at different bit levels.

N Bit multiplier	Number of LUT used as logic	Number of occupied Slices	Total eq. gate count for design	Additional JTAG gate count for design	Maximum combinational path delay (ns)
2-Bit	4	2	24	384	4.626ns
4-Bit	31	16	230	768	8.387ns
8-Bit	139	70	1073	1536	11.886ns

Table 3.1 Device Utilization Summary of N-Bit Multiplier

IV. COMPARATIVE RESULTS

To show the efficiency of proposed Vedic multiplier at eight bit level, it has been compared with some other popular multiplier structures based on different multiplication algorithms at the eight bit level. For the comparison purpose some standard papers have been used. For true and reliable comparison, proposed multiplier has been implemented on the same platform of target FPGA, which has been used by the reference papers. Comparative tables are shown below:-

(a)In the following given table the target FPGA used belongs to Virtex 2P (family), XC2VP2 (device), FG 256 (Package), -7 (speed grade).

Maximum Combination Path Delay for Different Multipliers at Eight Level in Nano Seconds						
Karatsuba [10]	**Vedic Karatsuba [10]**	**Modified Booth Wallace [4]**	**Vedic with Partitioning [4]**	**Conventional Vedic [10]**	**Vedic with CSA [4]**	**Proposed**
31.039	**18.695**	**15.815**	**15.685**	**15.418**	**13.07**	**11.886**

Table 4.1 Comparative Table 1 for Different Multipliers at 8-Bit Level

(b)In the following given table the target FPGA used belongs to Spartan 3 (family), XC3S50 (device), PQ 208 (Package), -4 (speed grade).

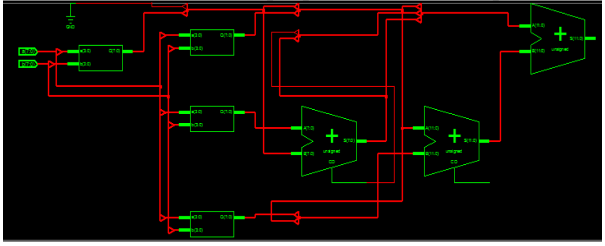
Maximum Combination Path Delay for Different Multipliers at Eight Level in Nano Seconds			
Array [2]	Booth [2]	Conventional Vedic [2]	Proposed
32.01	29.549	21.679	19.467

Table 4.2 Comparative Table 2 for Different Multipliers at 8-Bit Level

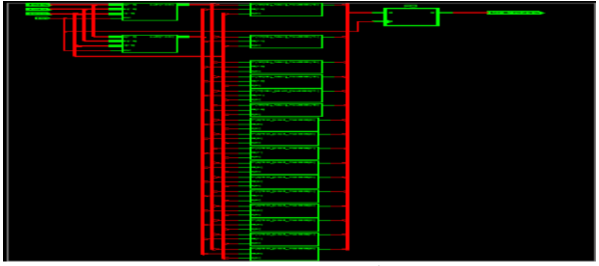
By designing the proposed Vedic multiplier for the same reconfigurable hardware as shown in [4] and [2], make the comparison platform (hardware) independent, algorithmic, technique and approach based comparison. So by comparing with different multipliers at the same platform it can be concluded that the algorithm and approaches which has been proposed to design Vedic multiplier, in this thesis work, is better in comparison to the other popular algorithms and approaches shown in [4] and [2]. In [10] M. Ramalatha et.al. Have not shown that which target FPGA they have used to design their modules so we have compared our proposed multiplier design with our conventional target FPGA, which we have used to make the overall design of ALU. So by this it can be concluded that our proposed algorithm, approach and platform are better than [10].

V. Synthesis And Simulation

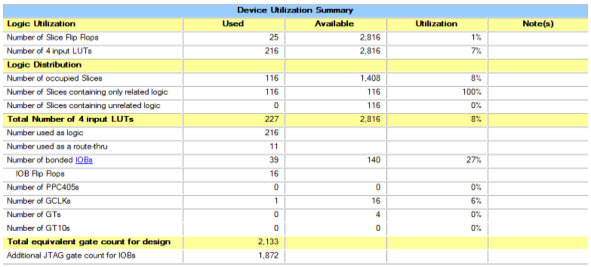
1.RTL schematic of proposed vedic multiplier:-



2.RTL schematic of proposed ALU:-

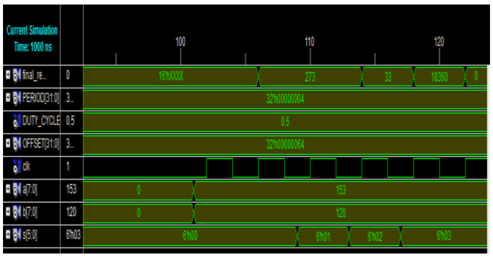


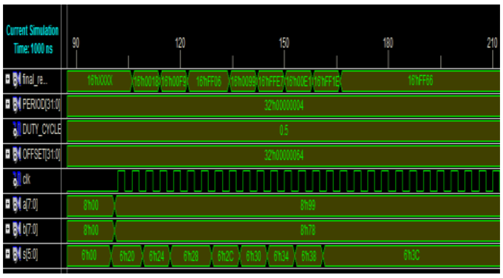
3.Device utilization summary of proposed ALU:-



Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Flip Flops	25	2,816	1%	
Number of 4 input LUTs	216	2,816	7%	
Logic Distribution				
Number of occupied Slices	116	1,408	8%	
Number of Slices containing only related logic	116	116	100%	
Number of Slices containing unrelated logic	0	116	0%	
Total Number of 4 input LUTs	227	2,816	8%	
Number used as logic	216			
Number used as a route-thru	11			
Number of bonded IOBs	39	140	27%	
IOB Flip Flops	16			
Number of PPC405s	0	0	0%	
Number of GCLKs	1	16	6%	
Number of GTs	0	4	0%	
Number of GT10s	0	0	0%	
Total equivalent gate count for design	2,133			
Additional JTAG gate count for IOBs	1,872			

4. Simulation results of proposed ALU as per control word of ALU:-





VI. Conclusion

We have proposed a new technique to design Vedic multiplier using unique addition tree structure, which gives better response in terms of speed in comparison to the conventional vedic multiplier hardware, Vedic multiplier with partitioning, Vedic multiplier with carry save adder, Modified Booth Wallace , Karatsuba, Vedic Karatsuba, Array, Booth, Wallace multiplier. And then this multiplier module has been put in the ALU along with conventional modules.

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