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Sliding Mode Control of DSTATCOM Using Seven Level Multilevel Inverter

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***Abstract*:**In distribution system (DS), the majority of power consumption has been drawn in reactive loads. These loads are drawn in low power factor and therefore give rise to reactive power burden in the distribution system. So that DSTATCOM controller is used to compensate reactive power, correction of power factor and elimination of current harmonics. This paper presence the 7-Level Cascaded H-bridge Inverter as DSTATCOM for compensation of Balanced and Unbalanced Linear and Non-Linear Loads by using Level Shifted and Phase Shifted PWM techniques. The advantage of CHB Inverter is reducing the number of switches and thus switching losses.The simulation verification of the derived results are provided through a three-phase distribution static compensator (DSTATCOM) model. The application in the three-phase system has been shown through simulation studies

Index Terms:Cascaded H-bridge multilevel inverter (CHBMLI), distribution static compensator (DSTATCOM), Multiband hysteresis modulation, switching characterization.

I. INTRODUCTION

The multilevel power conversion has been receiving increasing attention in the past few years for high power application [4]. Numerous topologies have been introduced and studied extensively for utility and drive applications in the recent literature. These converters are suitable in high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltage with a limited maximum device rating [1], [4]. There are various current control methods for two-level converters [5]. Hysteresis control of power converters, based on instantaneous current errors, is widely used for the compensation of the distribution system as it has good dynamic characteristics and robustness againstparameter variations and load non-linearties [6].

A DSTATCOM is a voltage source converter (VSC) based device. When operated in a current control mode, it can improve the quality of power by mitigating poor load power factor, eliminating harmonic content of load.

In this paper, a generalized multiband hysteresis modulation has been proposed for the sliding-mode control of CHBMLI controlled systems. A frequency-domain method is proposed for the switching characterization of the multilevel inverter using Tsypkin's method and the describing function of nonlinear relay [23]. A hierarchical switching scheme is used for the equal-power-rated modular cells of the cascaded multilevel inverter. Sequential swapping of the hierarchy is done for applications involving balancing of the capacitor voltages. The simulation and experimental verification of the derived results have been obtained through a single-phase DSTATCOM model. The application has been shown through simulation results for a three-phase distribution-system compensation using DSTATCOM.

II. SLIDING-MODE CONTROL OF DSTATCOM

In this section, a sliding-mode control for distribution system load voltage control using DSTATCOM is presented briefly [13]. A DSTATCOM-compensated distribution system is shown in Fig. 1.

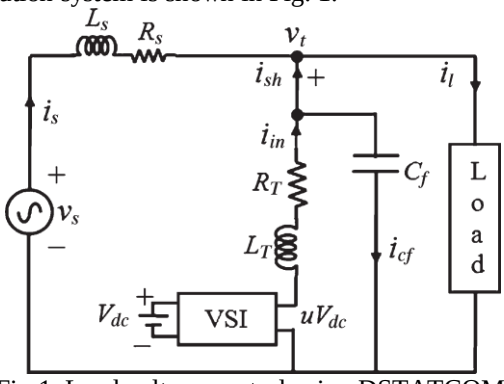

Fig.1. Load voltage control using DSTATCOM.

The distribution system consists of a load that is supplied from voltage source *vs*through a feeder *(Rs, Ls)*, as shown in Fig. 1. DSTATCOM consists of a VSI that is connected to the load through an interfacing inductance *LT*. Resistance *RT* represents the equivalent resistance in the shunt path. Voltage *V*dcrepresents the net dc-link voltage of the VSI. Filter capacitor *Cf*is connected in the shunt. The currents flowing through the different branches are source current *is*, load current *il*, current through the filter capacitor *icf*, inverter output current *i*in, and current injected in the shunt branch *ish*. The net controllable voltage at the output of the VSI is *uV*dc, where *u* is defined as the control input and represents the switching logic of the inverter. It assumes discrete values between −1 and +1, depending upon the number of levels of the VSI, e.g., −1, −1/2, 0, +1/2, and +1, for a five-level inverter.

In order to design a control law independent of the load and source parameters, the following state vector is defined: *zT= [v̇tvt]*.State variable *vt*is the terminal voltage or point of-Common-coupling (PCC) voltage and *v̇t* is its derivative. Considering the terminal voltage as output, the state-space representation of the system shown in Fig. 1 can be written as

$$\dot{z} = Fz + g1u + g2d$$

$vt=hoz$ (1)

Where

$$F=\begin{bmatrix}\frac{-R_T}{L_T} & \frac{-1}{C_f L_T}\\ 1 & 0\end{bmatrix} g_1=\begin{bmatrix}\frac{V_{dc}}{C_f L_T}\\ 0\end{bmatrix} g_2=\begin{bmatrix}1\\0\end{bmatrix}$$

$$h_O=\begin{bmatrix}0 & 1\end{bmatrix}$$

Variable d is considered to be a periodic source that depends upon the shunt current as

$$d=-\frac{1}{C_f}\left(\frac{di_{sh}}{dt}\right)-\left(\frac{R_T}{C_f L_T}\right)i_{sh} \qquad (2)$$

State vector $z(t)$ is required to track reference vector $zr(t)$. This reference state vector comprises the reference for the terminal voltage and its derivative defined as $zTr= [\dot{v}trefvtref]$. It is desired to derive a model following the sliding-mode control for the sinusoidal reference with frequency $\omega 0$, as given by

$vtref(t) = Vtrefsin(\omega_O t-\delta P)$ (3)

where$V$trefis the amplitude of the reference terminal voltage and δpis its phase angle with respect to the reference phase of source voltage vs.

The design of sliding-mode control requires two conditions to be satisfied [11], [24], i.e., reaching and sliding phases. Let us choose a switching surface, which will be called here onward as switching function se that is defined by the following control law:

$se=Kze=k1(\dot{v}tref-\dot{v}t)+k2(vtref-vt)$ (4)

wherezeis the error state vector defined as

$ze= (zr-z) =[\dot{v}tref-\dot{v}t \quad vtref-vt]^T$ (5)

In (4), K is the feedback gain matrix with two nonzero positive gains, namely, $k1$ and $k2$. The existence condition of sliding-mode control is expressed as

$\dot{s}e>0, \ whense<0$

$\dot{s}e>0, whense<0$ (6)

If u in (1) is chosen by the following variable-structure control law:

$u=+1,forse>0$

$u=-1,forse<0$ (7)

Such that it complies with the existence condition (6), the system will then operate in sliding mode, and zewill tend toward the origin. It is shown in [11] that, under sliding mode, the error state dynamics is governed by the state-space equation

$\dot{ze}= F^*ze$ (8)

Where

$$F^*=\begin{bmatrix}\frac{-K_2}{K_1} & 0\\ 1 & 0\end{bmatrix}$$

For a positive value of ($k2/k1$), the sliding surface is stable. The states under sliding mode follow the references independent of the system and load parameters [13].

Under ideal sliding-mode control (7), the switches used in the VSI need to be fully rated and operate at very high switching frequency.Amultiband hysteresis modulation using a cascaded multilevel inverter will be discussed hereinafter so as to bring the device ratings into the limits of practical insulated-gate bipolar-transistor (IGBT) switches with the desired maximum switching frequency.

III. MULTIBAND HYSTERESIS MODULATION

The graphical representations of the cascaded multilevel inverter with the proposed generalized multiband hysteresis

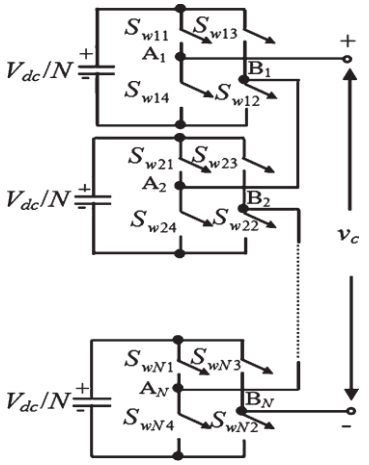

Fig.2.Cascaded n-level inverter using N number of H-bridges.

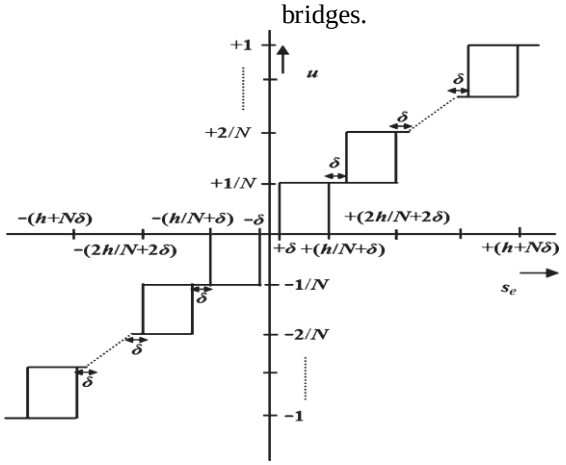

Fig. 3.Multiband hysteresis modulation.

Modulations are shown in Figs. 2 and 3, respectively, [20]. Fig. 2 shows a general n-level (n = 3, 5, 7 . . .) cascaded multilevel inverter topology. The basic building block of the cascadedinverter is an H-bridge. The switches Sw11, Sw12,. . .SwN4shown in Fig. 2 represent an IGBT with an anti parallel diode. The number of such H-bridges required for an n-level inverter is $N = (n - 1)/2$. For higher voltage/power-rating applications, the switching frequency and device ratings are limited. Therefore, it is desirable to distribute the voltage and power stress among the number of devices. For an n-level inverter, the voltage stress on the semiconductor switches and the dc-link capacitor is 1/N times the net dc-link voltage Vdcrequired. The voltage output of the n-level inverter is denoted by $vc= uVdc$. Fig. 3 shows the proposed multiband hysteresis modulation.The frequency spectrum of the output voltage can be appropriately shifted to the high-frequency region

and that the magnitude of the switching harmonics in the output voltage will also be reduced significantly.

The number of hysteresis loops in each odd quadrant, as shown in Fig. 3, is *N*, which is the same as the number of H-bridges in the cascaded multilevel inverter. Parameter *h* is the net hysteresis band, and δ is a small dead zone introduced to avoid any overlapping between adjoining loops [20].

A. Seven-Level Modulation

For a Seven-level modulation, three H-bridges are required. The corresponding multiband hysteresis modulation is shown graphically in Fig 2.The detailed control algorithm for a seven-level inverter based on the multiband hysteresis modulation is described in the Following:

Condition 1:*ifse(t)>0, then*
Condition 1.1:
ifse(t)>+ δ, then
u(t)= +1/2, for+(h/2+δ)<se(t)<+(h/2+2δ)
u(t)= +0 for se(t)<δ

Condition 1.2 :

ifse(t)>+(h/2+2δ), then

u(t)= +1, for se(t)>+(h+2δ)
u(t)= +1/2, for se(t)<+(h/2+2δ) *(9a)*

Condition 2 :*ifse(t)<0, then* *Case* 2:*Sw*23 is ON, for
Condition 2.1 :
ifse(t)<−δ, then
u(t)= −1/2, for –(h/2+δ)>se(t)>−(h/2+2δ)
u(t)= +0, for se(t)>−δ
Condition 2.2 :
Ifse(t)<−(h/2+2δ), then
u(t)= −1, for se(t)<−(h+2δ)
u(t)= −1/2, for se(t)>−(h/2+2δ) (9b)

With this scheme, the modulator has seven levels of output, i.e., $u = -1, -1/2, -3/2, 0, +3/2, +1/2$, and +1. The time-domain representation of seven-level hysteresis modulation, showing switching function *se*(*t*) and seven-level switching logic *u*(*t*), following the algorithm (9a) and (9b).

B. Hierarchical Switching Scheme

There are many switching combinations for obtaining the same level of inverter output voltage [25]. In this section, a switching scheme is proposed to follow the algorithm given in (9) for obtaining the seven-level output, which can easily beextended to the further higher level inverter. The scheme leads to a unique switching pattern corresponding to each level in the output. In this scheme, the switching stress of all the switches of the same H-bridge is equal. For the seven-level modulation discussed in the previous section, the following two hierarchies are chosen, 1) level-3 H-bridge,2) level-5 H-bridge and 3) level-7 H-bridge

For Condition 1 in (9a), the left-leg switches of both H-bridges shown are kept at low switching frequency, i.e., switches Sw11, Sw14,Sw21, and Sw24change their states at the fundamental frequency as follows:

Condition 1:*se>0*, Switches Sw1 andSw21are ON. (10a)

Under steady-state condition, switching function sevaries at the fundamental frequency. Therefore, the left-leg switches operate at this frequency for the positive half-cycle.

The right-leg switches of the H-bridges, i.e., Sw13, Sw12, Sw23, and Sw22, operate at high switching frequency for the positive half-cycle of switching function *se*, following the multiband hysteresis modulation. Each hierarchical bridge will operate for that corresponding level of the output only. The position of switches in the other H-bridge will remain fixed in this period. Consider the various cases of *Condition 1* in (9) as follows.

Condition 1.1: (Level-3 operation); *se* >+δ,switch*Sw*23 Remains ON, and

Case 1:*Sw*12 is ON, for *u*=+1/2, such that *vc*=+*V*dc/2
Case 2:*Sw*13 is ON, for*u*=0, such that *vc*=0.

Condition 1.2: (Level-5 operation); *se* >+(*h*/2 + 2δ), SwitchSw12 remains ON, and

Case 1:*Sw*22 is ON for *u*=+1, such that *vc*=+*V*dc
*Case 2: Sw23*is ON for *u*=+1/2, such that *vc*=+*V*dc/2

Now, for Condition 2in (9b), i.e., *se <0*, the right-leg switches of all the H-bridges are kept at low switching frequency, i.e., switches Sw13,Sw12, Sw23, and Sw22 change their states at the fundamental frequency for the negative half-cycleof*se* as follows:
Condition 2:*Se*<0, switches *Sw*13 and *Sw*23 are ON.
(10b)
The left-leg switches, in this case, i.e., Sw11, Sw14,Sw21, and Sw24, operate at high switching frequency for the negative half-cycle of switching function *se*.

Condition 2.1: (Level-3 operation); *se* <−δ, switch *Sw*21 Remains ON, and

Case 1:Sw14 is ON, for *u*=−1/2, Such that *VC*=−*Vdc/2*
Case 2:*Sw*11 is ON, for *u*=0, Such that *VC*=0.

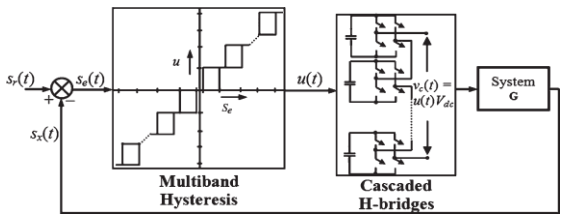

Fig. 4 Block diagram for a generalized *n*-level-inverter-controlled system using multiband hysteresis modulation

Condition 2.2: (Level-5 operation); *se* <− (*h*/2 + 2*δ*), SwitchSw14 remains ON, and
Case 1:*Sw*24 is ON, for *u*=−1,
Such that *VC*=−*V*dc
Case 2:*Sw*21 is ON, for *u*=−1/2,
such that *vc*=−*V*dc/2.

The hierarchical switching scheme can easily be extended to any higher level inverter modulation. For an *n*-level inverter, there are *N* hierarchical H-bridges. Each is assigned as level-3, level-5 . . . or level-*n* H-bridge. It will be shown in the following section that a sequential change in the hierarchy of each H-bridge leads to the equal average switching of all the H-bridges.

C. Switching Characterization

In this section, an expression relating the desired maximum switching frequency *fc* of the switching elements in the H-bridges of the cascaded multilevel inverter, and the hysteresis band *h* of the multiband hysteresis modulation, as shown in Fig. 3, has been obtained.

The block diagram represents the steady state condition of the system [13], [15]. Under steady state, it is assumed that the low-frequency reference vectorss*r*is tracked by the controlled vector *sx*against low-frequency perturbations such as source voltage and nonlinear load under closed loop. The difference of the two vectors generates switching function *se*, as given by (4). Using (1), the following systems are defined:

$$Gu(s)=V\text{dc}G(s)$$
$$=K(sI-F)^{-1}g1$$
$$=\frac{(V_{dc}/C_fL_T)(k_1s+k_2)}{s^2+(R_T/L_T)s+(1/C_fL_T)} \quad (11)$$

It has been shown in [13] that the hysteresis band *h* required for a given maximum switching frequency *fc*(= *ωc*/2*π*), using the switching transition concept of Tsypkin's method, for a two level hysteresis modulation shown in Fig. 7, can be obtained using the following:

$$h = -4\pi \text{Im}\,(H(\omega c)) \quad (12)$$

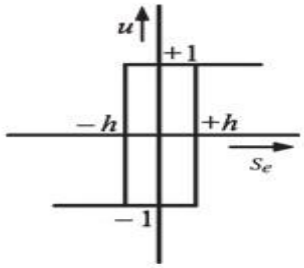

Fig. 5Two-level hysteresis modulation.

Where

$$\text{Im}\{H(\omega_C)\}=\sum_{n=1(2)}^{\infty}\frac{1}{n}\text{Im}\{G_u(jn\omega_C)\}$$

Also, it is well known from the describing-function theory that the describing function of the nonlinear hysteresis shown in Fig. 5 with hysteresis band *h* is given by [23]

$$N_X(X)=\frac{4}{\pi X^2}\left[\left(X^2-h^2\right)^{1/2}-jh\right] \quad (13)$$

Its inverse can be obtained as

$$-\frac{1}{N_X(X)}=-\frac{\pi}{4}\left[\left(X^2-h^2\right)^{1/2}+jh\right] \quad (14)$$

Where *X* is the amplitude of the limit cycle and represents the minimum amplitude of switching ripples in switching function*se*[13], over one cycle of the fundamental frequency, basedupon the first harmonic linearization. Equating (14) and system transfer function *Gu*(*jω*) gives relation (12), based upon the first harmonic approximation at frequency *ωc*.

Proposition 1:The effective maximum switching frequency*fc*e, as seen in the output of an *n*-level inverter, following the multiband hysteresis modulation shown in Fig. 3, is the sameas that for the two-level inverter, i.e., *fc* with the same net hysteresis band length *h*. The magnitude of switching ripplesin the output is reduced by 1/2*N* times as compared to that present in the case of the two-level inverter.

Proof:It is assumed that the variable-structure control for multiband hysteresis modulation satisfies the existence condition(6) for the switching surface *se* shifted correspondingly for different levels in Fig. 3. Consider now the *n*-level inverter operating in a *k*ith level at a particular instant under steady state. Then, the (*k* − 1)/2 = *p*thH-bridge having a *k*ithhierarchy must be operating at that particular instant following the *p*thband in Fig. 3. For example, if a five-level inverter is used and if this inverter is at level-3 operation at a particular instant under steady state, then the first H-bridge must be operating following the first hysteresis band in the first quadrant and this H-bridge has a level-3 hierarchy. Consider again the *Pth*hysteresis band in Fig. 3. The hysteresis band length starts from [(*p* − 1)*h*/*N* + *pδ*] and ends at [*ph*/*N* + *pδ*].The output levels corresponding to these points are (*p* − 1)/*N*and *p*/*N*, respectively. Therefore, the net band length is *h*/*N*,and the difference in the net operating level is 1/*N*. Now, let usplace this hysteresis band symmetrically around the origin, as.

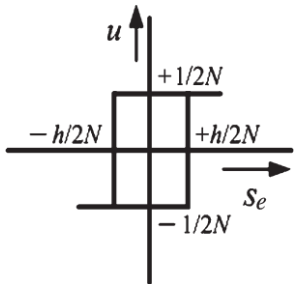

Fig. 6.Switching characterization of an *n*-level inverter using the *PTH* hysteresis band.

Shown in Fig. 6. This is based on the assumption made earlier that switching surface *se* may be shifted correspondingly for different levels for the purpose of analysis. The describing function of the hysteresis band shown in Fig. 6 can be obtained as

$$N_{X'}(X') = \frac{1}{\pi(NX')^2}\left[\left\{(2NX')^2 - h^2\right\}^{1/2} - jh\right] \quad (15)$$

whereX_{-} is a limit-cycle amplitude in switching function *se* for an *n*-level-inverter-controlled system. The negative inverse of (15) yields

$$-\frac{1}{N_{X'}(X')} = \frac{\pi}{4}\left[\left\{(2NX')^2 - h^2\right\}^{1/2} + jh\right] \quad (16)$$

By comparing (16) with (14), it can be seen that the imaginary parts of the two equations are the same. Therefore, this leads to the same condition (12) of the switching of the two level inverter. Hence, the effective maximum switching frequency *f*ceof an *n*-level inverter and the maximum switching frequency *fc* of a two-level inverter, for the same net hysteresis band *h*, are the same. Although, on instantaneous basis, the number of switches participating in this switching operation is two out of 4*N* switches in a multilevel inverter, therefore the average switching frequency of each switch will be less than *f*ce/2*N*. The switching loss will also be distributed in the case of the multilevel inverter. A comparison of the real parts of (14) and (16) yields the following:

$$X' = \frac{X}{2N} \quad (17)$$

This implies that the amplitude of the limit cycle or ripples in switching function *se* is reduced by 1/2*N* times as compared to that for the two-level inverter. Also, since switching input *u* togglesbetween −1, . . . ,−2/*N*,−1/*N*, 0, +1/*N*, 2/*N*, . . . , +1,the net pulse height of the switching pulses are 1/*N* comparedto (1 −(−1)) = 2 in the case of the two-level inverter.Hence, the magnitude of switching ripples in the output ofthe multilevel-inverter-controlled system is reduced to (1/2*N*)times as compared to the two-level-inverter-controlled systemfor the same effective switching frequency.

IV. MATLAB/SIMULINK MODEL and SIMULATION RESULTS

Case 1: Five level inverter as DSTATCOM

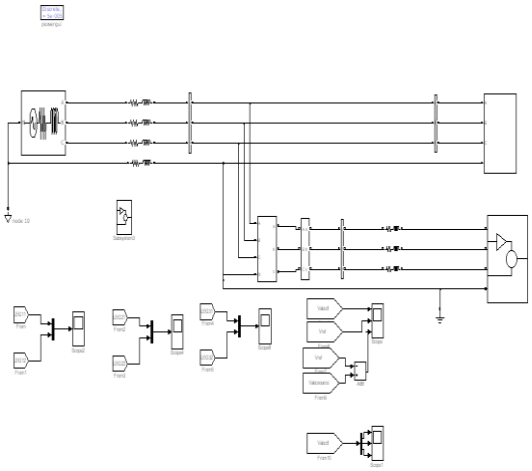

Fig. 7 Simulation circuit of DSTATCOM with 5-level VSI.

Fig.7 shows the simulation circuit of the DSTATCOM with 5-level inverter topology.

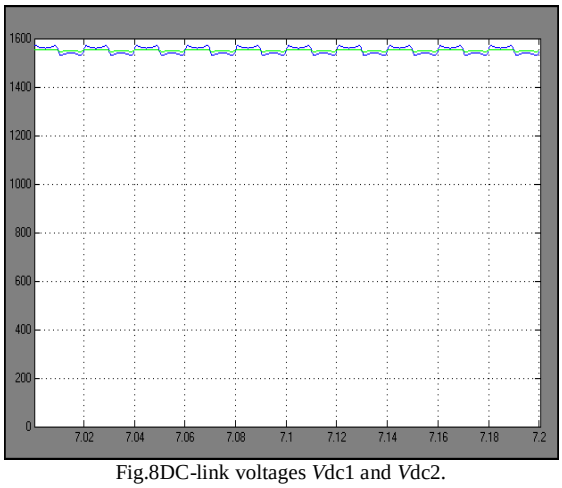

Fig.8DC-link voltages *V*dc1 and *V*dc2.

Fig.8shows the DC-link voltages Vdc1 and Vdc2, which varies with the operation of the DSTATCOM.

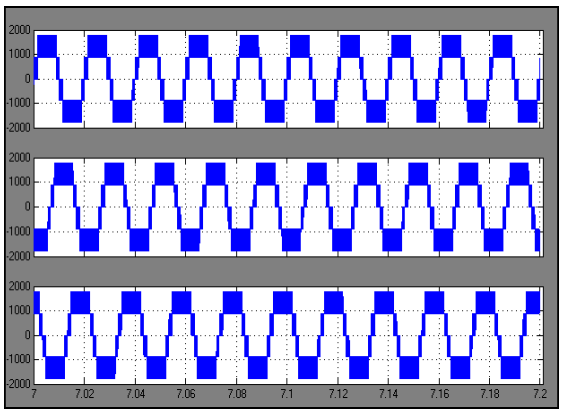

Fig.9Five-level-inverter output voltages of three phases.

Fig.9 shows the five level inverter output voltages of the three phases.

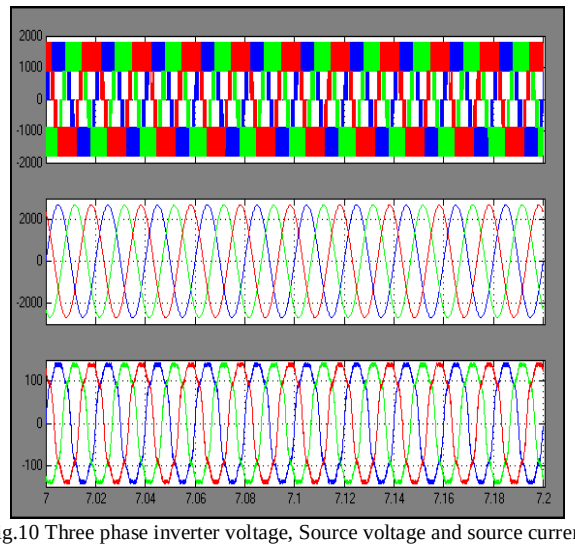

Fig.10 Three phase inverter voltage, Source voltage and source current

Fig.10 shows the three phase inverter output voltage, source voltage and current which ae not having harmonics.

Case 2:Seven level inverter as DSTATCOM

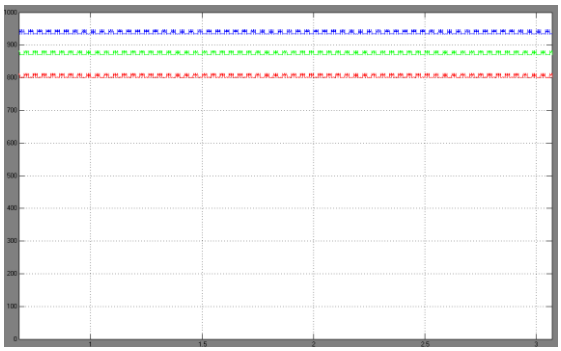

Fig. 11DC-link voltages *V*dc1 and *V*dc2.

Fig. 11 shows the DC-link voltage of Vdc1 and Vdc2 of leg 1 of seven levels VSI.

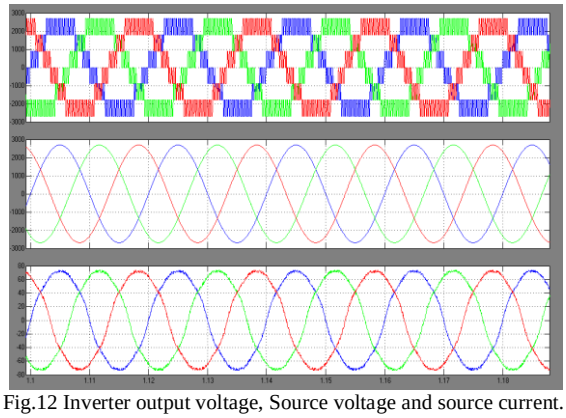

Fig.12 Inverter output voltage, Source voltage and source current.

Fig.12 shows the output voltage waveform the inverter, source voltage and source current of the system with seven level DSTATCOM.

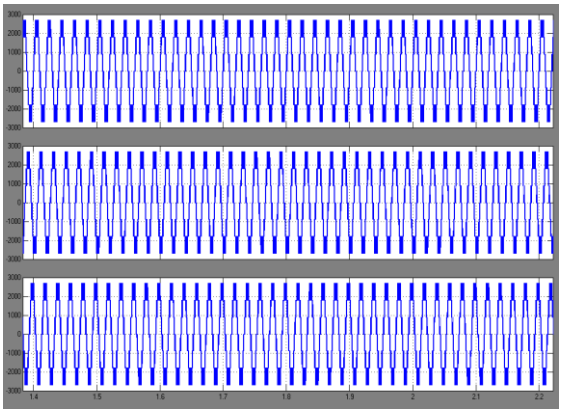

Fig.13 Seven level inverter output voltages of the inverter.

Fig.13 shows the seven level inverter output voltages of the inverter which is connected to the system.

VI. CONCLUSION

In this paper, a proposal has been made for a DSTATCOM based on a five-level and seven levels Cascaded multilevel inverter. The basic concepts and structure of the DSTATCOM are discussed. The multiband hysteresis modulation proposed in this paper has shifted the switching components toward higher frequencies and has hence reduced the switching ripple content in the output controlled voltage. The simulation results verify the control scheme proposed. The sequential swapping of hierarchy for each cell yields the self-balancing capability in case the dc-link voltage is supported by the capacitors. The simulation results confirm that the proposed DSTATCOM offers satisfactory performance.

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