International Journal of Modern Engineering Research (IJMER)
www.ijmer.com Vol. 3, Issue. 4, Jul - Aug. 2013 pp-1994-1998 ISSN: 2249-6645

Complex test pattern generation for high speed fault diagnosis in Embedded SRAM

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Abstract: *The memory blocks testing is a separate testing procedure followed in VLSI testing. The memory blocks testing involve writing a specific bit sequences in the memory locations and reading them again. This type of test is called March test. A particular March test consists of a sequence of writes followed by reads with increasing or decreasing address. For example the March B test has the following test pattern. ↕(W0)↑(R0,W1,R1,W0,R0,W1)↑(R1,W0,W1)↓(R1,W0,W1,W0)↓(R0,W1,W0) There are several test circuits available for testing the memory chips. However no test setup is developed so far for testing the memory blocks inside the FPGA. The SRAM blocks of FPGA are designed to work at much higher frequency than the FPGA core logic. Hence testing the SRAMs at higher speed is essential. The conventional memory test circuits cannot be used for this purpose. Hence the proposed work develops a memory testing tool based on March tests for FPGA based SRAM (Block RAM testing). The code modules for March test generator shall be developed in VHDL and shall be synthesized for Xilinx Spartan 3 Family device. A PC based GUI tool shall send command to FPGA using serial port for selecting the type of test. The FPGA core gets the command through UART and performs the appropriate and sends the test report back to PC. The results shall be verified in simulation with Xilinx ISE simulator and also in hardware by using Chip scope. Xilinx Spartan 3 family FPGA board shall be used for hardware verification of the developed March test generator.*

Key words: *SRAM block, FPGA, VLSI-very large scale integration.*

I. INTRODUCTION

Nowadays, the area occupied by embedded memories in System-on-Chip (soc) is over 90 %, and expected to rise up to 94% by 2014 [1]. Thus, the performance and yield of embedded memories will dominate that of SOCs. However, memory fabrication yield is limited largely by random defects, random oxide pinholes, and random leakage defects. Gross processing and assembly faults, specific processing faults, misalignments, gross photo defects and other faults and defects [2].

This paper aims to propose a new solution for researchers and engineers to find a efficient test and diagnosis algorithm in shorter time. A combinational march-based test algorithm will be implemented for this purpose. Universities and industry involved in memory Built-in-Self test, Built-in-self diagnose will benefit by saving a few years on research and development developed in this work is compatible and expandable for SRAM memory due to fact the manual and automatic test procedure testing.

In this article, we present an original memory test frame work: an SRAM memory test bench, roaming and programmable. This test bench allows not only to employ different commercial SRAM memories but also to apply various algorithms for test. With this new test bench, students can concertize the memories testing's lectures and enlightened the inherent properties of the various applied algorithms as well as the difference between the memory architectures and technologies.

II. MARCH TEST GENERATOR

The memory blocks testing involve writing a specific bit sequences in the memory locations and reading them again [3]. This type of test is called March test. A March test consists of a sequence of March elements. A March elements has a certain number of operations (or March primitives) that must be applied to all memory cells of an arrays. Thus, ↑ (r0; w1) is a March element and r0 and w1 are March primitives. The addressing order of a March element can be done in an up (↑), down (↓) way or (↕) if the order is not significant .A March primitive can be a write 1 (w1), write 0 (w0), read 0 (r0) that can be performed ina memory cell. There are many March tests such as March SR, March C-, March B, and so on. March B chosen in this paper because it has better fault coverage Than March SR and March C- . March B is an efficient and economical memory test should provide best fault coverage in the shortest time [4].

March **B algorithm** has following steps :
↕ (W0) ↑(R0,W1,R1,W0,R0,W1)↑(R1,W0,W1)
↓(R1,W0,W1,W0)↓(R0,W1,W0)

In the above steps, "up" represent executing SRAM address in ascending order while "down" in descending order. This well-know March test allows to detect all the stuck @ and transition fault of a memory cell array, as well as all address decoder faults and coupling (interaction between two cells) faults.

The following figure shows the sequences of March tests to be applied to the SRAMs of FPGA.

March C-	↕(W0) ↑(R0,W1) ↑(R1,W0) ↓(R0,W1) ↓(R1,W0) ↕(R0)
March SR	↓(W0) ↑(R0,W1,R1,W0) ↓(R0,R0) ↑(W1) ↓(R1,W0,R0,W1) ↑(R1,R1)
March B	↕ (W0) ↑(R0,W1,R1,W0,R0,W1) ↑(R1,W0,W1) ↓(R1,W0,W1,W0) ↓(R0,W1,W0)

Fig 2.1: March Test Sequence

III. TEST BENCH ARCHITECTURE

Our test bench architecture for memories is composed of one computer, a March test generator, a serial interface (for communication between the programmable generator and the computer) and SRAMs on FPGA.

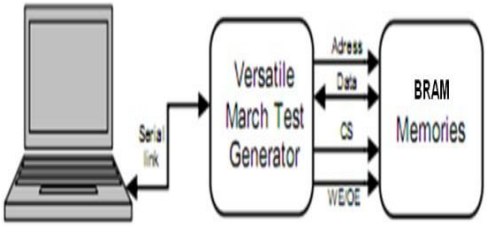

Fig 3.1: Test Bench Architecture

A user interface allows us to choose or set a specific March test. The chosen March test is uploaded through the serial connection to the Programmable test generator and then applied to SRAMs of FPGA.

If no fault is detected, the programmable generator returns a positive acknowledgement on the SRAM. Whether the opposite case occurs, i.e; when a reading operation (r0 or r1) does not return the expected data: the failing memory, the failing address, the failing march element and operation. Only the knowledge of physical defects beside the observed fault, or at least to make reasonable suppositions.

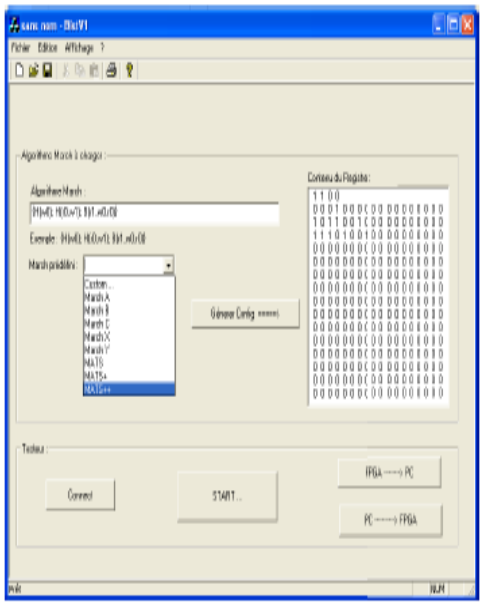

Fig 3.2: User Interface

IV. EXPERIMENTAL RESULTS

The following chapter consists of all the software and hardware results observed in the project. The results include snapshots of each and every module individually with all the inputs, outputs and intermediate waveforms.

4.1 Simulation results

Figure 4.1: Data output of SRAM using March C

- The written input values into SRAM with expected values. are read
- Here the contents of SRAM are read without any failure.
- Hence March test C- is Successful and SRAM is fault Free.

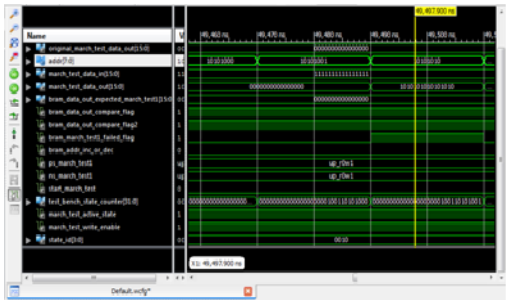

Figure 4.2: Data output of SRAM using March C- with Fault insertion

- The written input values into SRAM are read with expected values except at address "aa".
- Here the contents of SRAM are read with fault.
- Hence March test C- is Successful and SRAM is faulty.

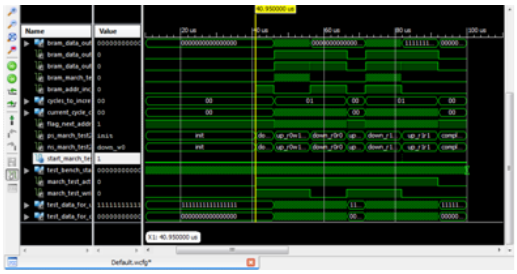

Figure 4.3: Data output of SRAM Using March SR

- The written input values into SRAM are read with expected values.
- Here the contents of SRAM are read without any failure.
- Hence March SR test is Successful and SRAM is fault Free.

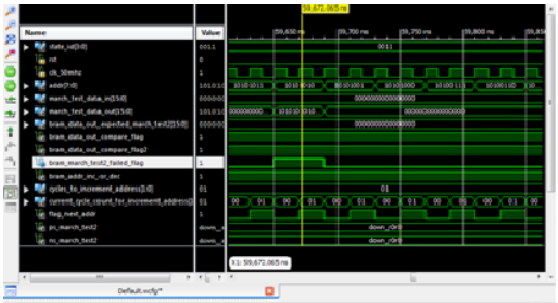

Figure 4.4: Data output of SRAM using March SR with Fault insertion

- The written input values into SRAM are read with expected values except at address "aa".
- Here the contents of SRAM are read with fault.
- Hence March SR test is Successful and SRAM is faulty.

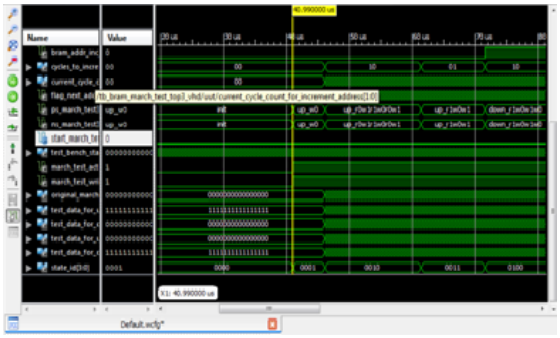

Figure 4.5: Data output of SRAM using March B

- The written input values into SRAM are read with expected values.
- Here the contents of SRAM are read without any failure.
- Hence March B test is Successful and SRAM is fault Free.

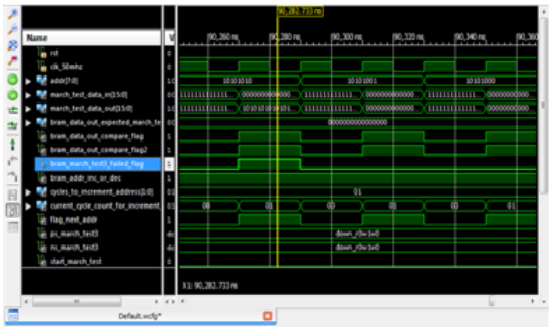

Figure 4.6: Data output of SRAM using March B with fault insertion

- The written input values into SRAM are read with expected values except at address "aa".
- Here the contents of SRAM are read with fault.
- Hence March B test is Successful and SRAM is faulty.

4.2 CHIP SCOPE RESULTS

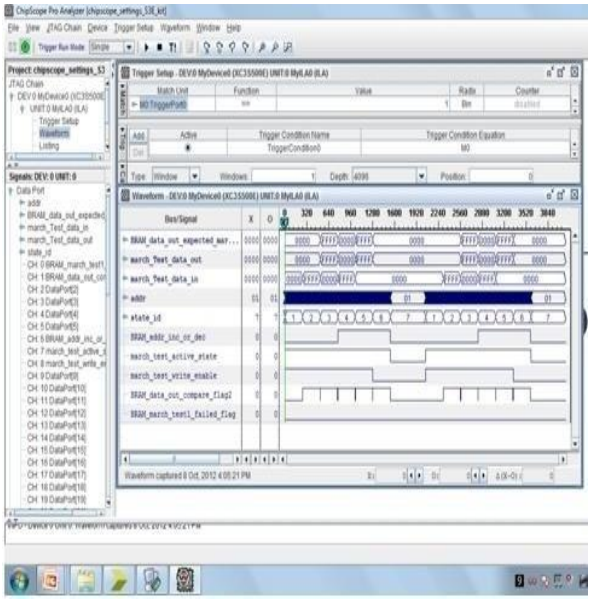

Figure 4.7: Data output of SRAM using March B

V. CONCLUSION

The generation and refinement of this teaching frame work come from the observation that the teaching of the test of the integrated circuits is too often approach in theoretical or virtual ways. We believe that, for our engineering

students, it would be important to have the opportunity to develop theoretical and practical skills to generate adequate test solution for actual electronic device .Although this platform has still to be improved the early feedback of our students is very encouraging. In all cases, they have affirmed to have clearly understood the way March test sequences are applied to have clearly understood the way March test sequence are applied to memories as well as the sensitization and observation process of the various fault models. Moreover, they also showed to have highly perfected their knowledge of the memory architecture and function.

REFERENCES

[1] Semiconductor Industry Association, "International technology roadmap for semiconductors (TTRS), 2003 edition," Hsinchu, Taiwan, Dec.2003.
[2] C. Stapper, A Mclaren, and M Dreckman, "Yield model for productivity optimization of VLSI Memory Chips with redundancy and partially good product," IBM Journal of Research and Development, Vol 24, No. 23, pp.398-409, May 1980.
[3] A.J Van de Goor, "Testing Semiconductor Memories: Theory and Practice, "John Wiley & Sons, ISBN 0-471-92586-1, 1991
[4] Pavlov. Andrei and Sachedev. Manoj, CMOS SRAM Circuit Design and parametric Test in Nano-Scaled Technologies, CA: Springer, 2008, pp.85-86.

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