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Optimized CAM Design

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Abstract: *Content-addressable memories (CAMs) are hardware search engines that are faster than algorithmic approaches for searching applications. CAMs consist of conventional semiconductor memory (usually SRAM) with added comparison circuitry that performs search operation to complete in a unique clock cycle. In case of sophisticated and high end applications we need large sized CAM which utilizes large amount of power but this has to be avoided. This paper proposes an idea for improving power, area and performance of the system of recently proposed high Performance Hybrid-Type CAM Designs. For this we replace the basic 9T CAM cell with a 4T CAM cell. The simulation results show the success of the method.*

Key words: *Basic 9T CAM cell, 4T CAM cell, NOR-Type Array, NAND-Type Array, Hybrid CAM Design.*

I. INTRODUCTION

Content Addressable Memory is used to access the memory through the data rather than the address which is used in the case of normal RAM's. The output of the CAM will be the location where the associated content is stored. In CAM with parallel comparison feature the power consumption is lesser than the normal CAM. In case of CAM, the input data and the stored data are being compared, if both matches then the match line are used to indicate it. Due to its low power and fast matching capability it is mainly used in advanced applications like Strong ARM processors, ATM switches, etc.

In this paper we are designing a Hybrid Type CAM[7] design so that it should have low power and high performance. Normally basic CAM cell consists of 9 transistors to write, read and match the data. It consists of both store unit and match unit. The main drawback of this basic CAM cell is that it occupies more area, needs more power and has large delay. So we need to explore modifications to it so that area, power and performance can be improved. So we are designing 4 transistor CAM cell[8] such that these can be effectively used in many applications.

In the design CAM different techniques have been proposed to reduce the power consumption and improve the performance of the CAM cell. A CAM cell design with XOR and XNOR blocks were designed [2], with different combinations of pmos and nmos transistors, depending upon the type of application. But the main drawback of the proposed design are usage of more number of transistors and more power consumption. A two stage CAM cell design is proposed [3], to reduce power consumption where a control circuitry consisting of an inverter is used between the two stages. Performance of this CAM cell design is degraded in this design and there exists the disadvantage of short circuit power dissipation. A static pseudo nmos CAM has been designed[4] which requires an extra pmos transistor for every CAM cell which use in it, so it is very bad idea to for each and every pmos for each stages. Other method has been designed which requires separate cmos parallel CAM for searching the data[5] which requires lot of area to implement it and also extra precharge device[6] to implement CAM. To overcome the disadvantages of the previous designs a Hybrid-Type CAM design[7] is proposed to improve the power, area and performance of the CAM cell. This consists of both the NOR-type CAM design for the high performance and NAND-type CAM design for Low-Power, as constraints.

II. BASIC CONTENT ADDRESSABLE MEMORY

Basic CAM cell consists of both store unit for storing the data and compare unit for comparing the data. We store the data using two cross-

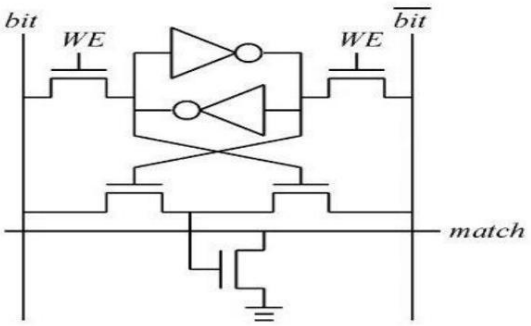

Fig 1: Basic XOR CAM cell

coupled inverters and is implemented with 6T SRAM cell. The compare unit is designed using pass transistors. The fast pull down transistor is used to discharge the data so that it indicates whether the data is matched. Depending on different applications the compare unit can be designed with XOR type or XNOR type blocks. The main operation of CAM cell can be described as: when the cross- coupled inverters store the data '1' and then the bit and nbit(bit bar/bitc) line has the data '1' and '0' respectively. Now one of the two pull down transistors will be ON state and the other will be OFF state so that there won't be any transistor path to discharge the match line and hence it remains in High-impedance state. Now if the bit

and nbit line has the data '0' and '1' respectively, then in the compare unit one of the pull down transistor will be in ON state so that the fast pull down transistor moves to ON state. This discharges the match line indicating that the data have been matched.

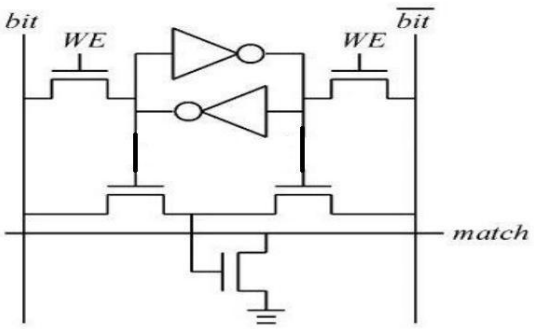

Fig 2: Basic XNOR CAM cell

III. MODIFIED CAM CELL (4T CELL)

This modified 4T CAM cell design consists of 4 nmos transistors and the cells are arranged such that the two transistors (tc1 and tco) are used to store the data and the remaining two transistors (tw1 and tw0) are used to write the data[8]. The gates of tc1('a') and tco('b') are used as storage capacitance elements so that it can be used to store the data as shown in fig 3. When the transistors tw1 and tw0 are in ON state the data can be transferred to the nodes a and b and then these can be read using transistors tc1 and tc0.

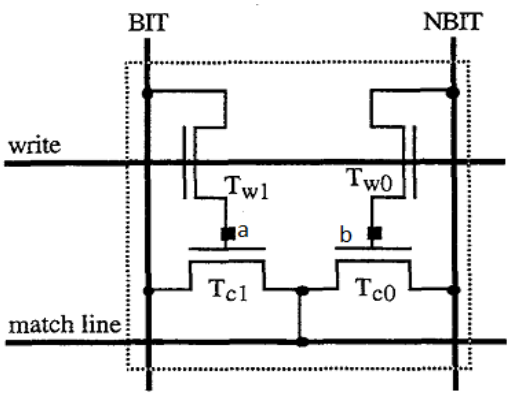

Fig 3:4T XOR CAM cell

Normally matching operation can be done using match line that is connected to the output of the XOR type transistors which are arranged using transistors tc1 and tc0. If the match line output is at logic '1' that indicates that the 'data stored' and the 'input data' are matched. If the match line output is at logic '0', it indicates that there is no match and then the match line gets discharged. Basically in this operation, first the match line has to be charged to logic '1' by using precharge transistor and then the matching operation can be done. Even in case of mismatch, the match line needs to be discharged, which can be done by using read transistor that is arranged between match line and ground. Fig 4. Shows the 4T XNOR CAMCell.

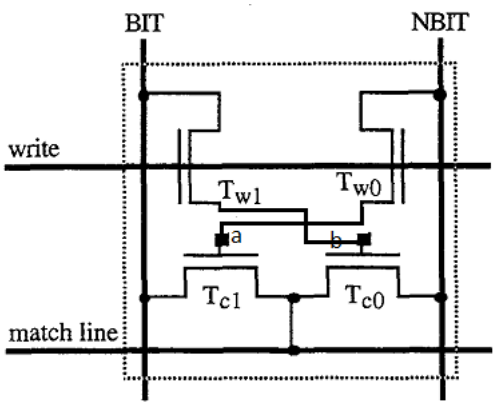

Fig 4: 4T XNOR CAM cell

IV. NOR-TYPE CAM ARRAY

In NOR-type CAM cell design, XOR-type CAM cell is used for better performance of the system. Here the pull-down transistors are arranged in NOR fashion so that it can discharge very fast and hence the performance improves. In case of pre-charge, the Match-line is precharged to HIGH.

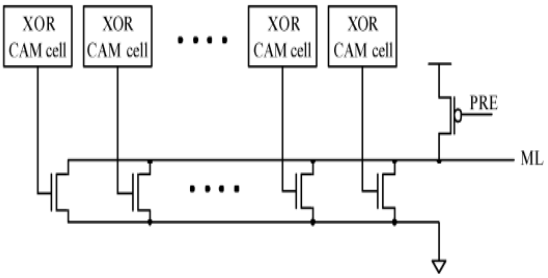

Fig 5: NOR type CAM Array

In the Evaluation phase, if the input data is matched with the stored data then the match line remains HIGH and if all the cells are mismatched then the Match-line will discharge through the pull-down transistors. Thus the NOR-type CAM cell provides better performance. But the drawback in this design is increase in Drain-Capacitance due to more number of transistors. This drawback, increases Power consumption. Hence, it is only useful in case of High performance.

V. NAND-TYPE CAM ARRAY

Unlike the NOR-type CAM cell, NAND-type CAM cell is used to reduce the power consumption of the system. In this the NAND-type CAM, cell is arranged using XNOR type and the transistors are arranged in NAND fashion.

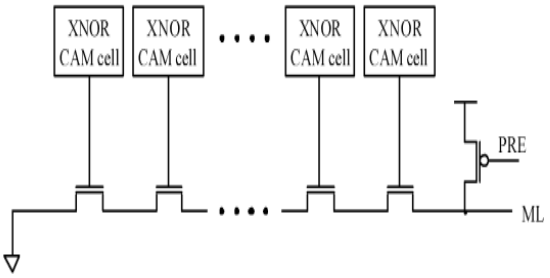

Fig 6: NAND CAM Array

Since the drain capacitance is less, the power consumption of the system is also less. In searching the data, initially the match line is precharged to HIGH, in the pre-charge phase and the match line discharges to ground in the evaluation phase, only when all the CAM cells are matched with the stored data. In case of mismatch the match line remains HIGH as in that of the pre-charge phase. Thus the power consumption of the system can be improved. But the drawback with this design is the time taken to discharge the match line is more, as it has long pull-down path. Hence, this NAND-type design is performance inefficient/slow.

VI. HYBRID-TYPE CAM DESIGN

Hybrid-type CAM design consists of both NOR-type Array with XOR CAM cell for performance advantage and NAND-type Array with XNOR CAM cell for power advantage. Mainly we divide the complete circuit into 3 parts namely, SEG1, SEG2 and CONTROL circuitry. In the SEG 1, we design the circuit using XNOR type and then arrange the pull-down transistors using NAND-type. In the SEG 2, we design the circuit using XOR type and the pull-down transistors are arranged in NOR type design as shown in fig.7.

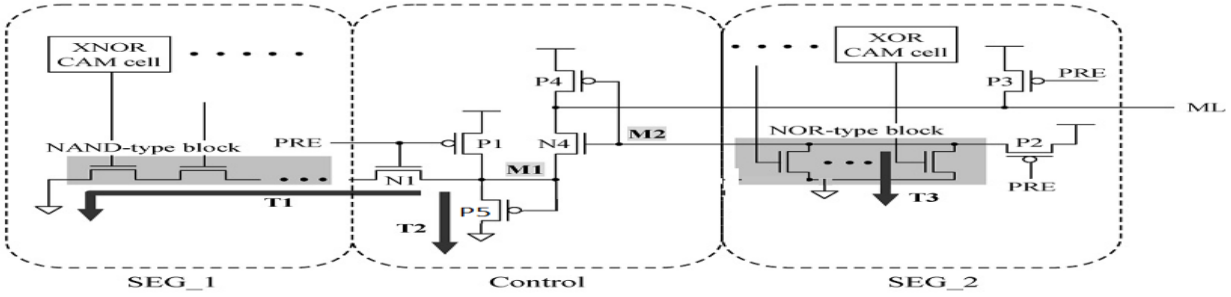

Fig 7: HYBRID CAM Structure [Ref 7]

SEARCH OPERATION OF CAM CELL

In case of searching a data, the input data is compared with that of stored data. The circuit operates in two different phases namely Pre-charge phase and Evaluation Phase. In Pre-charge phase the Match-line is kept in HIGH state and in the Evaluation Phase the state of Match-line depends upon the data matched.

1. PRE-CHARGE PHASE

The control signal PRE is kept LOW so that the circuit starts to Pre-charge. Thus when the PRE signal is kept LOW the match line that is connected to one of the pmos transistor **P3** is made to be in HIGH state. In this circuit we have 3 discharge paths namely **T1,T2 and T3** that are connected to three transistors **N1, P5 and NOR block** respectively. As both the nodes **M1** and **M2** are HIGH, there are no discharge paths for the Match-line in this phase. As there is no chance of discharging the data, the Match-line doesn't require much power. This design is very efficient in Power saving.

2. MATCH-EVALUATION PHASE

In this phase the control signal PRE is made HIGH to start the matching process of the design. The data to be searched is given to the bit lines of the CAM cell. When we search the data we come across 4 different cases but the exact matching occurs only when both the segments are matched. The voltages of each node are shown in Table.1. The detailed explanation of this matching process is given below.

Case1: In this case, SEG1 is mismatched and SEG2 is mismatched or matched. As the SEG1 is mismatched there exists no discharge path because there may be at least one transistor that is OFF. So the node voltage M1 remains HIGH and hence, there won't be any discharge path. Thus in this case the matching process doesn't depend on the SEG2. As there is no discharge path the Match-line still remains in the HIGH state.

Case2: In this case, SEG1 is matched and SEG2 is mismatched. As the SEG1 is matched all the transistors that are connected in the NAND fashion are in ON state, so that there exists a discharge path through the path T1. And thus, the node M1 remains LOW and the two pull-down transistor **P5** gets ON and so, there exists a path T2 to discharge. Now as the SEG 2 is mismatched there exists at least one path to discharge through N3 so that the node M2 remains LOW. Hence in this case, there won't be any path to discharge the match-line.

	SEG 1	SEG 2	Path			Key Node			Result
			T1	T2	T3	M1	M2	ML	
Case 1	Mismatch	Mismatch	X	X	X	H	H	H	Mismatch
	Mismatch	Match	X	X	X	H	H	H	Mismatch
Case 2	Match	Mismatch	0	0	0	L	L	H	Mismatch
Case 3	Match	Match	0	0	X	L	H	L	Match

Table 1: Node Voltages of each node of HYBRID CAM Cell.

Case3: In this case, both the segments are matched. Thus, as the SEG1 is matched, the node M1 gets LOW value as there exists a discharge path. Now in case of SEG2, as it is matched all the transistors are turned OFF and the path T3 to ground is disconnected. Now the node M2 is at HIGH state making the transistor N4 to turn ON. Now there exists a path for Match-line to discharge the data, through the paths T1 or T2. As the path T2 is the fastest path to discharge the data, the Match-line discharges through the transistor P5. Thus it indicates that the data have been matched properly. In this design as we have two pull-down paths to discharge the match-line. It discharges through path T2 as path T1 has transistors connected which takes long time to discharge. Thus, this design provides better performance.

VII. EXPERIMENTAL RESULTS

0.18um technology is used to implement the design. The below Figure 8 shows all the three cases of both SEG 1 and SEG 2 that have been used to search the data .

	Power	Area(um^2)
9T	314.17pw(XOR) 316.55pw(XNOR)	65.81
4T	100.92pw(XOR) 100.829pw(XNOR)	34.04

Table 2: Comparison between 9T and 4T

Thus, 9T CAM cell is compared with 4T CAM cell and the power of the CAM cell have been reduced by 3 times as shown in Table 2.

The NOR type and NAND CAM Arrays are also compared on the basis of power and performance as shown in Tables 3 and 4.

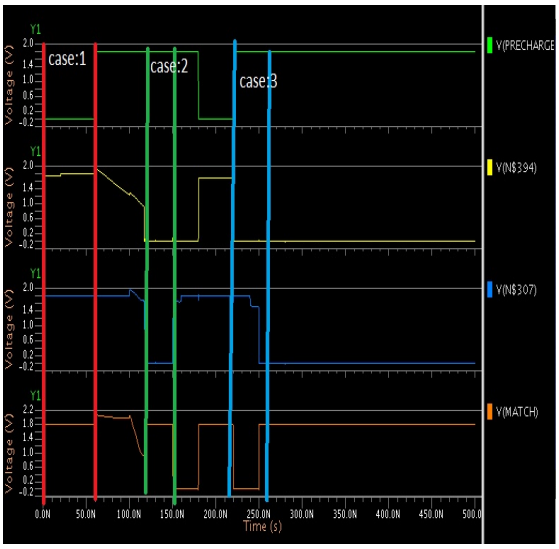

Fig 8. Simulation results of HYBRID CAM

	Power	Delay
9T	397.2uw	88.86ns
4T	19.60nw	60.9ns

Table 3: NOR Type CAM Array

	Power	Delay
9T	70.10nw	109.9ns
4T	840.25pw	69.39ns

Table 4: NAND Type CAM Array

Thus, by combining NAND type CAM Array for power efficiency and NOR type CAM Array for performance efficiency, the HYBRID DYNAMIC CAM design have been designed and it is observed that the design has low power consumption and increased performance. The total power consumption of HYBRID CAM design is shown in Table 5.

	Power	Delay
9T	38.57uw	58.12ns
4T	548.34pw	23.48ns

Table 5: HYBRID CAM Design

Thus by observing the results we can say that by replacing 9T CAM cell with 4T CAM cell the power consumption of the system has been improved and also its performance is also improved drastically. The above Figure 8 shows the simulation results of HYBRID CAM cell, done using MENTOR GRAPHICS and all the three different cases of CAM cell for matching the data is shown.

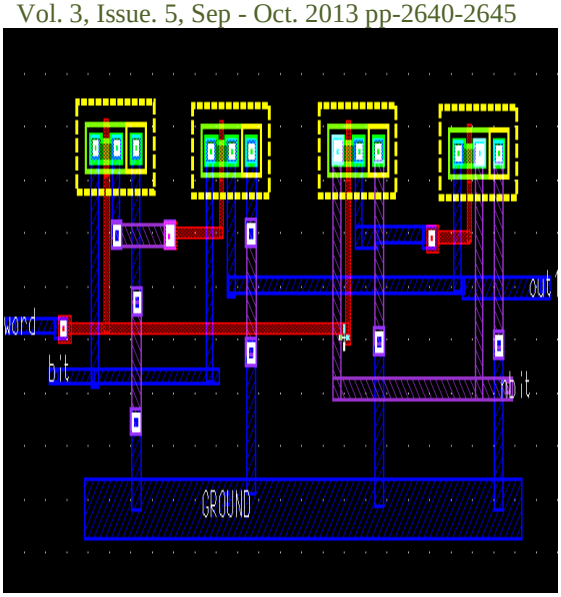

Fig 9: 4T CAM Cell layout in 0.18 um standard CMOS Technology.

VIII. CONCLUSION

Thus, a HYBRID CAM Structure has been designed for Low Power and High Performance using NOR and NAND type CAM Array and area of the complete system has been reduced by replacing 9T basic CAM cell with 4T CAM cell with a fast pull down path to accelerate the search operation.

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