International Journal of Modern Engineering Research (IJMER)
www.ijmer.com Vol. 3, Issue. 5, Sep - Oct. 2013 pp-2758-2766 ISSN: 2249-6645

Performance Evaluation of Nine Level Modified CHB Multilevel Inverter for Various PWM Strategies

P. Satheesh Kumar[1], Dr. S. P. Natarajan[2], Dr. Alamelu Nachiappan [3], Dr. B. Shanthi[4]

*(Associate professor, Department of Electrical and Electronics Engineering, Mailam Engineering College, Mailam, Tamilnadu-604304, India,)

**(Professor & Head, Department of Instrumentation Engineering, Annamalai University, Annamalai Nagar, Tamilnadu-608002, India,)

*** (Professor, Department of Electrical and Electronics Engineering, Pondicherry Engineering College, Pondicherry- 605014, India,)

**** (Professor, Centralized Instrumentation and Service Laboratory, Annamalai University, Annamalai Nagar, Tamilnadu-608002, India,)

ABSTRACT: *In this paper nine level Modified Cascaded H-Bridge Multilevel Inverter (CHB-MLI) is analyzed for the various multi-carrier Pulse Width Modulation strategies. For the same nine level inverter output this particular topology has reduced count of switches, on comparing with the conventional Cascaded H Bridge Multilevel Inverter. For a single phase, nine level inverter output this topology requires one H-bridge and a multi conversion cell. Four equal voltage sources with four controlled switches and four diodes comprise a multi conversion cell. Instead of sixteen controlled switches as in conventional method, this topology requires only eight switches to obtain nine level output. The reduction of switches lowers switching losses, cost and total harmonic distortions. Performance parameters have been analyzed for the nine level CHB-MLI.*

Keywords: *Alternate phase opposition disposition, Modified Cascaded Multilevel Inverter H-bridge Inverter, Phase disposition, Phase opposition disposition, Phase shift Pulse width Modulation, Sinusoidal Pulse Width Modulation.*

I. INTRODUCTION

Multilevel inverter (MLI) has wide range of high-power applications and feeds demands in industries in recent years. The aptness of MLI attracts the hot researchers in the direction of renewable energy sources for its numerous benefits. As renewable energy sources such as photovoltaic, wind and fuel cells can be easily interfaced to a multilevel inverter system of high power applications, MLI still gains further credit to its field. MLI can operate at high switching frequencies while producing lower order harmonic components.

A multilevel inverter is a power-electronic system that generates a desired output voltage by synthesizing several levels of dc input voltages. The main advantages of multilevel inverters are lower cost, higher performance, less electromagnetic interference, and lower harmonic content [1].The most common multilevel inverter topologies are the diode-clamped, flying-capacitor, and cascaded H-bridge inverters with separate dc voltage sources [2]. The diode clamped multilevel inverter topology, restricts the use of it to the high power range of operation. Moreover flying capacitor based multilevel inverter also exhibits a disadvantage including more number of capacitors [3].

In recent years, the cascaded H-bridge inverters have wide applications. The merit includes modularity and the ability to operate at higher voltage levels and as the number of levels increases, the quality of the output signal will be improved. In addition inverter output voltage waveform will be closer to a sinusoidal waveform [4]. Moreover, high voltages can be managed at the dc and ac sides of the inverter, while each unit endures only a part of the total dc voltage. Needs of high number of semiconductor switches, involvement of separate DC source for each of H-bridge, voltage balancing issues are the notable drawbacks of cascaded H bridge inverter.

On comparing with the usual Cascaded H-Bridge multilevel inverters, for the same nine level output, this Modified cascaded multilevel inverter topology, the number of switches used reduced from 16 switches to 8 switches. Therefore for this reason, this Modified cascaded multilevel inverter has some value of importance. Hence this paper focuses on applying various multi carrier based PWM techniques to this Modified cascaded H Bridge multilevel inverter to analyze and compare the various parameters like THD & V_{rms}.

II. MODIFIED CASCADED MULTILEVEL INVERTER TOPOLOGY DESCRIPTION

The general structure of the Modified cascaded multilevel inverter is shown in Figure 1. This inverter consists of an H Bridge and multi conversion cell which consists of four separate voltage sources (V_{dc1}, V_{dc2}, V_{dc3} and V_{dc4}), four switches and four diodes. Each source connected in cascade with other sources through a circuit consists of one active switch and one diode that can make the output voltage source only in positive polarity with several levels. Only one H-bridge is connected with multi conversion cell to acquire both positive and negative polarity.

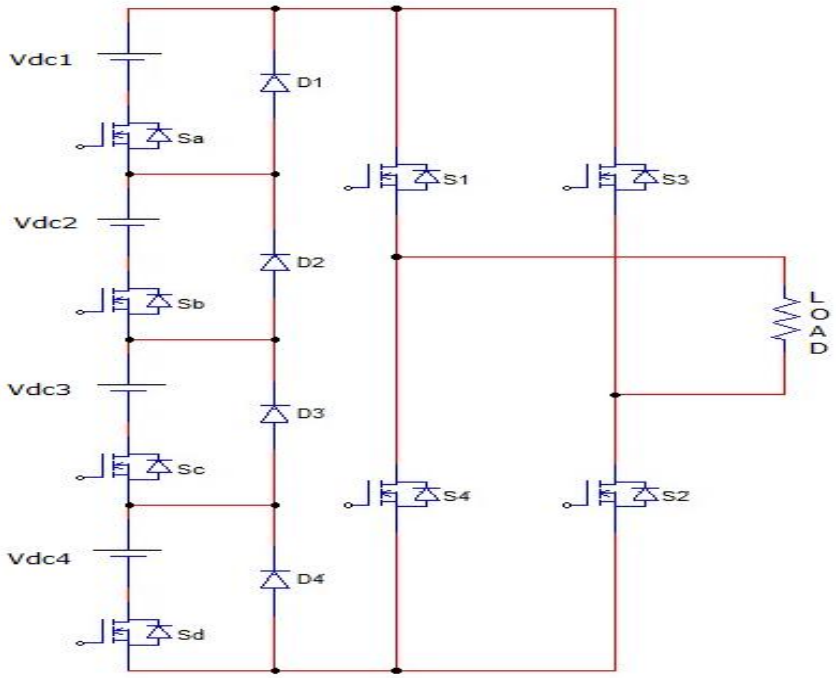

Figure 1: 9-Level Modified-Cascaded multilevel inverter

By turning on controlled switches S1 (S2, S3 and S4 turn off) the output voltage $+1V_{dc}$ (first level) is produced across the load. Similarly turning on of switches S1, S2 (S3 & S4 turn off) $+2V_{dc}$ (second level) output is produced across the load. Similarly $+3V_{dc}$ levels can be achieved by turning on S1, S2, S3 switches (S4 turn off) and $+4V_{dc}$ levels can be achieved by turning on S1, S2, S3 & S4 as shown in below Table 1.

S. No	Multi conversion Cell		H-Bridge		Voltage levels
	On switches	Off switches	On switches	Off switches	
1	S1, S2, S3, S4	D1,D2,D3,D4	Q1,Q2	Q3,Q4	$+4V_{dc}$
2	S1, S2, S3, D4	S4,D1,D2,D3	Q1,Q2	Q3,Q4	$+3V_{dc}$
3	S1, S2, D3, D4	S3, S4,D1,D2	Q1,Q2	Q3,Q4	$+2V_{dc}$
4	S1, D2, D3,D4	S2, S3, S4,D1	Q1,Q2	Q3,Q4	$+1V_{dc}$
5	D1, D2, D3,D4	S1, S2, S3,S4	Q1,Q2	Q3,Q4	0
6	S1, D2, D3,D4	S2, S3, S4,D1	Q3,Q4	Q1,Q2	$-1V_{dc}$
7	S1, S2, D3,D4	S3, S4,D1,D2	Q3,Q4	Q1,Q2	$-2V_{dc}$
8	S1, S2, S3, D4	S4,D1,D2,D3	Q3,Q4	Q1,Q2	$-3V_{dc}$
9	S1, S2, S3, S4	D1,D2,D3,D4	Q3,Q4	Q1,Q2	$-4V_{dc}$

Table: 1 Switching Patterns for 9 levels MC-MLI

From the above table, it is observed that for each voltage level, among the paralleled switches only one switch is switched ON. The input DC voltage is converted into a stepped DC voltage, by the multi conversion cell, which is further processed by the H Bridge and outputted as a stepped or approximately sinusoidal AC waveform. In the H Bridge, during the positive cycle, only the switches Q1 and Q3 are switched on. And during the negative half cycle, only the switches Q2 and Q4 are switched on.

The S number of DC sources or stages and the associated number output level can be calculated by using the equation as follows,

$N_{level} = 2S+1$ …………………………………………………….. (1)

For an example, if S=3, the output wave form will have seven levels (±3Vdc, ±2Vdc, ±1Vdc and 0). Similarly voltage on each stage can be calculated by using the equation as given,

$A_i = 1\ V_{dc}\ (1, 2, 3,)$ ……………………………………………….. (2)

The main advantage of proposed modified cascaded multilevel inverter is seven levels with only use of seven switches. For an example, if S=3, the output wave form will have seven levels (±3V_{dc}, ±2V_{dc}, ±1V_{dc} and 0). The number switches used in this topology is given by the equation as follows

$N_{Switch} = 2S+ 4$ ………………………………………………….……….. (3)

III. MULTIPLE CARRIER PULSE WIDTH MODULATION TECHNIQUES

In this PWM technique, more than one carrier wave which be either triangular or saw tooth wave form can be used. This paper focuses on various strategies.utilising more than one triangular wave as carrier and the reference wave is sinusoidal. Though there are many carrier wave arrangements, in this paper, the following four arrangements have been carried out. THD and V_{rms} values for these four strategies for various modulation indexes are compared.

1. Phase disposition PWM strategy.
2. Phase Opposition Disposition PWM strategy.
3. Alternate Phase Opposition Disposition PWM strategy
4. Phase Shift PWM strategy.

In these Multicarrier PWM schemes, several triangular carrier waves are compared with the single Sinusoidal reference wave. The number of carriers required to produce N level output is (m-1) where m is the number of carrier waveforms. The single sinusoidal reference waveform has peak to peak amplitude of A_m and a frequency f_m. The multiple triangular carrier waves are having same peak to peak amplitude A_c and same frequency $f_{c.}$ The single sinusoidal reference signal is continuously compared with all the carrier waveforms. A pulse is generated, whenever the single sinusoidal reference signal is greater than the carrier signal. The frequency ratio m_f is as follows: f_c / f_m

3.1. Phase Disposition PWM strategy (PDPWM)

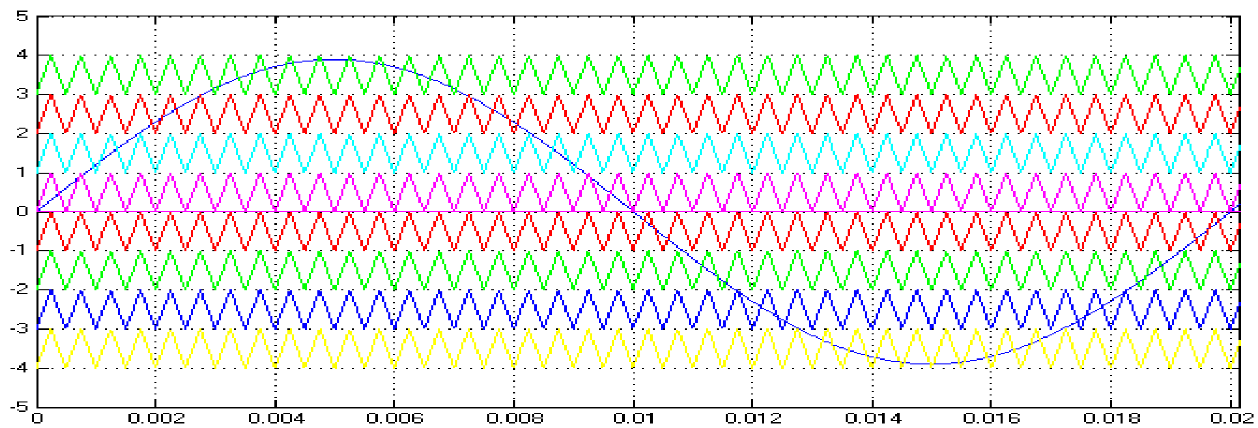

Figure 2: Carrier arrangement for Phase Disposition PWM strategy

The above fig. 2 shows, Phase Disposition PWM strategy (PDPWM), where (m-1) carrier signal with the same frequency f_c and same amplitude A_c are positioned such that the bands they occupy are contiguous. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off.

The below fig: 3 shows Complete Gate signal for 9-level MC-MLI using Phase Disposition PWM strategy
Amplitude of modulation index for PDPWM is

$m_a = 2A_m \ / (m-1) A_c$ …………………… (5)

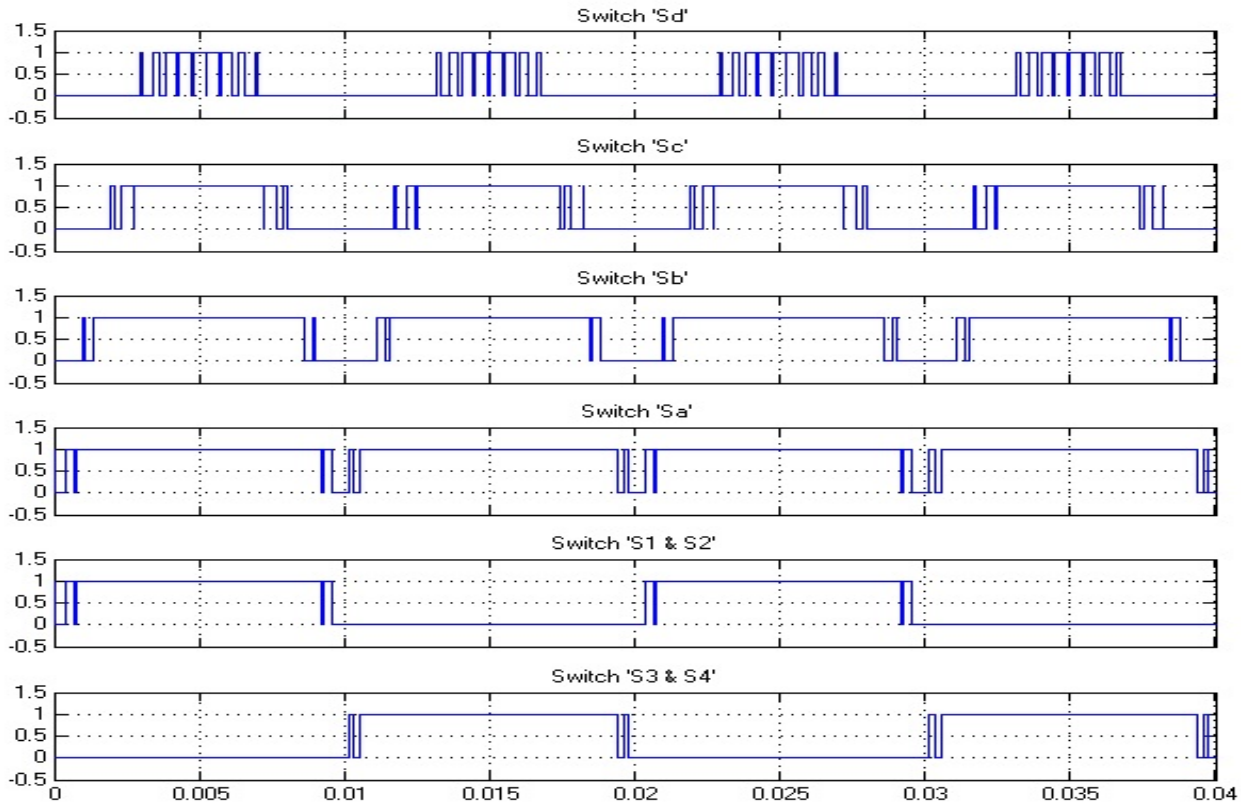

Figure 3 – Complete Gate signal for 9-level MC-MLI using Phase Disposition PWM strategy

3.2. Phase Opposition Disposition PWM strategy (PODPWM)

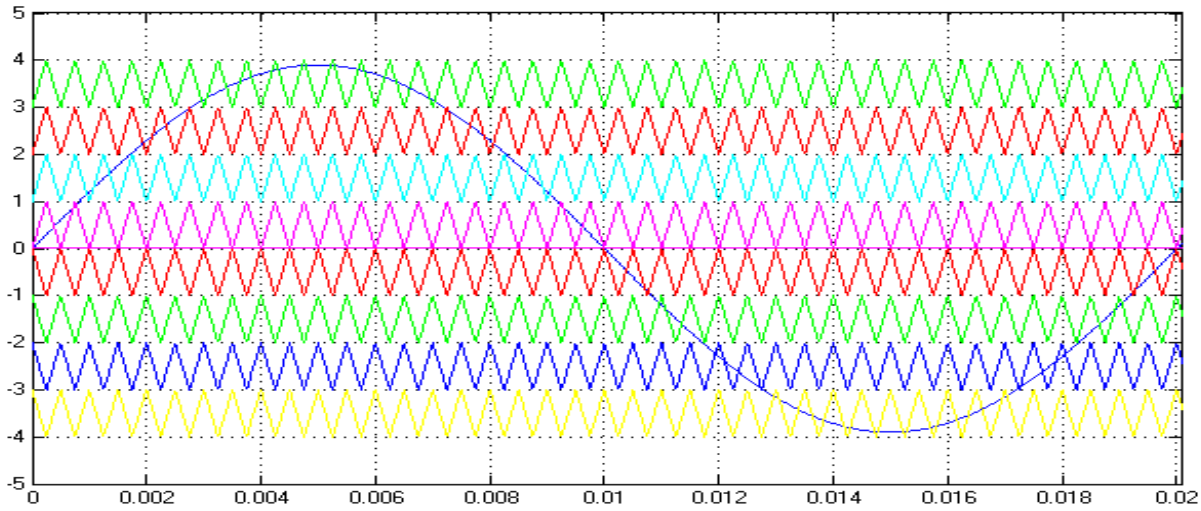

Figure 4: Carrier arrangement for Phase Opposition Disposition PWM strategy

POD PWM strategy is shown in fig.4, where the carrier waveforms, above the zero reference are in phase. The carrier waveforms below are also in phase, but are 180 degrees phase shifted from those above zero. The reference wave form is single sinusoidal. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off. The below fig: 5 shows Complete Gate signal for 9-level MC-MLI using Phase Opposition Disposition PWM strategy.

Amplitude of modulation index for PODPWM is

$$m_a = 2A_m / (m-1)* A_c \quad \text{..... (6)}$$

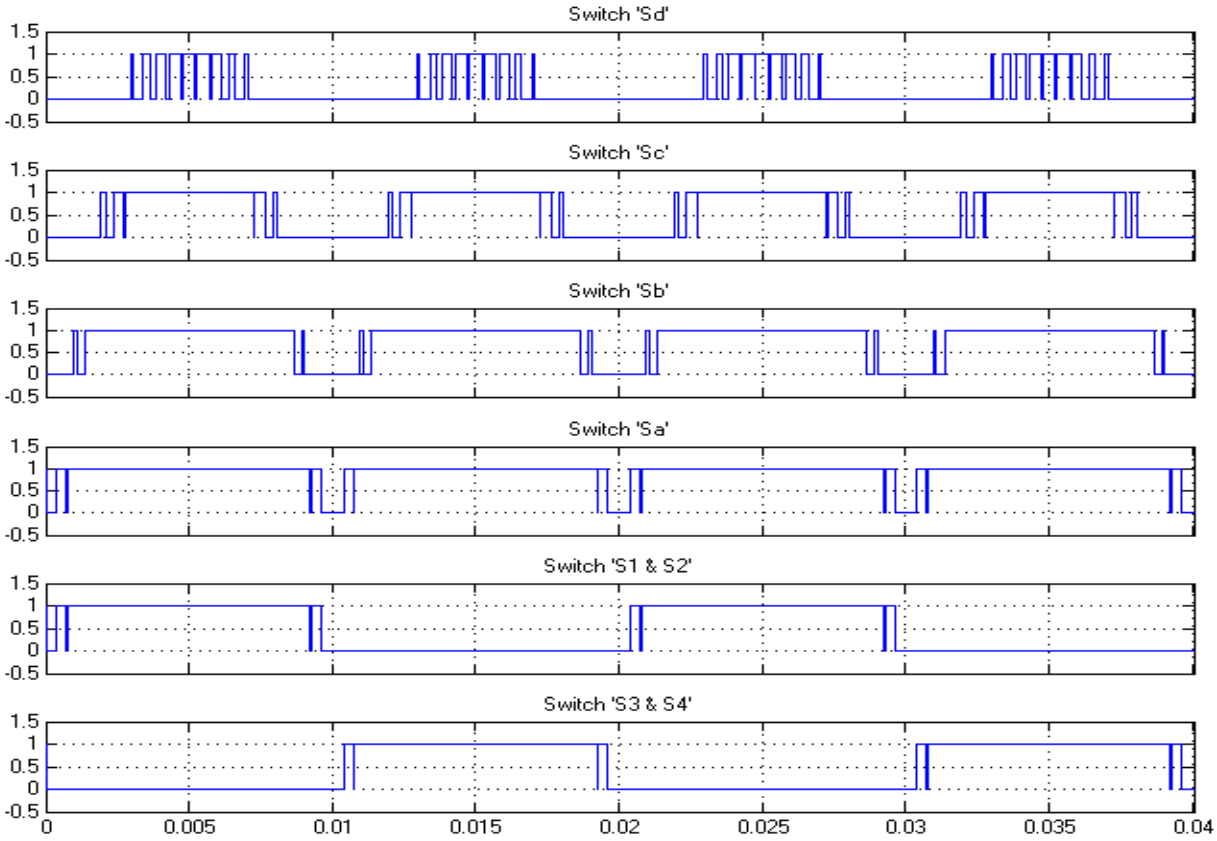

Figure 5: Complete Gate signal for 9-level MC-MLI using Phase Opposition Disposition PWM strategy

3.3. Alternate Phase Opposition Disposition PWM strategy (APODWM)

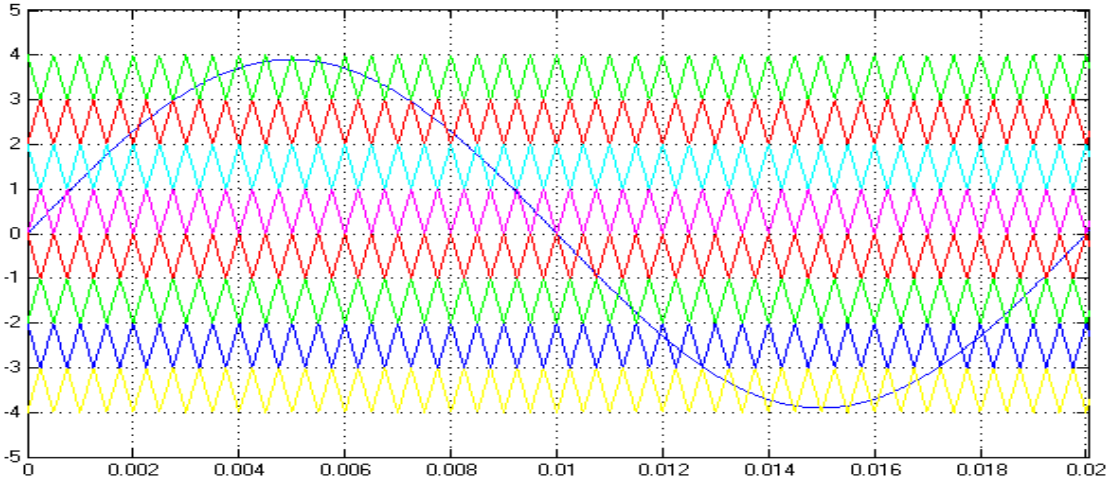

Figure 6: Carrier arrangement for Alternate Phase Opposition Disposition PWM strategy

The above fig. 6 shows APOD strategy where the multiple carriers having same amplitude are phase displaced from each other by 180 degrees alternately. During the continuous comparison, if the reference wave form is more than a carrier waveform, then the active switching device corresponding to that carrier is switched on. Otherwise, that concerned device is switched off. The below fig: 7 shows Complete Gate signal for 9-level MC-MLI using Alternate Phase Opposition Disposition PWM strategy.

Amplitude of modulation index for PODPWM is

$$m_a = 2A_m / (m-1)* A_c \quad \text{.....(7)}$$

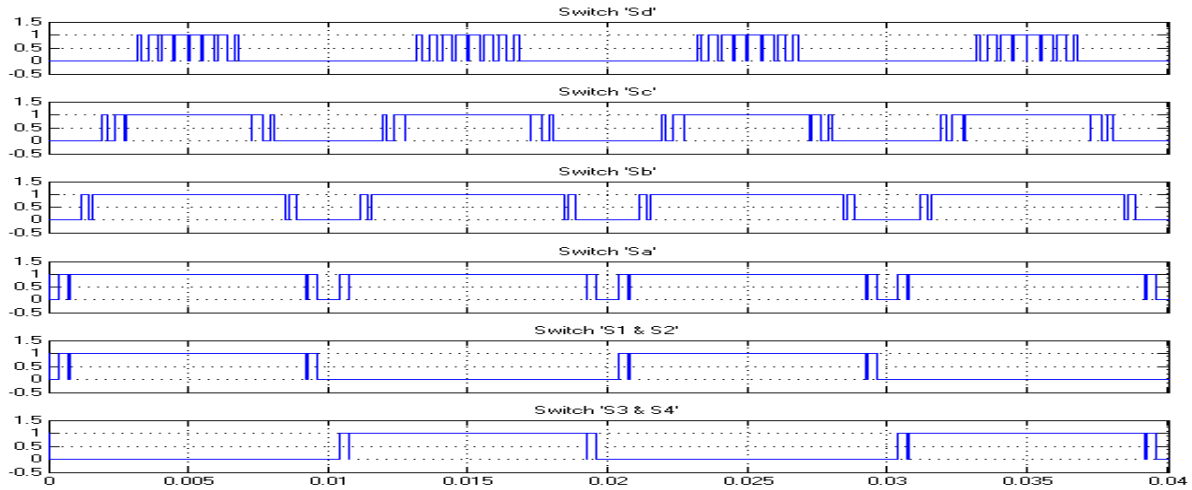

Figure 7: Complete Gate signal for 9-level MC-MLI using Alternate Phase Opposition Disposition PWM strategy

3.4. Phase shift PWM strategy (PSPWM)

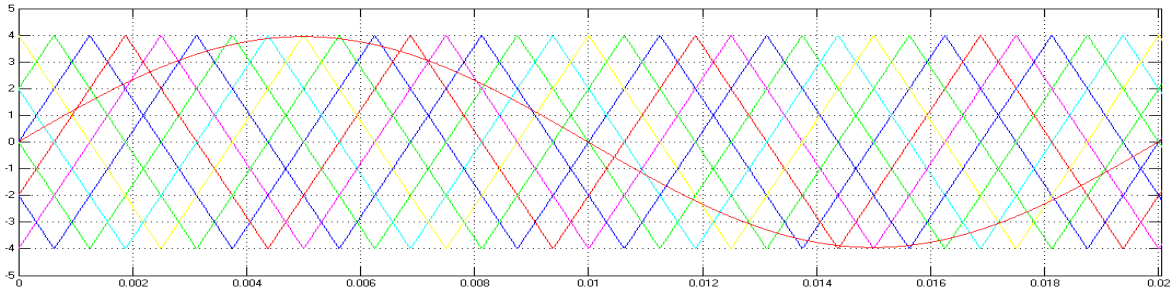

Figure 8: Carrier arrangement for Phase shift PWM strategy

The above fig. 8 shows PSPWM strategy where the multiple carriers having the same amplitude and frequency which are shifted to one another by certain degrees decided by the No. of levels. Thus for nine level output, 8 triangular carrier waves which are phase shifted by 45 degrees is utilized .The reference waveform is single sinusoidal (i) for odd m_f the waveforms have odd symmetry resulting in even and odd harmonics and (ii) for even m_f , PSPWM waves have quarter wave symmetry resulting in odd harmonics only. Amplitude of modulation index for PSPWM is

$$m_a = A_m / (A_c /2). \quad \text{.....(4)}$$

The below fig.9 shows complete gate signal for 9-level MC-MLI using Phase shift PWM strategy

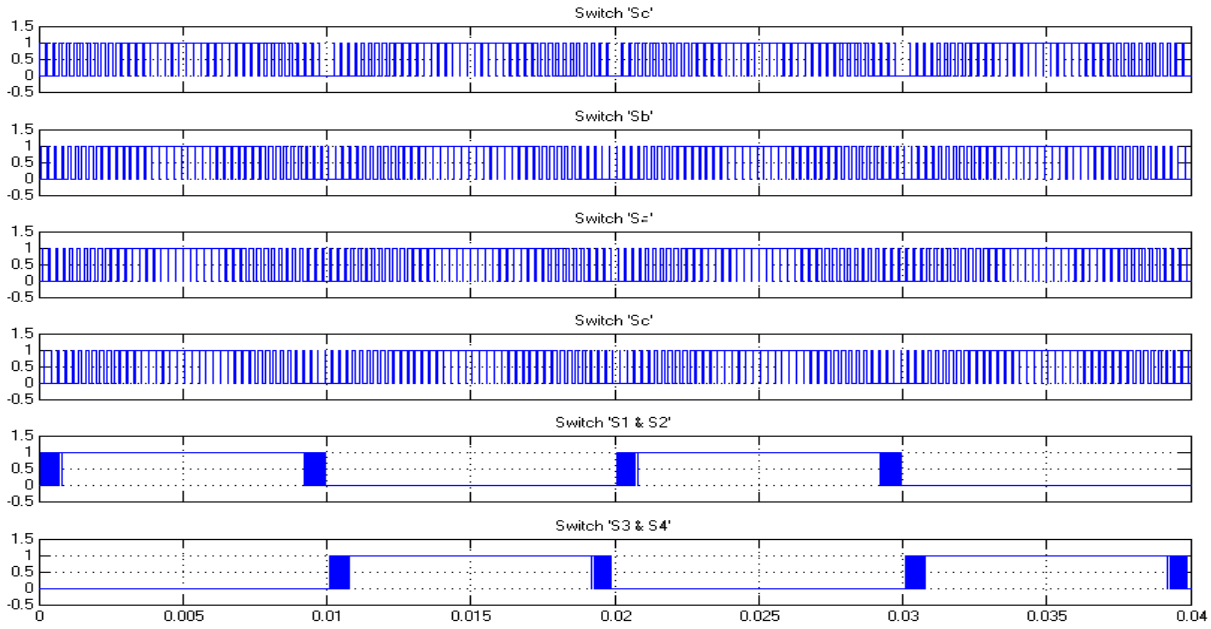

Figure: 9 – Complete Gate signal for 9-level MC-MLI using Phase shift PWM strategy

IV. SIMULATION RESULTS

The fig. 6 shown below is the simulink model of the 9 –level Modified cascaded H Bridge Multilevel inverter using power system block set. The following parameter values are used for simulation: V_1 =100v, V_2 =100v, V_3 = 100v, V_4= 100v f_c =2000 Hz and fm=50Hz .Gating signals for Phase shifted carrier wave arrangement and three different, level shifted carrier wave arrangements are simulated for 9 levels MC MLI. Simulations are done for various values of m_a and the corresponding THD% are observed using FFT block and listed in Table 2 The $V_{r\,ms}$ (fundamental) of the output voltage for various values of m_a and the corresponding Voltages are listed in Table3.

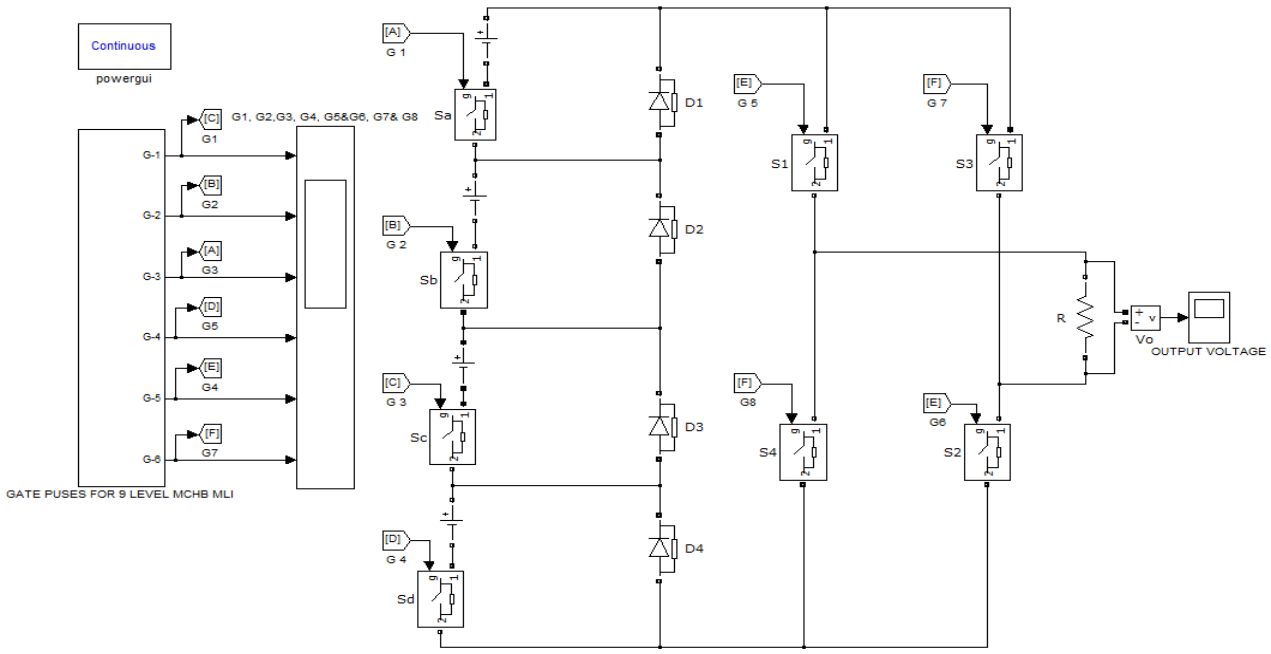

Figure 8: Simulink Model of the 9 level - Modified Cascaded Multilevel Inverter-MC-MLI

Table 2: THD comparison

M_a	PD PWM	POD PWM	APOD PWM	PS PWM
1	13.63	13.48	14.04	13.66
0.9	16.74	16.72	16.89	16.65
0.8	17.1	16.85	17.02	17.14

Table 3: V_{rms} comparison

M_a	PD PWM	POD PWM	APOD PWM	PS PWM
1	399	397.8	397	399
0.9	358.6	356.6	356.7	358.7
0.8	318.4	316.5	316.8	318.3

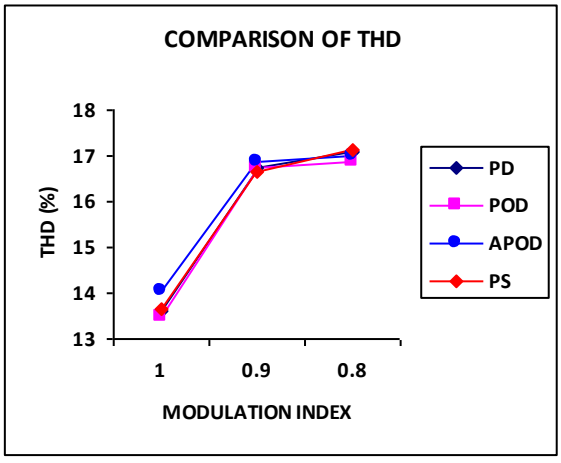

Figure 9 Comparison of THD

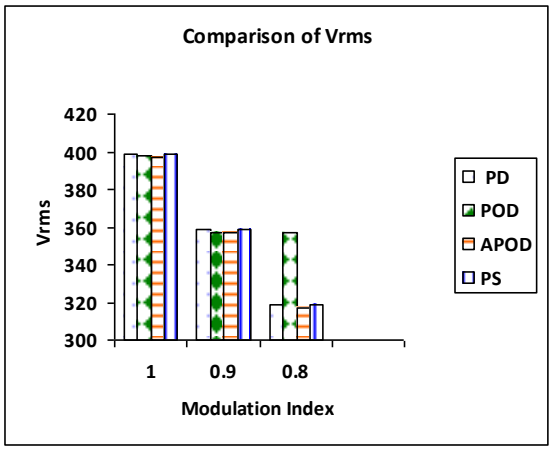

Figure 10 Comparison of V_{rms}

The Simulated 9-level Output Voltage waveform of MC-MLI using PDPWM Strategy is shown in fig. 11 and Fig. 12 shows the FFT plot of 9-level MC-MLI Using PDPWM using PDPWM Strategy. The Simulated 9-level Output Voltage waveform of MC-MLI using PODPWM Strategy is shown in fig 13 and Fig: 14 shows the FFT plot of 9-level MC-MLI using PDPWM Using PODPWM Strategy. The Simulated 9-level Output Voltage waveform of MC-MLI using APODPWM Strategy is shown in fig 15 and Figure: 16 shows the FFT plot of 9-level MC-MLI Using APDPWM using PODPWM Strategy. The Simulated 9-level Output Voltage waveform of MC-MLI using PSPWM Strategy is shown in fig 17 and Fig: 18 shows the FFT plot of 9-level MC-MLI Using PDPWM using PSPWM Strategy.

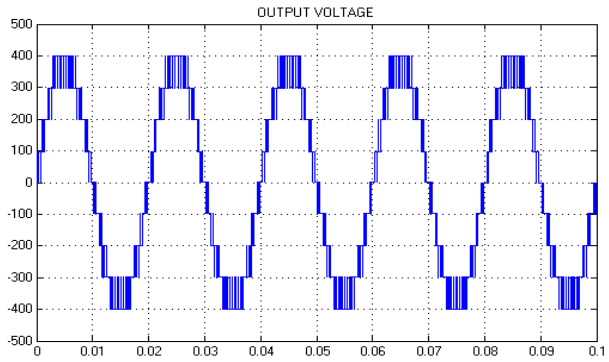

Figure 11: Simulated 9-level Output Voltage waveform of MC-MLI Using PDPWM Strategy

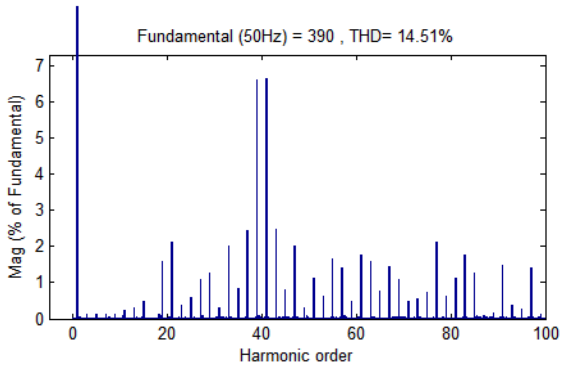

Figure 12: FFT plot of 9-level Output Voltage waveform MC-MLI Using PDPWM Strategy

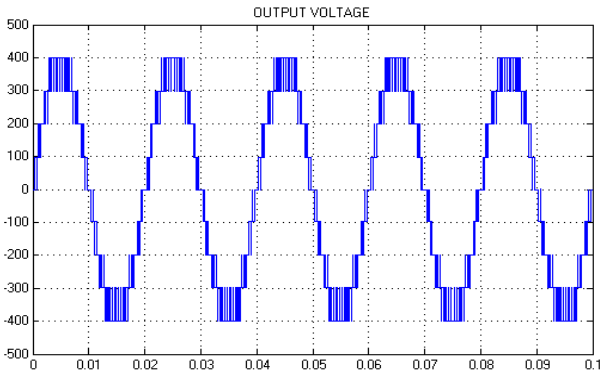

Figure 13: Simulated 9-level Output Voltage waveform of MC-MLI Using PODPWM Strategy

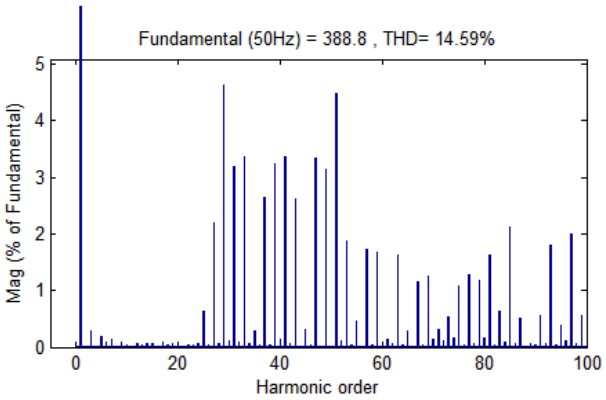

Figure 14: FFT plot of 9-level MC-MLI Using PODPWM Strategy

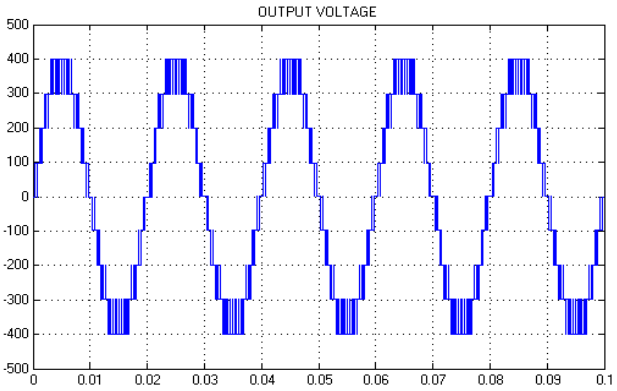

Figure 15: Simulated 9-level Output Voltage waveform of MC-MLI Using APODPWM Strategy

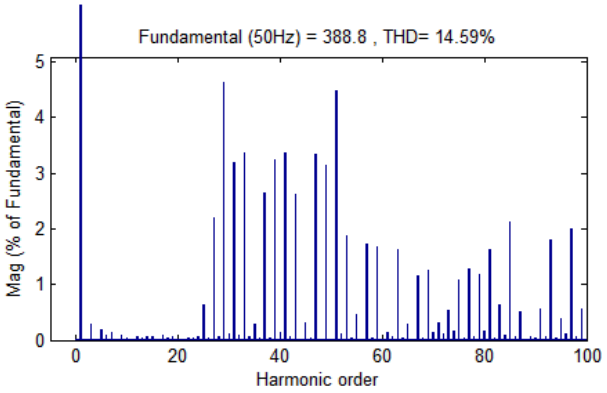

Figure 16: FFT plot of 9-level MC-MLI Using APODPWM Strategy

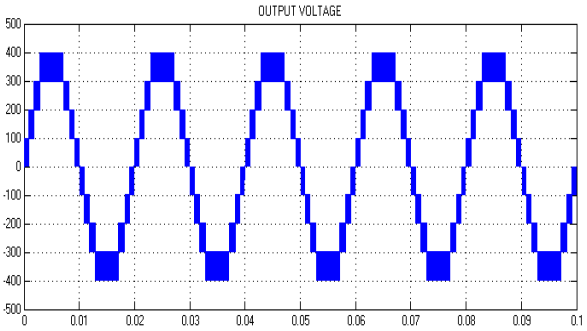

Figure 17: Simulated 9-level Output Voltage waveform of MC-MLI Using PSPWM Strategy

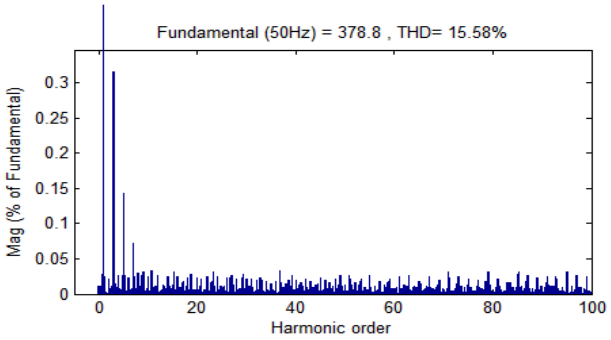

Figure 18: FFT plot of 9-level MC-MLI Using PSPWM Strategy

V. CONCLUSION

Single phase nine levels Modified cascaded multilevel inverter has been analyzed for various multi carrier sinusoidal Pulse Width Modulation strategies. This topology has the credit of having only eight switches with four diodes, instead of 18 switches in the conventional plants, which support reduction in switching losses, cost and circuit complexity.

Performance factors like %THD and V_{RMS} have been measured, and analyzed for Phase shifted carrier wave arrangement and three different, level shifted carrier wave arrangements both applied to the Single phase nine levels Modified cascaded multilevel inverter. The values have been measured for various modulation indexes. It is found that the PDPWM strategy provides appreciable %THD and acceptable V_{RMS}. In addition, it is also observed that it has less number of dominant harmonics than the other strategies.

REFERENCES

[1] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind.Electron. Mag., vol. 2, no. 2, pp. 28–39, Jun. 2008.*

[2] Z.Du, L.m.Tolbert, J.N.Chiasson, and B.Opineci, "A cascaded multilevel inverter using a single dc power source", in *Proc. IEEE APEC, pp.426-430, 2006.*

[3] Fang Zheng Peng "A Generalized Multilevel Inverter Topology with Self Voltage Balancing", *IEEE Trans. Ind .Appl., Vol.37, No.2, March/April 2001.*

[4] J. I. Leon, R. Portillo, S. Vazquez, J. J. Padilla, L. G. Franquelo, and J.M. Carrasco, "Simple unified approach to develop a time-domain modulation strategy for single-phase multilevel converters," *IEEE Trans.Ind. Electron., vol. 55, no. 9, pp. 3239–3248, Sep. 2008.*

[5] Y. Li and B. Wu, "A novel dc voltage detection technique in the chb inverter-based statcom," *IEEE Trans. Power Del., vol. 23, no. 3, pp.1613–1619, Jul. 2008.*

[6] J. Rodriguez, J. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron, vol.49, no. 4, pp. 724–738, Aug. 2002.*

[7] Ebrahim Babaei "A Cascaded Multilevel converter Topology With Reduced Number of Switches*", IEEE Trans. Power Electron vol.23,no.6, Nov 2008.*

[8] Rokan Ali Ahmed, S. Mekhilef, Hew Wooi Ping, ''New multilevel inverter topology with reduced number of switches'',*Proceedings of the 14th International Middle East Power Systems Conference (MEPCON'10), Cairo University, Egypt, December 19-21, 2010, Paper ID 236.*