

Performance Analysis of Three Phase Cascaded H-Bridge Multi Level Inverter for Voltage Sag and Voltage Swell Conditions

¹Ganesh Pashikanti, ²Sudha Dasari

¹P.G Scholar, ²Assistant Professor, ^{1,2}Vathsalya Institute of Science and Technology

ABSTRACT: A Multilevel Inverter is a power electronic device built to synthesize a desired AC voltage from several levels of DC voltages. Nowadays, modern industrial devices are mostly based on electronic devices such as programmable logic controllers and electronic drives. The electronic devices are very sensitive to disturbances and become less tolerant to power quality problems such as under voltage and over voltage conditions. In general under voltage and over voltage conditions will occur more at source side. In this paper a closed loop Control system is designed using PI controller in order to maintain load voltage constant for under voltage and Over voltage conditions. The triggering pulses to Cascaded H-Bridge (CHB) MLI is given using multi carrier phase shifted technique and MATLAB simulations have been carried out.

Keywords: Multilevel Inverter (MLI), Carrier based Pulse Width Modulation (PWM), Phase Shifted (PS), Under Voltage, Over Voltage.

I. INTRODUCTION

Multilevel inverters have gained more attention in high power applications because it has got many advantages [1-4]. It can realize high voltage and high power output by using semiconductor switches without the use of transformer and dynamic voltage balance circuits. When the number of output levels increase, harmonic content in the output voltage and current as well as electromagnetic interference decrease. The basic concept of a Multilevel inverter is to achieve high power by using a series of power semiconductor switches with several lower dc voltage sources to perform the power conversion by synthesizing a staircase voltage waveform [1,5]. To obtain a low distortion output voltage nearly sinusoidal, a triggering signal should be generated to control the switching frequency of each power semiconductor switch. A three phase Cascaded H-bridge Multi (five) Level Inverter has been taken. Fig.1 shows a three-phase five-level Cascaded H-Bridge MLI. It requires a total of six dc voltage sources.

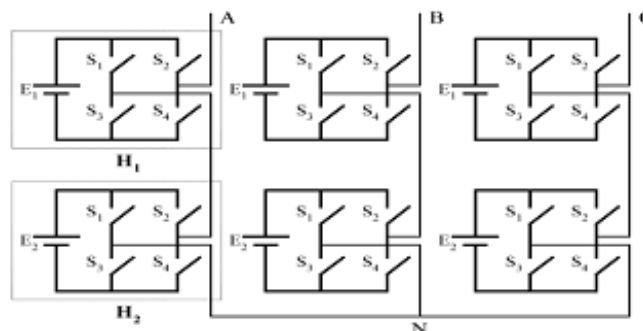


Fig.1 Conventional Three Phase 5-Level Cascaded H-Bridge Multilevel Inverter.

As Multilevel inverter is made up of semiconductor switches which are very sensitive to disturbances and become less tolerant to power quality problems such as under voltage and over voltage conditions this paper investigates an approach of designing a closed control system using PI controller to maintain load voltage constant for under voltage and Over voltage conditions.

II. CONTROL TECHNIQUES OF MLI

There are different control techniques available for a CHB MLI [13, 15] as shown in Fig.2 Among all those techniques, PWM control technique which produces less total harmonic distortion (THD) values is most preferable. In PWM technique also, sinusoidal PWM is used for generating triggering pulses to MLI. In sinusoidal PWM pure sinusoidal wave as modulating signal and multi carrier signal which is of triangular in shape have been considered [10, 14, 15]. For an m-level MLI, (m-1) carrier signals are required.

2.1 Multi carrier Sinusoidal PWM: For generation of triggering pulses to the MLI, carrier signals can be constructed using various control techniques like APOD, POD, PD, PS, Hybrid and can be modulated using sine wave [6-7]. As phase shifted technique is best suitable for CHMLI, is used in this paper for generation of triggering pulses to CHMLI [7-9]. Multilevel sinusoidal PWM can be classified as shown in Fig.3 [14-19].

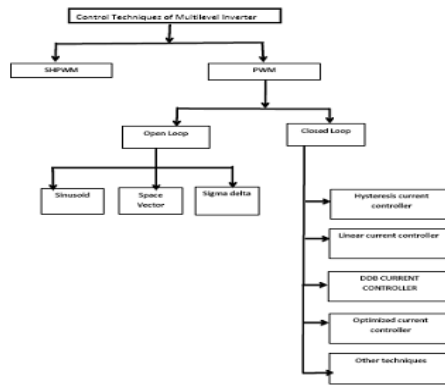


Fig.2 Control Techniques for a Cascaded H-Bridge MLI

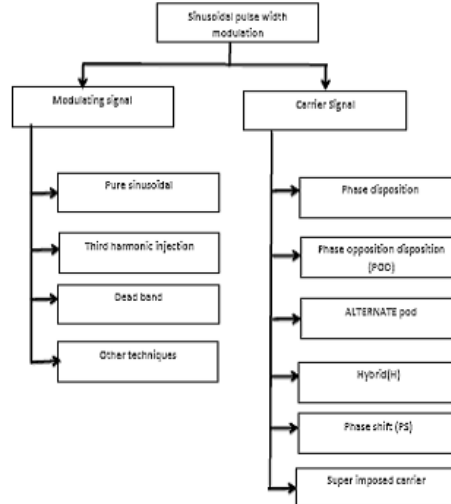


Fig.3 Classification of Sinusoidal PWM

Amplitude Modulation

$$M_a = \frac{A_m}{A_c(m - 1)}$$

Frequency Modulation

$$M_f = \frac{F_c}{F_r}$$

Here A_m = Amplitude of Modulating Wave (Sine)

A_c = Amplitude of Carrier Wave (Triangular)

F_c = Carrier Frequency

F_r = Reference Frequency

2.2 Modes of Operation: For generating triggering pulses, sine wave (reference) can be modulated with phase shifted carrier technique in bipolar and uni polar mode. As in this paper bi polar mode of operation is used, carrier signals arrangement using PS control technique in bipolar mode of operation is shown in Fig.4 In bi polar mode, four carrier signals of triangular in nature and one sine wave are used [6,15].

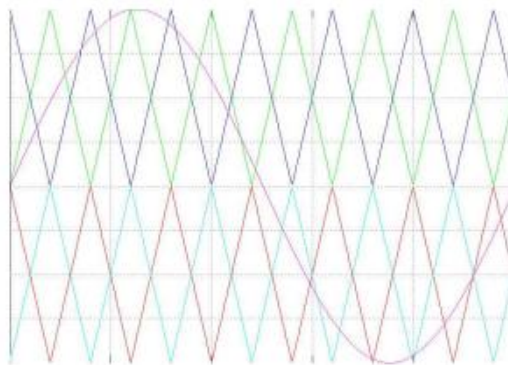


Fig.4 Carrier Arrangement for Bi-Polar Mode in PS Technique

For a five level MLI, in PS Technique the carrier signals are Phase Shifted by 90 Degrees $\frac{360}{(m-1)}$

III. POWER QUALITIES

Power Quality is the concept of powering and grounding sensitive equipment in a matter that is suitable to the operation of that equipment according to IEEE Std 1100. Power quality is mainly concerned with deviations of the voltage from its ideal waveform (voltage quality) and deviations of the current from its ideal waveform (current quality). Power quality phenomena can be divided into two types; they are 1) Variations 2) Events.

Voltage and Current variations are relatively small deviations of voltage or current characteristics around their nominal or ideal values. The two basic examples are voltage magnitude and frequency. Events are phenomena which only happen every once in a while. An interruption of the supply voltage [IEEE Std.1159] is the best-known example.

3.1 Under Voltage: Under voltages of various duration are known under different names. Short duration under voltages are called “voltage sags” or “voltage dips”. Long duration under voltage is normally simply referred to as “under voltage”. Voltage sag is a reduction in the supply voltage magnitude followed by a voltage recovery after a Short period of time. Reduction of voltage magnitude of short duration can be called as voltage sag. For the IEEE voltage drop is only a sag if the during sag voltage is between 10% and 90% of the nominal voltage. Voltage sags are mostly caused by short circuit faults in the system and by starting of large motors. Voltage sag is generally characterized by depth and duration. The depth of the sag depends on the system impedance, fault.

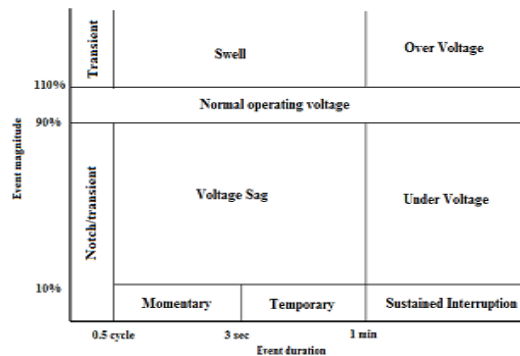


Fig.5 Voltage Magnitude Events as Used in IEEE Std. 1159-1995

Distance, system characteristics (grounded or ungrounded) and fault resistance. The duration of the sag depends on the time taken by the circuit protection to clear the fault.

3.2 Over Voltage: Just like with under voltage, overvoltage events are given different names based on their duration. Over voltages of very short duration, and high magnitude, are called “Transient Over Voltages”, “Voltage Spikes,” or sometimes “Voltage Surges.” When the output voltage exceeds 110% of the rated voltage & with duration More than 1 minute is called Over Voltage. Long and Short over voltages originate from, lightning strokes, switching operations, sudden load reduction, single phase short circuits, and nonlinearities. A resonance between the nonlinear magnetizing reactance of a transformer and a capacitance (either in the form of a capacitor bank or the capacitance of an underground cable) can lead to a large overvoltage of long duration. This phenomenon is called Ferro resonance, and it can lead to serious damage to power system.

In this paper the three phase ac voltage supply is taken directly and is given to three dc voltage is given as a input to Cascaded H-bridge 5 level Multilevel Inverter and the output of MLI is given to load.

In closed loop control the supply voltages and load voltages are both compared and error value is given to PI Controller. Output of PI controller is imposed on the phase shifted carrier phase controlled rectifier which converts ac supply to controlled pulsated dc voltage and this is given to low pass filter. Low pass filter is a device which converts pulsated dc voltage to pure dc voltage and this pure

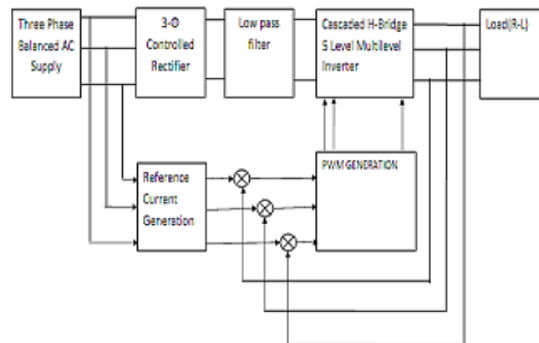


Fig.6 Closed Loop Block Diagram

So as to get pulses. These pulses are given to MLI for each phase. Here we are using three PI controllers for three phases MLI. The desired voltage at the load bus is maintained at 1pu.

3.3 PI Controller: To regulate the load-bus voltage, a PI controller is employed that contains a feedback signal derived from the voltage at the load bus V.

$$Z_c = K_p e + K_i \int edt$$

Where,

K_p = Proportional Constant

K_i = Integral Constant

E = Error Value

3.4 Design of Filter: LC Filter is the combination of two filters & provides a lower ripple than which is possible with either L or C alone. As it is known, in an inductor filter, ripple increases with RL but decreases in a capacitor filter. So the combination of both L and C filter lowers the ripple content. Here,

$$C = \frac{10}{2 * w(R_L^2 + (2W_L L_L)^2)}$$

$$VRF = \frac{\sqrt{2}}{3} \frac{1}{(2 * W)^2 LC - 1}$$

Where VRF is Voltage Ripple Factor

IV. SIMULATION RESULTS

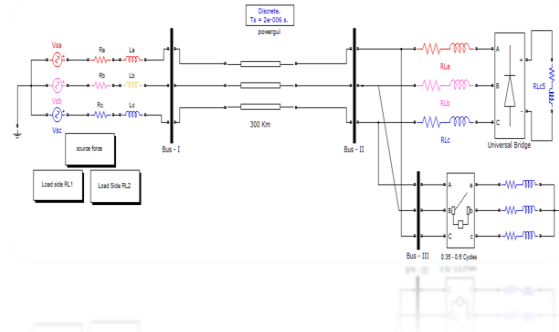


Fig.7 Simulink Diagram of Open Loop System for Voltage Sag

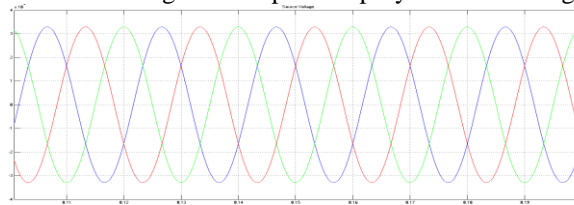


Fig.8 Supply Voltages

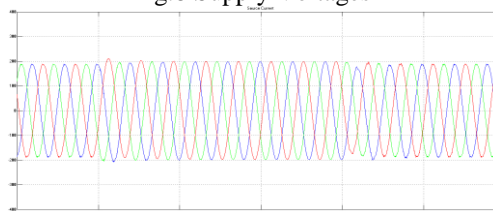


Fig.9 Supply Current

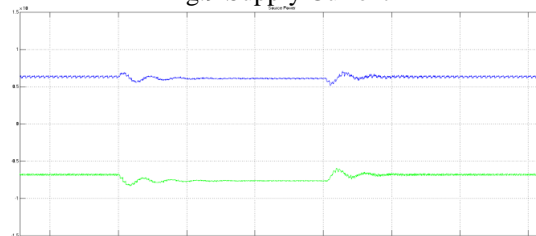


Fig.10 Source Active Power & Reactive Power

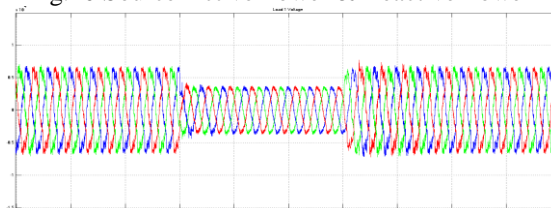


Fig.11 Load Voltage

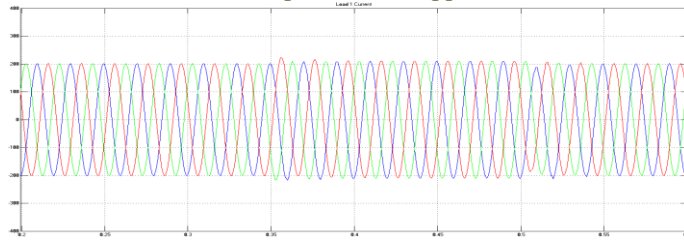


Fig.12 Load Current

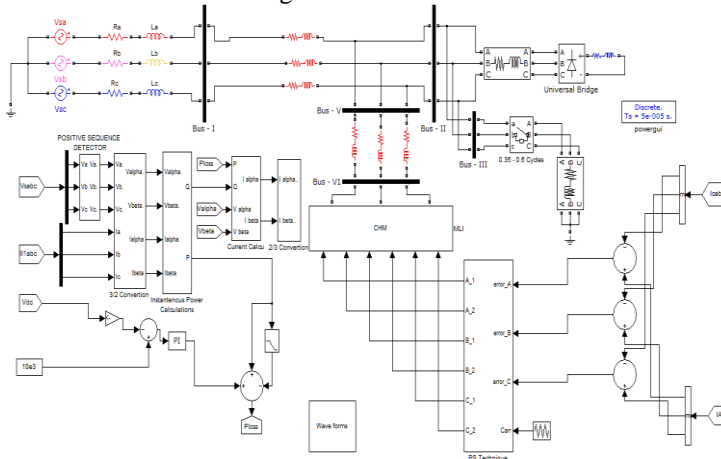


Fig.13 Voltage Sag Closed Loop

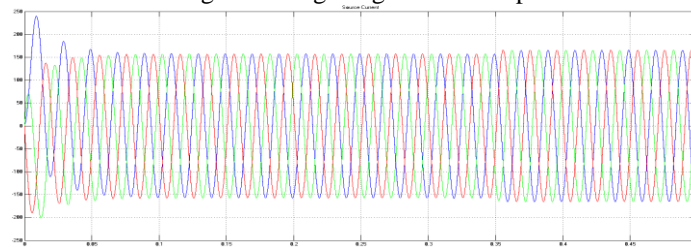


Fig.14 Closed loop Current

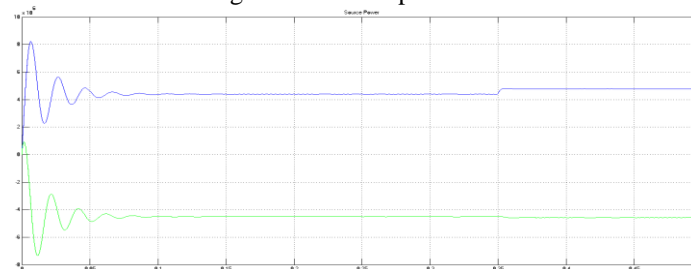


Fig.15 Active & Reactive Powers

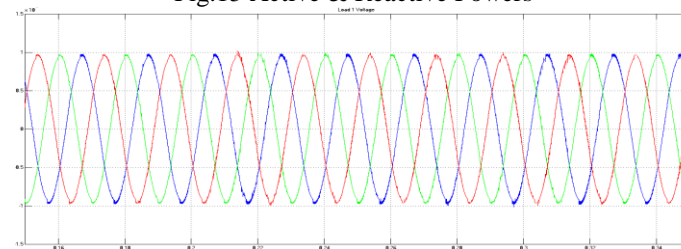


Fig.16 Load Voltage

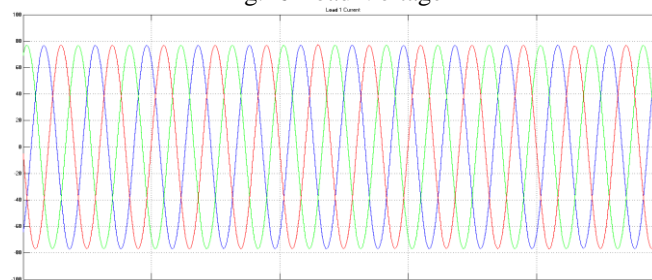


Fig.17 Load Current

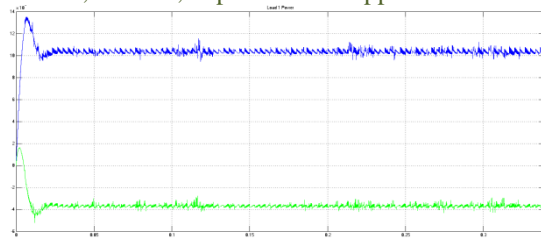


Fig.18 Active & Reactive Powers at Load Side

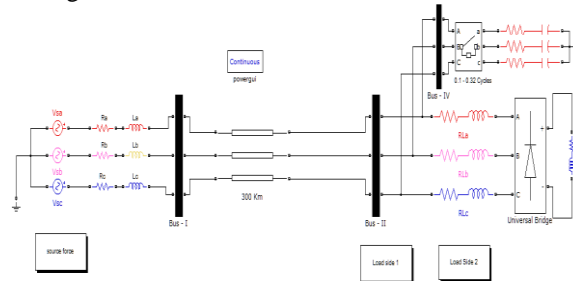


Fig.19 Voltage Swell Open Loop

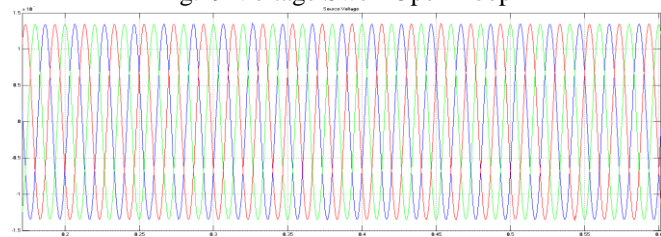


Fig.20 Source Voltage

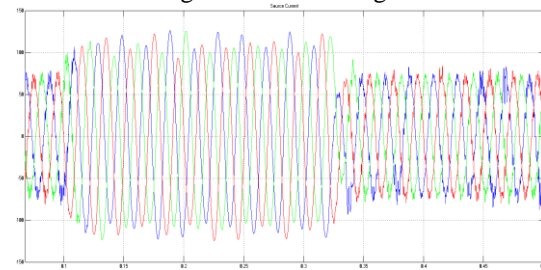


Fig.21 Source Current

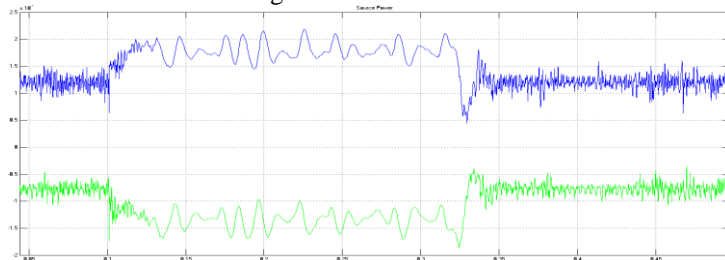


Fig.22 Source Active & Reactive Power

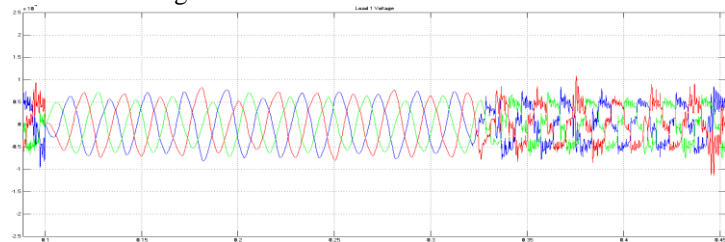


Fig.23 Load Voltage

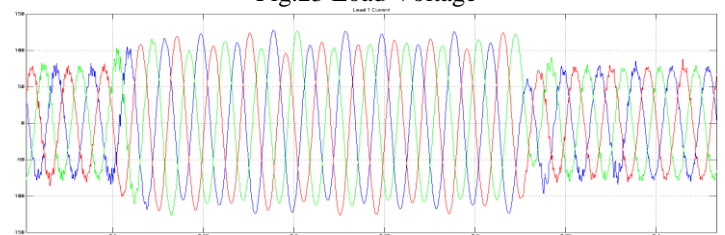


Fig.24 Load Current

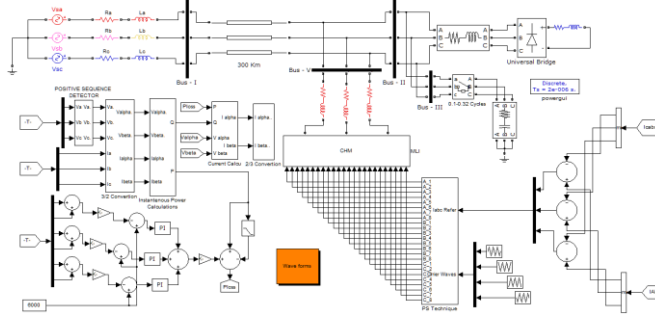


Fig.25 Voltage Swell Closed Loop

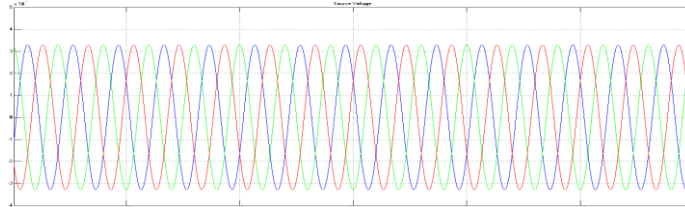


Fig.26 Source Voltage

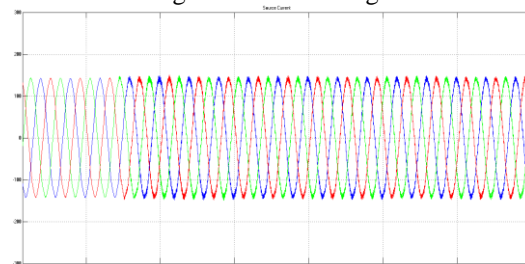


Fig.27 Source Current

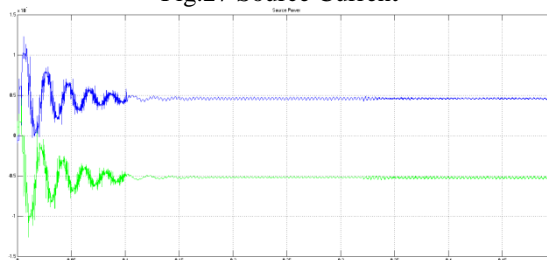


Fig.28 Source Active & Reactive Power

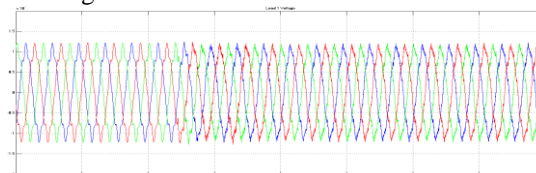


Fig.29 Load Voltage

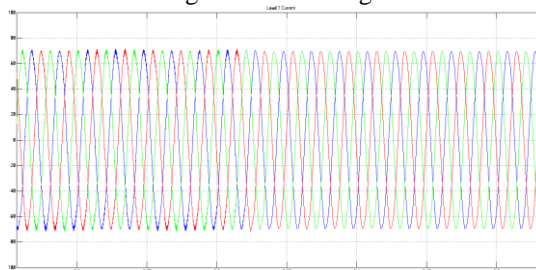


Fig.30 Load Current

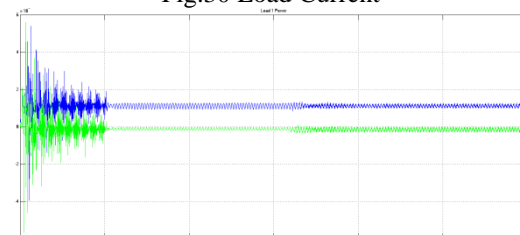


Fig.31 Load Active & Reactive Power

V. CONCLUSION

In this paper three phase Cascaded H-Bridge Multilevel inverter is simulated using multi carrier Phase Shifted technique and analyzed for Under Voltage and Over Voltage conditions. In the open loop system under voltage and over voltages were introduced at the supply side and the changes in the load voltages are analyzed from the observed waveform. In the closed loop system, with the help of PI Controller the load voltage is maintained constant during under voltage and over voltage conditions which can be observed from the above simulated figures.

REFERENCES

- [1] D. A. Rendusara, E. Cengelci, P. N. Enjeti, V. R. Stefanovic, and J.W. Gray. "Analysis of common mode voltage—neutral shift in medium voltage PWM adjustable Speed drive (MV-ASD) systems," IEEE Trans. Power Electronics, vol.15, no.6, pp.1124-1133, Nov. 2000.
- [2] Fang Zheng Peng, Jih-Sheng Lai, and Rodriguez J. "Multilevel inverters: A survey Of topologies, controls, and applications", Industrial Electronics, IEEE Transactions, Vol. 49, issue: 4, pp. 724-738, Aug 2002.
- [3] Holmes, D.G, McGrath, B.P. "Multi carrier PWM strategies for multilevel inverters" Industrial Electronics, IEEE Transactions, Vol. 49, issue: 4, pp.858-867, Aug 2002.
- [4] Leon M. Tolbert, Fang Zheng Peng, Tim Cunyngham, and John N.Chiaasson. "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles" IEEE Trans. Industrial Electronics, vol.49, no.5, pp.1058- 1064, Oct. 2002.
- [5] Yan Deng, Hongyan Wang, Chao Zhang, Lei Hu and Xiangning He, "Multilevel PWM Methods Based On Control Degrees of Freedom Combination And Its Theoretical Analysis", IEEE IAS 2005 Conference record no.:0-7803-9208-6/05, pp.1692 – 1699, 2005.
- [6] Alan Joseph, et al. "A 24-pulse rectifier cascaded multilevel inverter with minimum number of transformer windings," IEEE Fourtieth IAS Annual Meeting ,vol.1, Oct. 2005, pp.115-120.
- [7] J. Rodriguez, B. Wu, S. Bernet, J. Pontt, and S. Kouro, "Multilevel voltage source-converter topologies for industrial medium-voltage drives," IEEE Trans. Ind.Electron., vol. 54, no. 6, pp. 2930–2945, Dec. 2007.
- [8] S. Khomfoi, L. M. Tolbert, "Multilevel Power Converters," Power Electronics Handbook, 2nd Edition Elsevier, 2007, ISBN 978-0-12- 088479-7, Chapter 17, pp.451-482.
- [9] Samir Kouro, Student Member, IEEE, Pablo Lezana, Member, IEEE, Mauricio Angulo, and Jose Rodriguez, Senior Member, IEEE Transactions on Power Electronics, Vol. 23, No. 1, January 2008 "Multicarrier PWM With DC-Link Ripple Feed forward Compensa. for Multilevel Inverters".
- [10] Panagiotis Panagis, Fotis Stergiopoulos, Pantelis Marabeas and Stefanos Manias "Comparison of State of the Art Multilevel Inverters". 978-1-4244-1668-4/08/2008 IEEE
- [11] Ge Baoming, and Fang Zheng Peng, "An Effective Control Technique for Medium-Voltage High Power Induction Motor Drives", 978-1-4244-1766-7/08-2008 IEEE.
- [12] "A 5-Level Cascaded Hybrid Multilevel Inverter for Interfacing with Renewable Energy Resources" Surin Khomfoi1, Chatrchai Aimsaard 978-1-4244-3388- 9/09/2009 IEEE
- [13] "Optimized Hybrid Phase Disposition PWM Control Method for Multilevel Inverter" C. Govindaraju and Dr. K. Baskaran Internatio. Journal of Recent Trends in Engineering, Vol 1, No. 3, May 2009 49
- [14] "A modular power electronic transformer based on a cascaded H-bridge multilevel converter" H. Iman-Einia, b, Sh. Farhangia, J.-L. Schanenb, M. Khakbazan-Fardc H. Iman- Eini et al. / Electric Power Systems Research 79 (2009) 1625–1637.