Impact of Hybrid Pass-Transistor Logic (HPTL) on Power, Delay and Area in VLSI Design

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Abstract: *Power reduction is a serious concern now days. As the MOS devices are wide spread, there is high need for circuits which consume less power, mainly for portable devices which run on batteries, like Laptops and hand-held computers. The Pass-Transistor Logic (PTL) is a better way to implement circuits designed for low power applications.*

Keywords: *Pass-Transistor Logic (PTL), MOS devices, low power applications.*

I. Introduction

The power consumption in a circuit can be decreased by reducing:
- Switching activity in the circuit
- Switching capacitance of each node
- Supply voltage
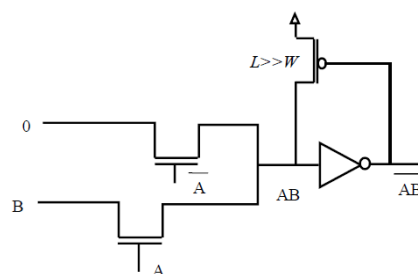- Short-Circuit Current

Let's look at a PTL design:

Fig 1 shows the PTL design

This kind of PTL design is called the Single-Rail Pass-Transistor Logic (also called LEAP). Here, a basic AND/NAND function is implemented. The PMOS transistor which is connected opposite to the output inverter is called a bleeder transistor, which is used to pull the weak '1' arriving at the input of the inverter.

Now, the advantage of PTL comes from the fact that it is best suitable to implement all the above power reduction techniques:

1. Switching activity in the circuit can be reduced by eliminating the glitches. This can be done by controlling the delays of each pass transistor (controlling the widths and lengths).
2. Switching capacitance of a node in the PTL will be less when compared to a node in the CMOS design. Due to the smaller size of the transistors in PTL implementation.
   - The lengths of the transistors should be as small as possible, because increased lengths result in more IR_{drop} across the transistor.
   - The widths of transistors also should be small. It's because the improvement seen in the switching of that transistor will be subdued by the delay caused in the input, which is driving that wider gate.
3. Like the CMOS technologies, the supply voltage can be reduced at the cost of some increase in delay of the circuit.
4. There are fewer ground connections (only at the inverters) means fewer V_{DD} to GND connections during switching. So theoretically PTL implementation should draw least amount of short circuit power.

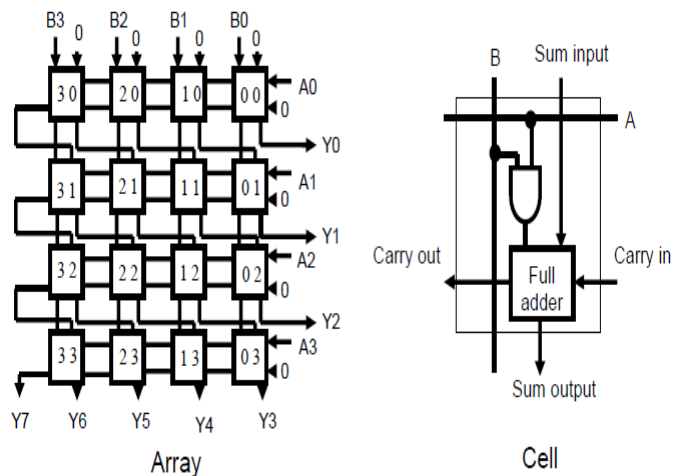## II. The Present Project

Fig 2 shows the Present Project Array & Cells structure

Steps followed to create the final 32x32 bit CMOS design:
1. A full adder is designed at the behavioral level in VHDL.
2. A multi_cell is implemented using the full adder and "and" gate.
3. The 32x32 bit multiplier is designed at the structural level using the 'multi_cell' in VHDL.
4. The generated 32x32 bit multiplier code is simulated in ModelSim to verify its functionality.
5. Then the 32x32 bit multiplier is synthesized using Leonardo for TSMC025 technology.
6. The synthesized model is imported into Design Architect.

The critical path given by Leonardo for my design is:
"Eldo" simulator which is a part of the Anacad&Mentor package is used for simulations at the transistor level.

III. Implementations

There are basically 3 implementations I have manually designed transistor by transistor:
1. Normal PTL single rail design.
2. Transmission gate based design show in fig 3
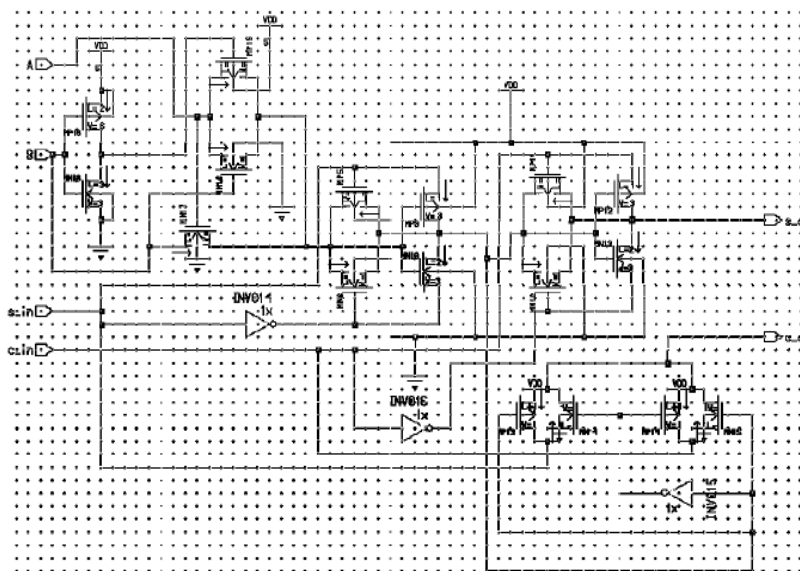3. A new PTL design based on special XOR/XNOR gates)

Fig 3 shows the implementation design pattern

All the implementations are working properly. Actually, I have implemented and simulated a full 4x4 multiplier using the above transmission gate based design. The above design is robust w.r.t loads (has good Delay Vs Load characteristics). The waveforms are looking robust like the CMOS based design with reasonable delays. But, the Eldo is having problems with this implementation (not reporting the static power correctly).

IV. Power Consumption And Delay

Circuit Type	Static Power	Dynamic Power	Delay
CMOS	356.56pW	12.49μW	551ps
PTL	353.36pW	79.24μW	8.45ns
T_x gate	-	9.4μW	1.39ns
New PTL*	105.15pW	16.63μW	662ps

Fig 4 shows the Power Consumption and Delay table

Only 15 transistors are needed. The XOR design implemented in here will not produce a complete transition for 0, 0 inputs. It is considered that having smaller voltage swing will save dynamic power.

Given below are the previously obtained results for a 0.35μm 4x4 multiplier based on the new PTL cell operating at 3.3V and 500 MHz. [2] (compared with other designs)

	Proposed	16-trans	Trans. Gate
Avg. Pwr. *10^{-3}W	0.851	1.798	2.746

Table 3. Simulation results for 4bit multiplier using the 2 adder cells.

V. Area Overhead

Considering for each cell, the area consumed by CMOS is at least 4 times the area consumed by the PTL design. So if we consider a 32x32 bit multiplier a much higher saving in area can be expected from the PTL design.

VI. Proposed Model

There are two measures employed to overcome the draw backs in the conventional designs. Due to the presence of the large number of transistors in the discharge path the delay is high and also large power is consumed in power-up of the transistors. So, the number of nMOS transistors in the discharging path should be reduced. Also there is a need to increase the pull down strength when the input data=1. So there is a need to conditionally enhance the pull down strength when input data is "1." This design inherits the upper part of the SCCER design. Transistor stacking design of ip-DCO in Figure 4.4 and SCCER in Figure 4.6, is replaced by removing the transistor N2 from the discharging path. Transistor N2 and N3 are connected in parallel to form a two-input pass transistor logic (PTL)-based AND. It controls the discharge of transistor N1.

The input to the AND logic is always complementary to each other. As a result, the output node is kept at zero most of the time. There is a floating node when both input signals equal to "0". But it doesn't provide any harm to the circuit performance. The critical circumstance occurs only when there is rising edges at the clock pulse. Transistors N2 and N3 are turned ON together in this case to pass a weak logic high to node. This weak pulse strength is enhanced by switching ON the transistor N1 by a time span equal to the delay provided by inverter I1. The switching power at node can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. On designing the flip-flop in this way, the number of transistors in the discharging path can be reduced. This speeds up the pulse generation and hence delay is reduced. The area overhead is also reduced.The flip-flop using the conditional enhancement scheme is given in the Figure 3.
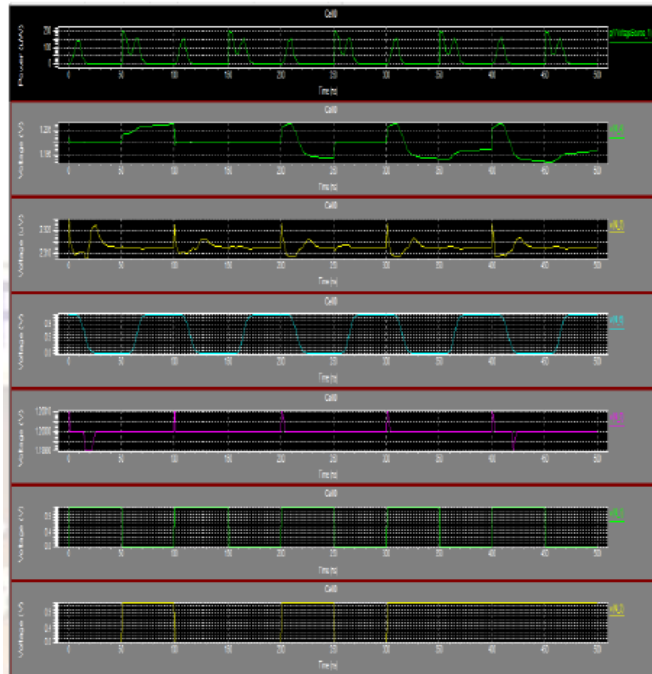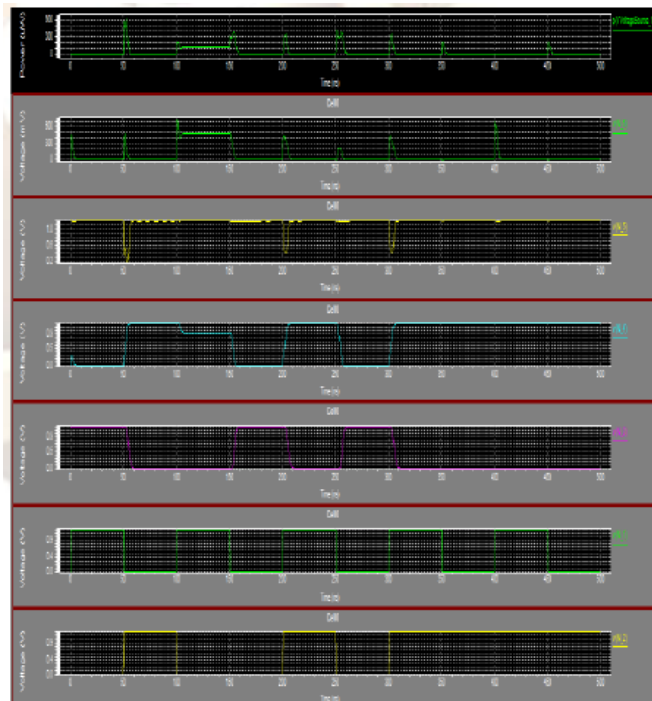
Fig 5. Simulation Waveform of HPTL

Fig 6. Simulation Waveform of the Proposed Model

Pulses that trigger discharging are generated only when there is a need, so unwanted circuit activity due to glitches can be avoided which reduces the overall power consumption. Pulse discharge can be made faster. The delay inverters which consume more power for stretching the pulse width are replaced by the PMOS transistors which enhances the pull down strength when there is a longer discharge path. Transistor sizes are also reduced to provide area and power saving.

The Waveforms
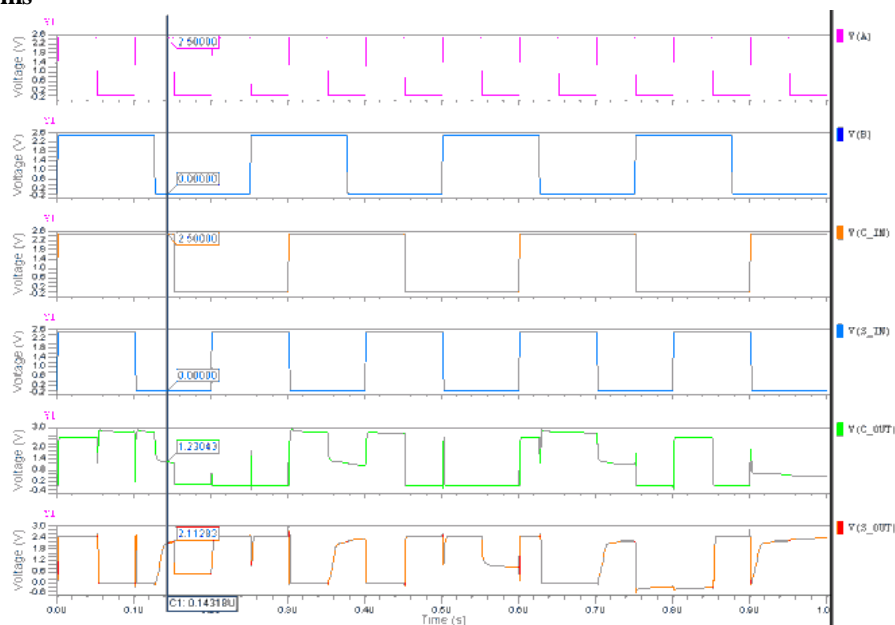
VII. Lessons Learnt

As there are no particular cell libraries for PTL designs. I had to manually create my own designs. The mistake I have done is instead of creating a single logic gate and fully optimizing it; I aggressively designed the entire multi_cell and tried to optimize the widths and lengths of that complex cell.

So whenever we want to create a complex cell, first we should start with a basic gate, try to get the best optimized design and then go for the bigger one.

VIII. Conclusion

The area overhead of CMOS is at least 4 times more than the PTL. The power consumption is less in case of PTL compared to CMOS. A good PTL design needs a lot of astute trade-offs. In clock generation circuitry an AND function is removed and is replaced with a Pass Transistor logic based AND gate. Since in the PTL style AND gate the n-mos transistors are in parallel they consume less power and provide a faster discharge of the pulse. A software package called the TANNER EDA tools utilizing MOSIS 90nm technology is used for the study. The comparison of the Number of transistors used and the Average power consumed for 100% activity, 50% activity and 0% activity are done. The power consumed is for five cycles of operation. The power consumption shows a decreasing trend as the switching activities are reduced. From the above results it is clear that this type of design approach can be implemented in real space systems to increase the efficiency as well as to minimize the power consumption

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