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Design of Hybrid Multilevel Inverter to Improve the Total Harmonic Distortion

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ABSTRACT: This paper present hybrid multilevel inverter produces 9 level voltages using three asymmetric DC voltage source to obtain pure sinusoidal waveform, and control signal for this hybrid multilevel inverter is obtained by using sinusoidal Pulse width Modulation technique. The topologies is suitable for any number of levels, this topology use less number of power Switches and used asymmetric DC voltage source help to produces higher number of voltage level need less number of DC voltage source, produces less THD ratio comparison to other present typical topologies, Simulation work is done using the MATLAB/SIMULINK software which validates the methodology and finally THD profile is presented for analysis.

Keywords: Multilevel inverters, MLI, hybrid topologies, asymmetric and symmetric voltage source configuration, CHB, THD, phase shift pulse width modulation, PWM, sinusoidal pulse width modulation, phase opposition disposition

I. INTRODUCTION

Now a day's demand of power increases day by day in industrial and domestic purpose, fulfillment of this desired power, use natural resources as wind energy, solar cell etc, these recourses used as deferent DC voltage source, these different Dc voltage source helps to get different level of voltage. One most important application of this multilevel inverter focused on medium and high-power conversion [4].

MLI has given better Total harmonic Distortion (THD) profile and the improve the efficiency instead of increased the system complexity as the gate driver circuitry and the large number of power electronics devices, capacitor, inductor used hence the system increase the effective cost and reduce the system liability and efficiency[6]. The solution of the above problem is reduction in the number of power electronics devices and gate driver circuit [9].

There are three present conventional methods in multilevel technique 1. Neutral point clamped (NPC), 2. Cascaded H Bridge (CHB), and 3. Flying capacitors (FCs) [1]. These conventional methods has own limitation as NPC has High-Voltage Rating Required for Blocking Diode, Unequal Device Rating, Capacitor Voltage Unbalance. FCs higher number of storage capacitor required, among these inverter topologies, cascaded multilevel inverter reaches the higher output voltage and power levels (13.8 kV, 30 MVA) and the higher reliability due to its modular topology. this hybrid multi level inverter is family of CHB [5],This circuit has the several advantage, lowest THD ratio in lowest number of power switches and different number of level of voltage and these shown in comparative study.[1-3]

II. TOPOLOGY AND ITS WORKING

1.1. Structure

This hybrid multilevel topology uses eight Power switches with anti parallel diodes, where as IGBT or MOSFET can be use power switches but MOSFET has higher switching losses that's why preferred IGBT as main switch (S_1,S_2,S_3,S_4) and complementary switch (G_1,G_2,G_3,G_4) connected with three anti parallel DC voltage source (E_1=12v, E_2=24v, E_3=12v) these voltage use adding methodology to produce 9 level voltage, This DC voltage source taken as asymmetrical voltage source so required less number of DC voltage source received higher number of voltage level.

There is no capacitor and diode so total cost of circuit reduced and reduced switching power losses.

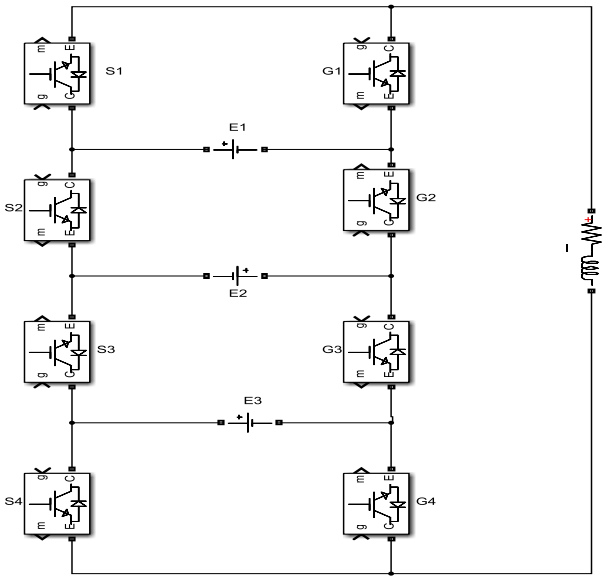

Figure.1. Single Phase nine level inverter with three asymmetric voltage source

Shown below system parameters.

Table I. System Parameters

System Parameters	**Value**		
Reference frequency	50 Hz		
Carrier frequency	1200 Hz		
Load resistance	1Ω		
Load inductance	3 mh		
DC Source	E_1=12v	E_2=24v	E_3=12v

1.2 Working

There is 9 level voltage produces with help of different voltages **+/-V, +/-2V, +/-3V, +/-4V, 0V,** hybrid multilevel has the 10 working states in this nine working states and two zero states, in which continuously four power switch working simultaneously for example for E1+ E3=36v load voltage working power switches S1, S2, S3, G2, these power switch has different voltage stress and switching frequency. Shown below table no. 2 switching stats.

Table. 2. Modes and Switching States

Level Of Voltage	**Modes**	**Load Voltage[V]**	**ON State Switches**			
0	1	0	G_1	G_2	G_3	G_4
E1	2	12	S_1	G_2	G_3	G_4
E2	3	24	S_3	S_4	G_1	G_2
E1+E2	4	36	S_1	S_2	S_3	G_2
E1+E2+E3	5	48	S_1	S_3	G_2	G_4
0	6	0	S_1	S_2	S_3	S_4
-E1	7	-12	G_1	S_2	S_3	S_4
-E2	8	-24	G_1	S_2	S_3	S_4
-(E1+E2)	9	-36	G_3	G_4	G_1	S_2
-(E1+E2+E3)	10	-48	G_1	S_4	G_3	S_2

III. SWITCHING SCHEME SIMULATION RESULTS

There are so many methods to switching methodology such as space vector and PWM etc. in PWM various strategy utilizing more triangular wave as carrier. Where as shown some technique

1. Phase disposition PWM strategy.
2. Phase opposition disposition PWM strategy
3. Alternate phase disposition strategy
4. Phase shift PWM strategy

in this hybrid multilevel inverter uses sinusoidal pulse width modulation in level shift phase disposition pulse width modulation switching scheme used in nine level topology for switching pulses. Different switches has different switching pulses, these switching pulse decided to get nine level voltages.

Voltage stress of different power switch is shown below in equation

S_2, $G_2 > S_3$, $G_3 > S_4$, $G_4 > S_1$, G_1.

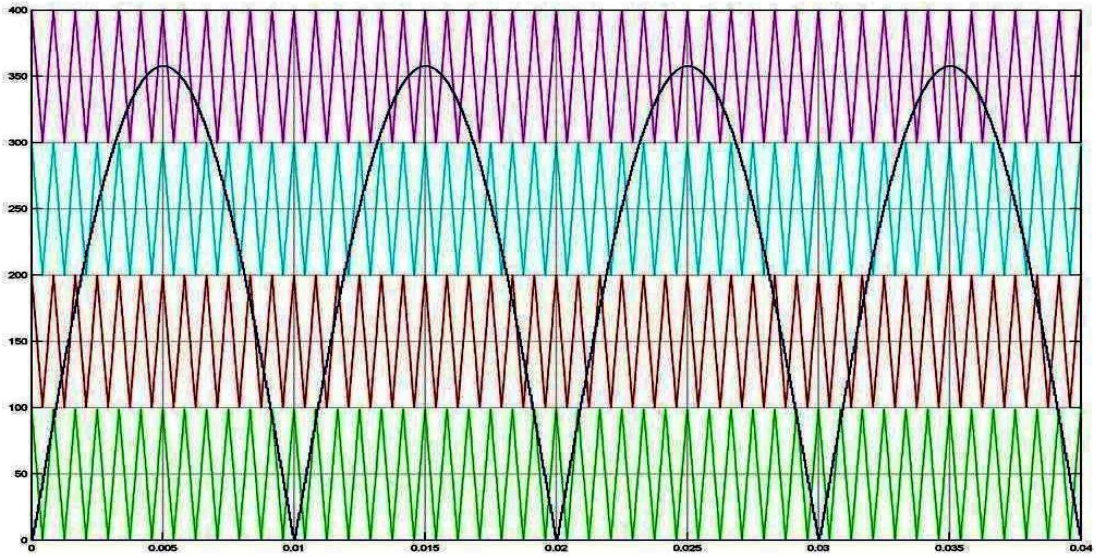

Figure.2. Refrance and carrier waveform for nine level inverter

There is used reference wave as sinusoidal wave of frequency 50hz and triangle wave as carrier frequency of 1200hz compare with the comparator result of shows in fig.2 and fig.3, comparison with the reference gives '1' when reference is greater than triangle wave otherwise gives 'o', this switching pulses added to each other get the aggregated signal, aggregated signal compare with the constant its output shows the different switching signal.

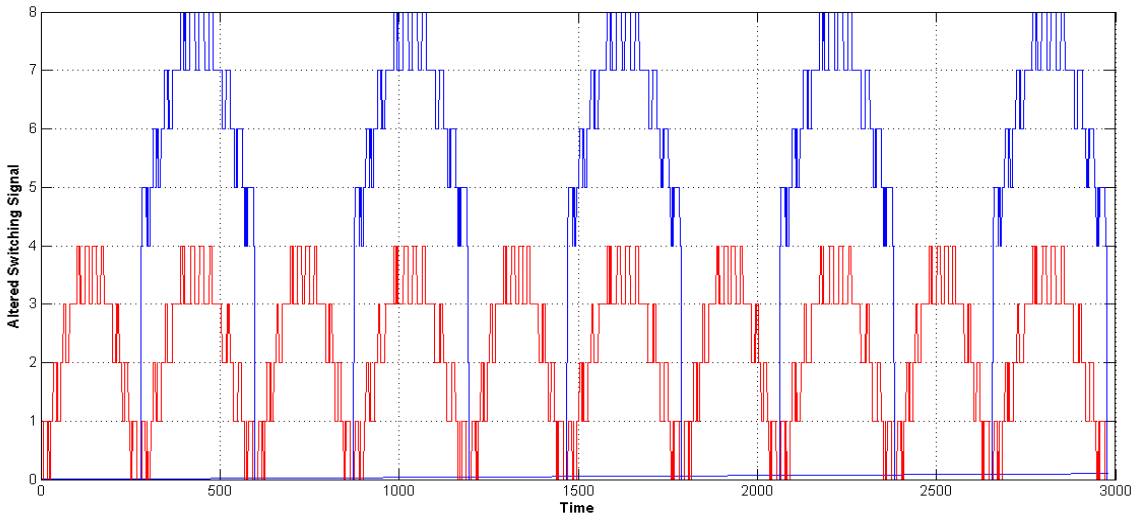

Figure.3. Altered signal

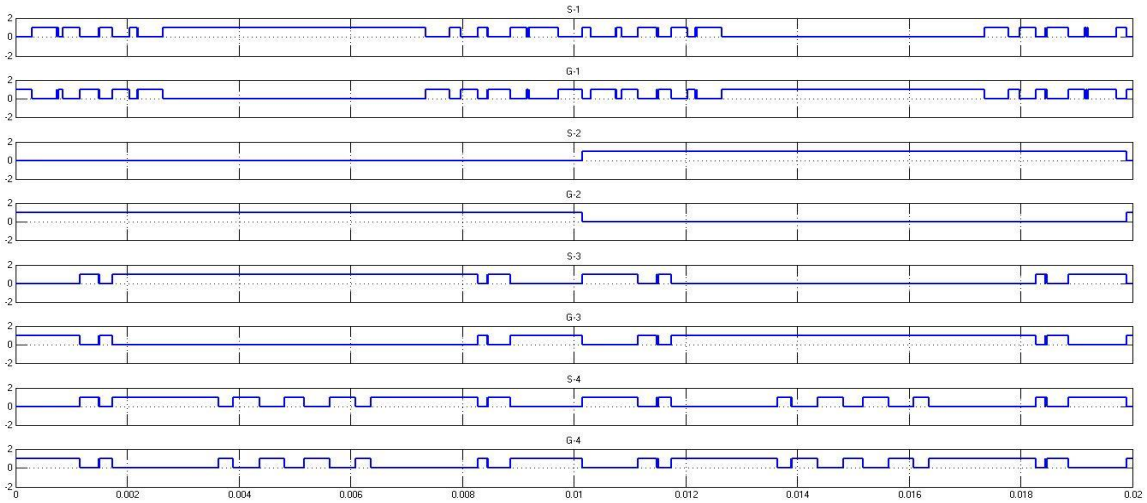

Figure.4.Switching Pulses for the nine level inverter.

IV. SIMULATION RESULTS

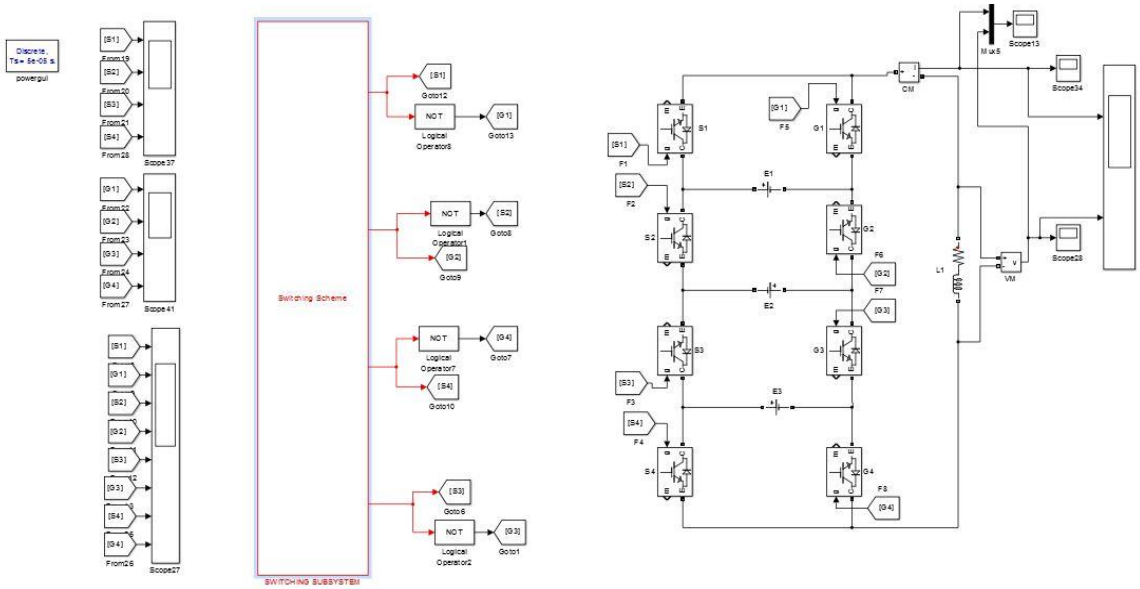

Figure .5: Simulink Model of the 9 level- hybrid multi level inverter

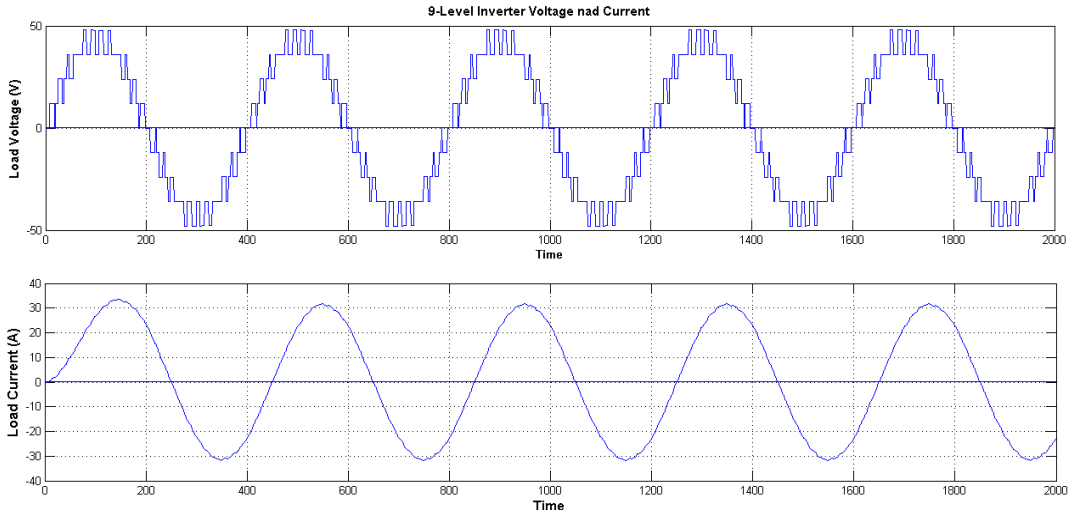

Figure.6. Simulation result of Voltage and Current

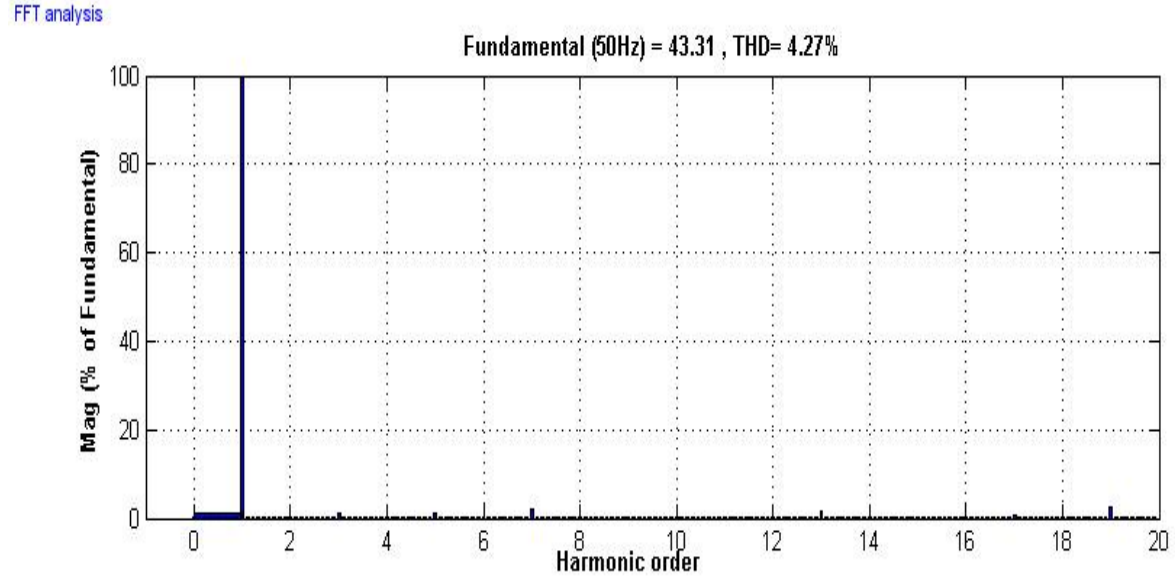

Figure.7. Total harmonic distortion for load voltage

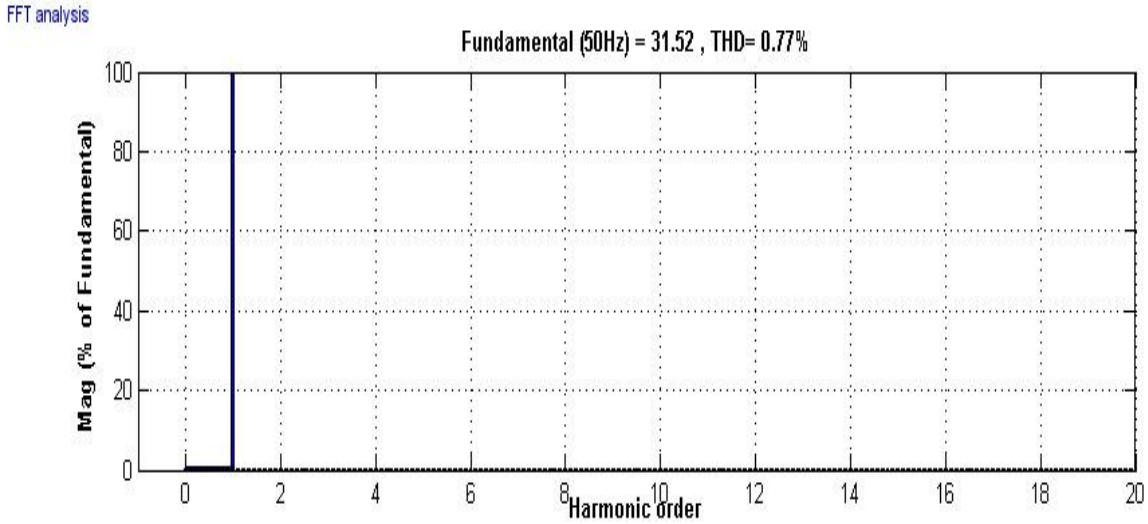

Figure.8. Total harmonic Distortion for load current

V. COMPARATIVE STUDY

In recently used family of multi level inverter, can be say that there is MLI will have to use higher number of power electronics switch and number of capacitor, diodes so that higher the system cost, increase system complexity due to gate driver circuit and increases THD ratio as example of NPC, FCs MLI, instead of hybrid multi level inverter less number of power electronics switches and other component so that low cost and decreases system complexity and used higher number of voltage level for smoothed the current wave. Over all study shown in the table no.III and table no. IV comparisons of traditional available multi level inverter with new hybrid multi level inverter

Table III. Comparison between Different Levels

Inverter	Fundamental voltage[V]			Frequency [Hz]	Voltage (THD) %	Current (THD) %
	E_1	E_2	E_3			
5-level Inverter	12v	12v	NO	50	22.27%	3.53%
7-level Inverter	12v	24v	NO	50	12.35%	1.12%
9-level Inverter	12v	24v	12v	50	4.27%	0.77%

.

Table IV. Comparison of elements, between different commercial available inverter with hybrid multilevel inverter

Inverter Configuration	Diode-Clamp	Flying-Capacitors	Cascaded inverters	New Hybrid MLI
Switching devices	2(m-1)	2(m-1)	2(m-1)	m-1
Main diodes	2(m-1)	2(m-1)	2(m-1)	0
Clamping diodes	(m-1)(m-1)	0	0	0
DC bus capacitors	(m-1)	(m-1)	(m-1)/2	0
Balancing capacitors	0	(m-1)(m-2)/2	0	0

Where m is number of components.

VI. CONCLUSION

This nine levels inverter remove the dependency from number of elements such as the capacitor and diode and increase output voltage level, it helps to reduces the system cost and also improve the total harmonic distortion(THD) profile compared with other present typical topology. This configuration of nine level topology uses the asymmetric voltage that's why needs less number of DC voltage sources by which reduce number of power electronics switch and gate driver circuit even advantage of reduction in requirement of DC sources in system it help to increases fault adjustment capability. This paper present comparative study with in term of total cost, THD and shows the all analytical and theoretical comparison. Over all reduces the THD and increase the work efficiency.

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