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Combined PWM Technique for Asymmetric Cascaded H-Bridge Multilevel Inverter

Mohammad Soltani[1], Mohammad Hosein khanzade[2], Abbas shoulaie[3]
**(Department of Power Electrical Engineering, Iran university of science and technology, Tehran, Iran)*
***(Department of FAVA Engineering, Imam Hosein University, Tehran, Iran)*
****(Department of Power Electrical Engineering, Iran university of science and technology, Tehran, Iran)*

ABSTRACT: *The increasing use of medium voltage drives and high power equipment required to detailed study on switching method and topology of multi-level inverters. In Asymmetric Cascaded H-Bridge topologies that have unequal input dc voltages and different devices in various parts of the CHB inverter, signify significant improvements for medium-voltage industrial drives. A number of modulation strategies are used in multi-level power conversion applications. In multi-carrier switching method for asymmetric CHB, the number of subject switches is less than carriers and usually is used off-line switching method. They're not applicable for closed-loop systems. In this study, introduce equations for combine the PWMs to use the controllability advantage of the multi-carrier method in asymmetric topology. This method compared with the possible level shifted based on three parameters modulation index, frequency index and output voltage THD and finally obtain the best THD for it.*

Keywords: *Multi-level inverter, Asymmetric Cascaded H-Bridge, level shifted multi-carrier, combined PWM, THD.*

I. INTRODUCTION

Multi-level voltage-source inverters are studied for high-power applications, and standard drives for medium-voltage industrial applications have become available [1]-[4]. It uses the concept of utilizing multiple small voltage levels to perform power conversion. Advantages of this multi-level approach include high power quality and electromagnetic compatibility (EMC) and low switching losses [5], [6]. The most used topologies are the neutral point clamped (NPC) [7], flying capacitor (FC) [8] and the cascaded H-bridge inverter (CHB) [9]-[13]. They are mainly controlled with sinusoidal PWM extended to multiple carrier arrangements of two types: level shifted (LS-PWM), also known as phase disposition, and phase shifted (PS-PWM) [14]. Other established modulation methods include the multi-level extension of space vector modulation (SVM), multi-level selective harmonic elimination [4] and nearest level control (NLC) [15]-[17]. The last three methods are used for lower switching frequency applications.

By using PWM techniques the inverter's fundamental voltage can be controlled and the harmonics can be attenuated. In this method a carrier signal at the desired switching frequency (f_{cr}) is generated and compared with the command or modulating voltage signal (v_m) and gate signals for the switching devices are generated by comparing the modulating signal with the carrier signal. When the modulating signal is above the carrier, the upper switch is on and when below, the lower switch is on. The fundamental frequency component in the inverter output voltage can be controlled by amplitude modulation index (m_a) is defined as [14], [18],

$$m_a = \frac{v_m}{v_{cr}} \tag{1}$$

Where v_m and v_{cr} are the peak values of the modulating and carrier signals, respectively. The frequency modulation index m_a is defined by [14], [18],

$$f_m = \frac{f_{cr}}{f_m} \tag{2}$$

Where f_{cr} and f_m are the frequencies of the modulating and carrier waves, respectively.

The CHB topology of multi-level inverter can be in two structures include symmetric and asymmetric. The symmetric multi-level inverters have the same voltage on each of the intermediate-circuit capacitors, and all the power semiconductors have to be capable to block the same voltage in their 'off' state. The asymmetric multi-

level inverters have similar circuit topology as symmetric multi-level inverters. They differ only in the input dc voltages and switching procedure [19], [20]. Higher output quality can be obtained with smaller circuit and control complexity, and output filters can be remarkably shrunk or even eliminated. The essential discussion regarding CHB topology involves the cost and the volume of the facilities. The need for more dc sources is a drawback in the CHB. Using unequal dc sources for each cell removes this drawback to a certain degree and reduces the number of switches. The volume of transformer reduction for geometry input dc voltages to the cells in the network applying the whole voltage capacity of the switches for unit with high voltage, a reduction in the number of regenerative facilities to the network upon need, reduction switching loss and etc. [13]. can be considered as the advantages of asymmetric to symmetric states. In asymmetric CHB power injection and uniform switching properties of the cells are eliminated while, the number of the cells applied in forming multi-level output voltage decrease significantly. The switching method of this topology, due to reduced number of subject switches becomes complicated; to compensate this, the SHE is suggested in the other article [21]-[27]. Attempt is made in this article to introduce a method for asymmetric topology switching which would overcome the problems in off-line method. It provides to access to the lowest level of harmonic distortion in the multi-carrier method. This method compared with the possible level shifted based on three parameters modulation index, frequency index and output voltage THD and obtain the best THD for it.

II. ASYMMETRIC CHB AND MULTICARRIER SWITCHING

In the CHB topology the unequal dc sources can be used in feeding the inverter cells, with no need in increasing the number of series in the cells, and increase the number of levels through changes in switching manner. To have the highest number of output voltage levels in asymmetric CHB the proportion between dc voltage sources of the cells must be 3^n [14]. Switching the inverters of CHB series is usually conducted through SHE and multi-carrier methods. In the asymmetric CHB series, the adopted methods are of SHE and NLC through obtaining the switching angles with less concern on multi-carrier method; since, in the method the number of switches is not of major concern, while, merely the output voltage and its harmonics are of concern. The method, through simple is off-line and is non-efficient in closed-loop system.

The fig (1) illustrate three modulation of level shifted: 1) the IPD, where all triangular waves are in-phase, 2) the POD, where all carriers above the zero reference are in phase but in opposition with those below the zero reference, 3) the APOD, where all carriers are alternatively in opposite disposition. Each one, in varying frequency index and constant modulation index has different harmonic distortion level [4]. In the multi-carrier switching method the number of voltage output level correspond to the number of carriers. The first drawback, when the asymmetric sources are applied is that the number of the switches becomes less than the number of the levels, that is, less than the number of carriers. To introduce the asymmetric inverters, to series of cells are studied where the input dc voltage of one is three-fold of the other Fig. (2).

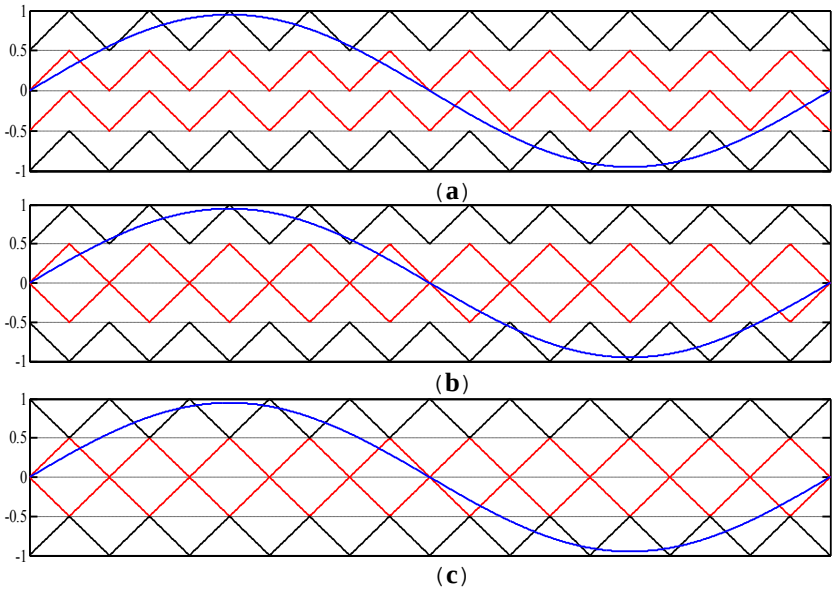

Fig. (1) Level shifted methods for 5-level inverter: a) IPD, b) POD and C) APOD

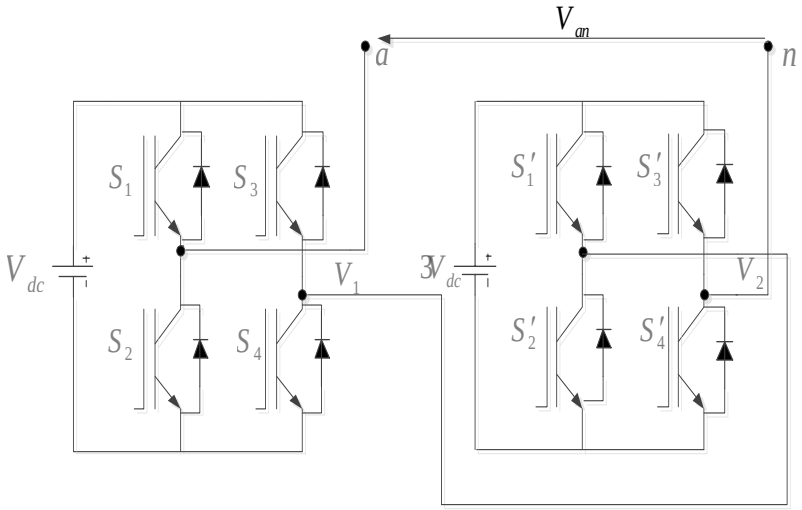

Fig. (2) The 9-level asymmetric CHB

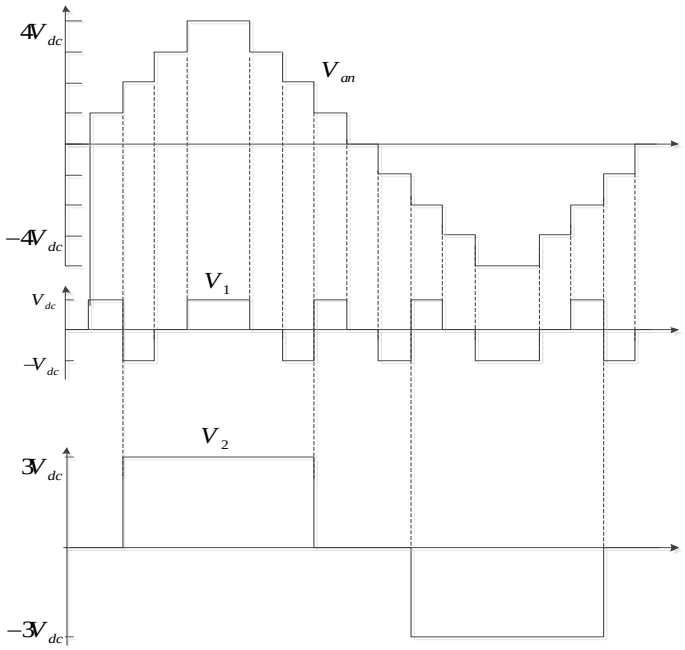

Fig. (3) Output Voltage of each one of the units

In level shifted switching, 9-level voltage is formed, including 8-voltage levels at above and below the coordinate access, where each requires one carrier wave.

The S_1, S_4, S'_1 and S'_4 switches are directly commanded by the microcontroller and switches S_3, S_2, S'_3 and S'_2 are of their corresponding NOT state, Fig. (2).This phenomenon is due to lack of simultaneous of ON switches of one branch and avoid from possible vulnerability. The problem with switching in asymmetric CHB is that the number of separate PWM (that generated by comparing the carrier waves with the reference wave) almost twice the number of the subject switches. Overall, two PWM pulses are required for each cell, that is, these face switches function are formed by a combination of eight PWMs which eventually results in the output voltage in state of two cells, Fig. (3).

III. PROPOSED SWITCHING METHOD

The carrier waves and generated PWMs from them are illustrated in Fig. (3). According to Fig. (4), high voltage cell is an H-Bridge inverter, applied for the 3-level output voltage. Here, switching of low voltage cell where combined PWM generated from carriers is applied. The whole command blocks of both the inverter cells are drawn in Fig. (5).

In this switching, it is assumed that S_1, S_4, S_1' and S_4' are the subjects of the command. If the PWMs of the positive carriers in coordinate axes are named as P_1-P_4 and the negative coordinate axes are named as q_1-q_4, then, the switches state to provide low and high voltage cells for different levels would be presented as tabulated in Table (1). In this table, the sign (-) denoted OFF and the sign (+) denotes ON. When the diode is in parallel and inverse position, the switch is assumed ON state.

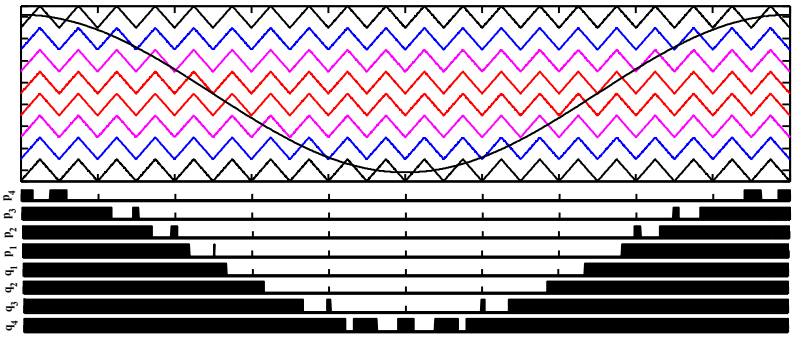

Fig. 4- Comparison of carriers with reference wave and formation of the PWM

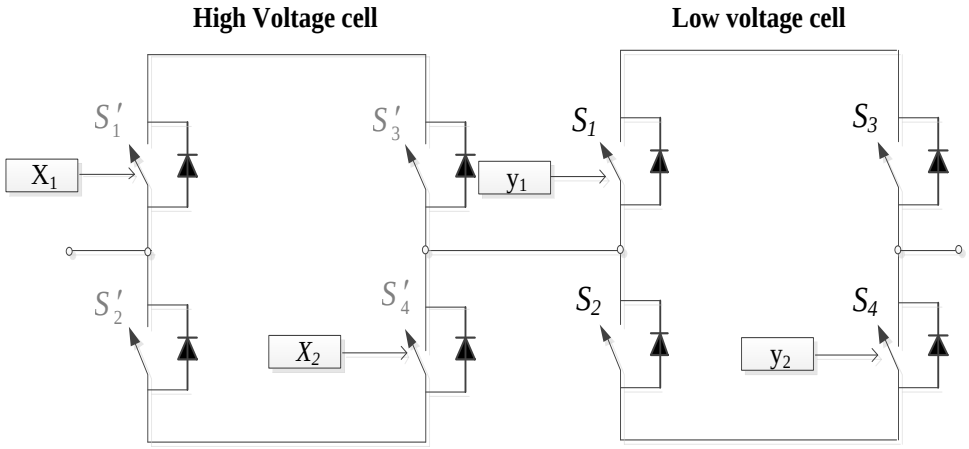

Fig. 5- The control blocks of the two inverter cells to generate 9-level output

Table 1- general switching states of the 9-level output

Output	***HV***	***LV***	S_4	S_3	S_2	S_1	S_4'	S_3'	S_2'	S_1'	
+4V	*+3V*	*+V*	+	-	-	+	+	-	-	+	p_4
+3V	*+3V*	*0*	+	-	+	-	+	-	-	+	p_3
+2V	*+3V*	*-V*	-	+	+	-	+	-	-	+	p_2
+V	*0*	*+V*	+	-	-	+	+	-	+	-	p_1
0	*0*	*0*	-	+	-	+	+	-	+	-	**-**
-V	*0*	*-V*	-	+	+	-	+	-	+	-	q_1
-2V	*-3V*	*+V*	+	-	-	+	-	+	+	-	q_2
-3V	*-3V*	*0*	+	-	+	-	-	+	+	-	q_3
-4V	*-3V*	*-V*	-	+	+	-	-	+	+	-	q_4

When the output voltage level reaches upper than +V or less than –V, the output of high voltage cell would be ±3V hence, the obtained PWM from carrier of the same level is applied to high voltage cell.

As observed in Table 1, in order for the x_1 and x_2 commands, Fig. 5,to have a 3-level voltage in high voltage cell, p_2 and q_2 become applicable, Eqs. (3 and 4).

$$x_1 = p_2 \quad (3)$$

$$x_2 = q_2 \quad (4)$$

To obtain the combined equation of PWMs, for the low voltage unit, the S_1 in the positive coordinate axes, any change in switching situation of the PWM subject are added with respect to their signs. If in the negative coordinate the voltage levels are sought, any change in switching situation of the PWM subject are deducted that is. On the other hand, the total status change of the ps and negative of qs constitute the general equation for S_1 switch through the following equation:

$$y_1 = p_1 - p_2 + p_4 - (q_2 - q_3) \quad (5)$$

To command S_4 switch, the PWMs symmetric of switching in Eq. (5) are applied. In fact, this symmetry is the difference of 180˚ between S_4 and S_1 command and the ps in Eq. (5) are converted to qs in Eq. (6) and vice versa. Therefore, the PWM control equation for the S_4 is presented as: Eq. (6).

$$y_2 = q_1 - q_2 + q_4 - (p_2 - p_3) \quad (6)$$

IV. THE SIMULATION RESULTS

If the y_1, y_2, x_1 and x_2 switching functions are implemented initially each one of the functions with m_f=20, Fig. (6). The output voltage of each one of the inverter cells, according to necessary reference is shown in Fig. 7. As observed reference wave of low voltage cell is out of sine shape and is generated as a result of deducting the inverter reference wave from the output voltage of HV cell.

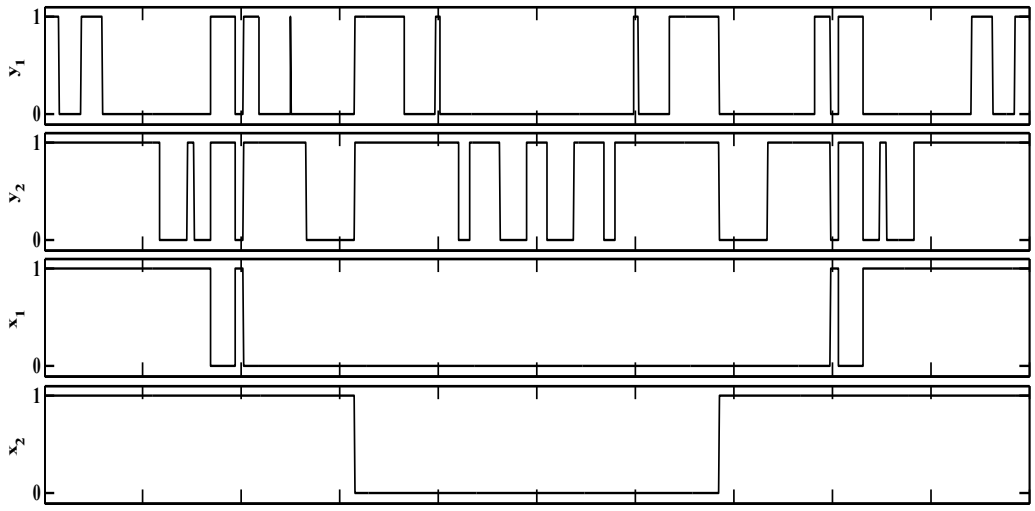

Fig. 6- The combined PWMs subjects in controllable switching at 9-level inverter

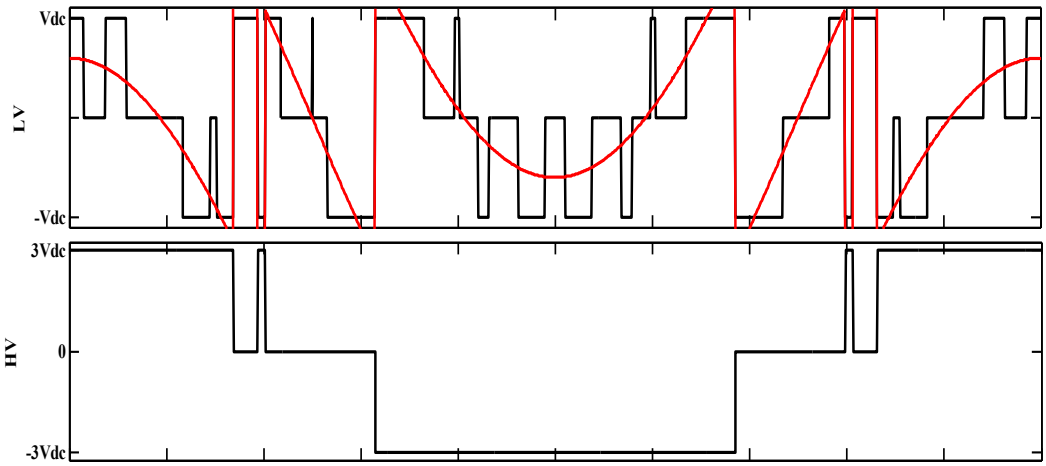

Fig. 7- The output voltage of each one of the CHB cells at asymmetric 9-level converter

In assessing the available multi-carrier methods the three essential parameters are modulation index, frequency index and the output voltage THD; that is in order to compare the THD in the IPD, POD and APOD methods the other two parameters will be effective. For better comparison in simulating the methods here, the carrier frequency is set at f_{cr} =2000 Hz. The simulation results of the asymmetric inverter through this PWM combined multi-carrier method is proposed, Fig. 8, where the output voltage in the IPD model and harmonic components of that are illustrated.

The schema of the output voltage and their harmonic components in POD and APOD methods are presented in Figs. (9 and 10). To compare the level shifted methods in asymmetric CHB converter, first, the uniform frequency index, the modulation index is obtained in accordance to the output voltage THD.

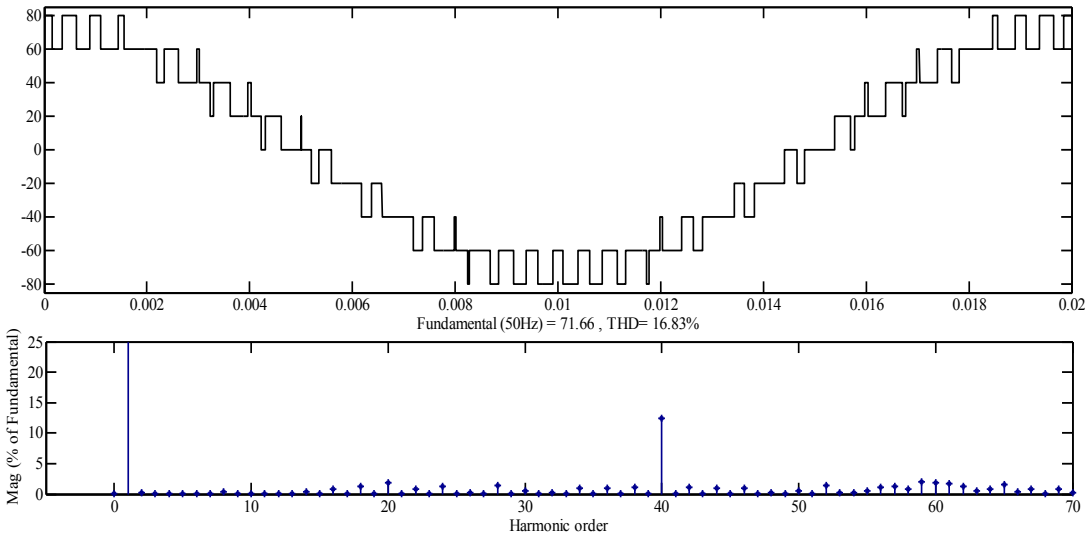

Fig. 8- 9-level output of asymmetric CHB through IPD switching method and harmonic components of output voltage for m_f=40 and m_a=0.9

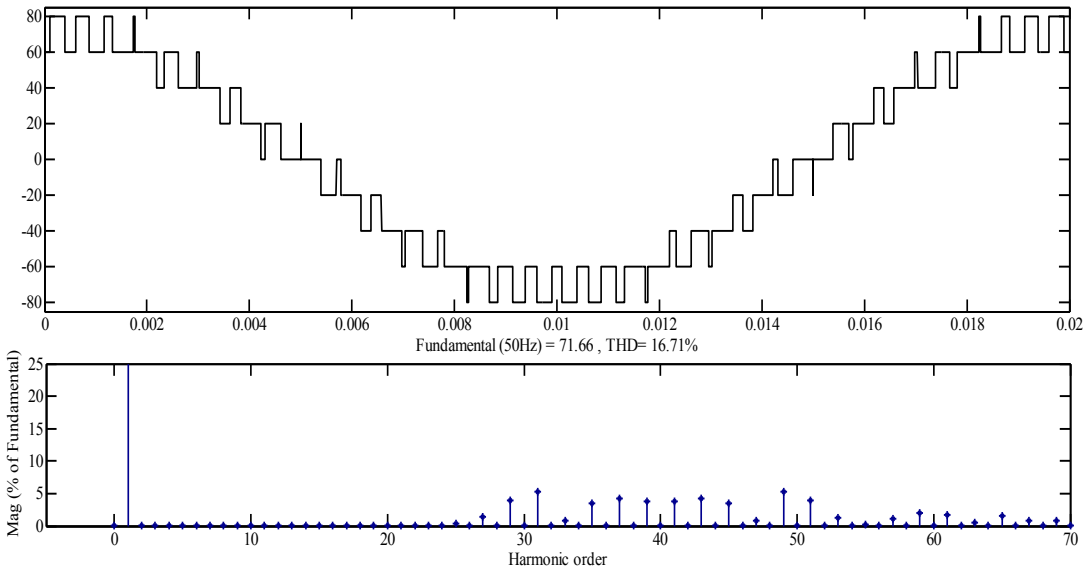

Fig. 9- 9-level output of asymmetric CHB through APOD switching method and harmonic Components of output voltage for m_f=40 and m_a=0.9

The comparison of output voltage THD in accordance with modulation index in all level shifted modes is at 1000 Hz carrier frequency. At this frequency the IPD model in most indexes has the mean of voltage THD coefficient. With the same manner of comparison in Fig. 12, at 2000 Hz frequency, less distance is observed among the curves. This phenomenon is due to the fact that the first harmonic distortion becomes distance from zero, hence, lowering the even harmonic distortion range close to zero.

As observed in Figs. (9 and 10) the first harmonic distortion for POD and APOD methods fall in $m_f \pm 1$, while if the m_f is an even number the harmonic distortion would fall in odd components. In POD and APOD method when m_f is an odd number, the output voltage has odd and even components to generating an increase at THD. This phenomenon in IPD method is the opposite and as observed in fig. 14, the best function of THD when the m_a close to one and the m_f is odd and close to 20. The volumes of the modulation and frequency indexes applied in the previous simulation are illustrated in Fig. 14.

After assessing the curves in this figure the m_a =1.09 and m_f =23 status can be observed in Fig. 15. At different m_a s and m_f =23 of IPD, POD and APOD methods based on THD are presented in Fig. 13.

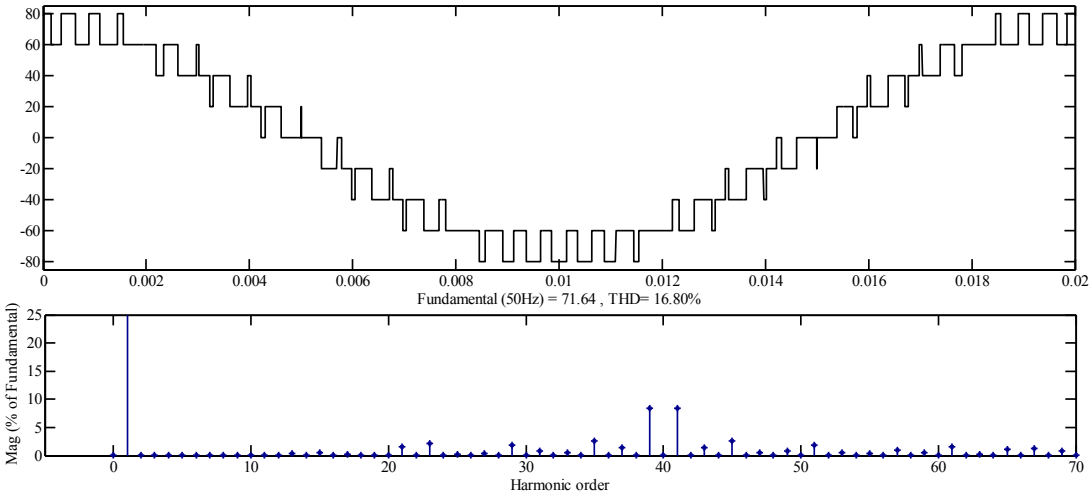

Fig. 10- 9-level output of asymmetric CHB through POD switching method and harmonic components of output voltage for m_f=40 and m_a=0.9

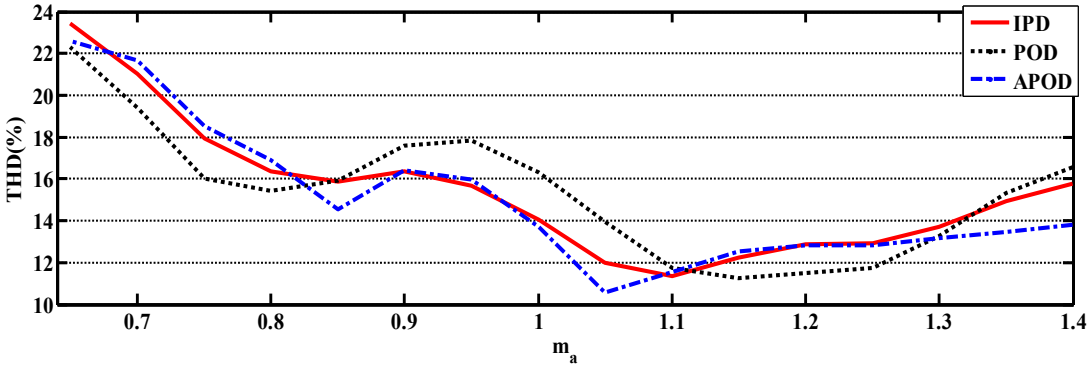

Fig. 11- The comparative diagram of level shifted methods at THD output voltage in accordance to different modulation indexes of f_{cr}=1000 Hz

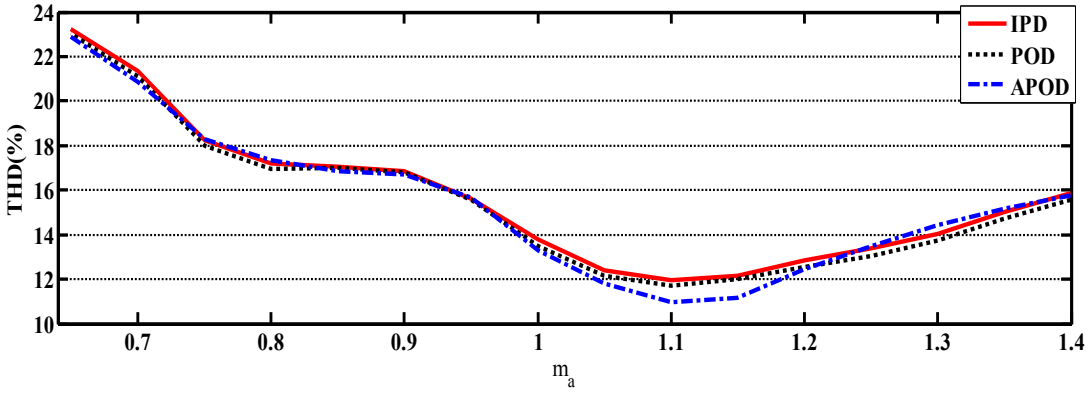

Fig. 12- The comparative diagram of level shifted methods at THD output voltage in accordance to different modulation indexes of f_{cr}=2000 Hz

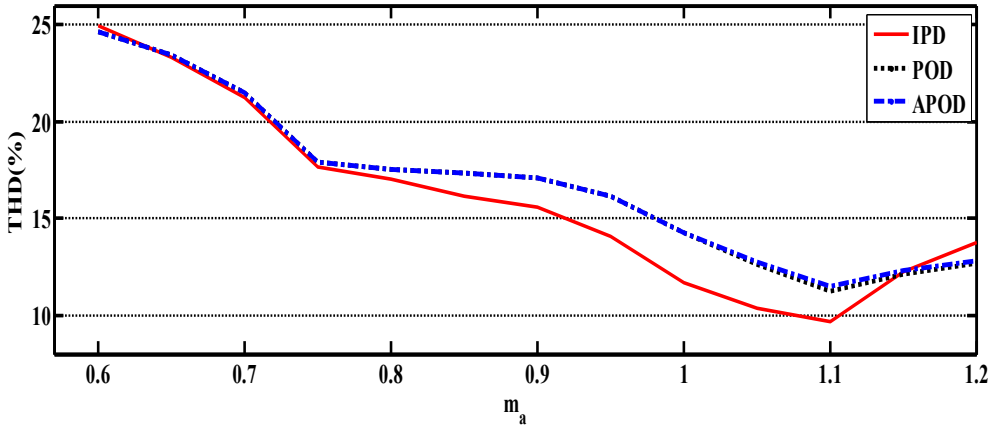

Fig. 13- Comparison of THD with respect to m_as for three methods of level Shifted at f_{cr}=1150 Hz switching

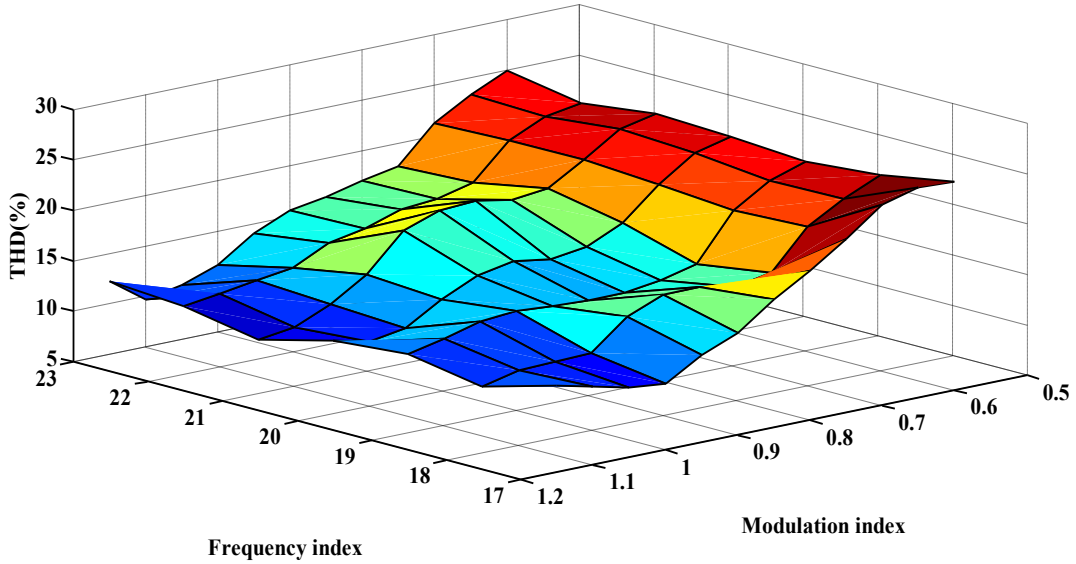

Fig. 14- Comparison of output voltage THD at different m_fs per m_a in IPD

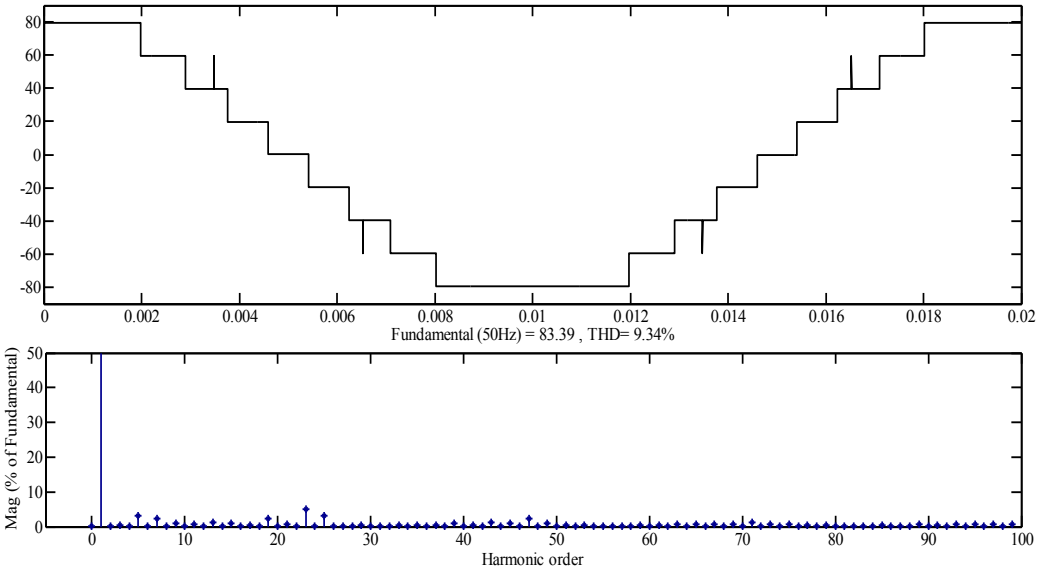

Fig. 15-The output voltage and its harmonic components according to this Proposed level shifted method at the best performance

V. CONCLUSION

In asymmetric CHB topology the number of the applied inverter units in forming multi-level voltage decreases significantly. The switching method of this topology becomes complicated due to a reduction in the subject switch count. The SHE and NLC methods are proposed in many articles and are considered inferior to multi-carrier methods, since, they are Off-Line. In multi-carrier method for this topology the number of carriers is more than the subject switches. In this study, combined PWM method is proposed to make the multi-level output voltage for asymmetric inverter efficient in closed-loop systems. This switching is adopted in POD and APOD at different modulation and frequency indexes, and their output voltage THD are compared, indicating that in IPD method the first harmonic distortion falls in frequency indexes, m_f and in POD and APOD it falls in $m_f \pm 1$. Therefore, in order to reduce even harmonic components, the best performance in IPD is odd frequency index and in the other two methods are even indexes. In this frequency index the IPD method has less harmonic distortion coefficient per m_a in relation to other two methods. Results indicate that this approach has an appropriate harmonic function and respect to its Online nature it is advantages to other popular asymmetric multi-level switching inverter.

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