International Journal of Modern Engineering Research (IJMER)
www.ijmer.com Vol.2, Issue.1, Jan-Feb 2012 pp-473-478 ISSN: 2249-6645

Design and Implementation Of Low Power CMOS Radio Receiver

[1]Neha Agarwal , [2]Dwijendra Parashar

[1](Department of Electronics and Communication, Laxmi devi Institute of Engg. & Technology Alwar)India
[2](Department of Electronics and Communication, Shobhit University Meerut, India

Abstract

A single-chip CMOS Global Positioning System (GPS) radio has been integrated using only a couple of external passive components for the input matching network and one external reference for the synthesizer. This paper explores architectural and design techniques for CMOS wireless receivers through the vehicle of the GPS system. This system comprises 24 satellites in low earth orbit that continuously broadcast their position and local time. Through satellite range measurements, a receiver can determine its absolute position and time anywhere on Earth, as long as four satellites are within view. Examples of such applications include automotive or maritime navigation, intelligent hand off algorithms in cellular telephony, and cellular emergency services, to name a few. To enable a cheap, low-power CMOS GPS solution, this work develops a receiver architecture that lends itself to complete integration. To implement this architecture, two major foci are the design of low-noise amplifiers (LNAs) and power efficient active filters in CMOS technologies. The realization of a 2.4dB noise figure, differential LNA is with only 12mW power consumption in a 0.5µm CMOS technology. Another focus is on the power efficient implementation of wide dynamic range active filters. In such filters, the design of the transconductor element is critical, and techniques for evaluating transconductor architectures are presented. An application of these ideas are to the GPS receiver problem results in a 10mW, 60dB peak spurious free dynamic range (SFDR) active filter with 3.5MHz bandwidth. These advances enable the realization of an 115mW CMOS GPS receiver that includes the complete RF and analog signal path, frequency synthesizer and A/D converters.

Keywords- ***Introduction, Radio receiver, GPS system architecture, Chip design, CMOS Mixer, Conclusion, Reference.***

I. Introduction

GLOBAL Positioning System (GPS) receivers for the consumer market require solutions that are compact, cheap, and low power. Manufacturers of cellular telephones, portable computers, watches, and other mobile devices are looking for ways to embed GPS into their products. Thus, there is a strong motivation to provide highly integrated solutions at the lowest possible power Consumption. GPS radios consist of a front-end and a digital baseband section incorporating a digital processor. While for the baseband processor, cost-reduction reasons dictate the use of the most dense digital CMOS technology, for the front-end, the best option in terms of power consumption is a SiGe BiCMOS technology. This explains why several commercial GPS radios consist of dual or multichip systems using the best technology option for the front-end and baseband processor. On the other hand, the implementation of a stand-alone GPS radio into a single chip in CMOS technology is appealing in terms of cost, and would speed up the integration of GPS capabilities into mobile products. This motivated the development of GPS macro blocks and radios in CMOS technology. However, the cost effectiveness of this solution depends on both reduction of external components and die area of the GPS radio. Since the silicon area of RF CMOS circuits, including on-chip inductors, does not shrink at the same rate as technology scaling, the reduction of the total cost poses a severe challenge. Typically, GPS radios are implemented in bipolar or BiCMOS processes and cannot be integrated with the digital signal processor chip due to higher cost. Furthermore, they use multi-down conversion receiver architectures that require off-chip filters, adding to the footprint and cost.

The Global Positioning System (GPS) is a satellite-based navigation system made up of a network of 24 satellites placed into orbit by the U.S. Department of Defense. GPS was originally intended for military applications, but in the 1980s, the government made the system available for civilian use. GPS works in any weather conditions, anywhere in the world, 24 hours a day. There are no subscription fees or setup charges to use GPS. All satellites transmit at both frequencies and their signals are distinguished by different Gold codes used to spread the signal, where most commercial GPS receivers use the L1 signal only. The system is based on time-of-arrival (TOA) of signals from the visible satellites. Using the location and time information sent by satellites and TOA from at least four visible satellites, four equations can be solved for altitude, latitude, longitude, and time.

II. Radio Receiver Architecture

The advent of wireless communications at the turn of the 20th century marked the beginning of a technological era in which the nature of communications would be radically altered. The ability to transmit messages through the air would soon usher in radio and television broadcasting and wireless techniques would later and application in many of the mundane tasks of everyday life. Today, the widespread use of wireless technology conveys many benefits that are easily taken for granted. From cellular phones to walkie-talkies; from broadcast television to garage door openers; from aircraft radar to hand-held GPS navigation systems, radio technology pervades modern life. At the forefront of emerging radio applications lies modern research on the integrated radio receiver. The goal of miniaturization made possible by integrated circuit technologies holds the promise of portable, cheap and robust radio systems, as exampled by the advent of cellular telephony in the mid-1980's. As miniaturization continues, embedded radio applications become possible where the features of multiple wireless systems can be brought to bear on a particular problem. One example is the use of a GPS receiver in a cellular telephone to permit the expedient dispatch of emergency service personnel to the caller's exact location.

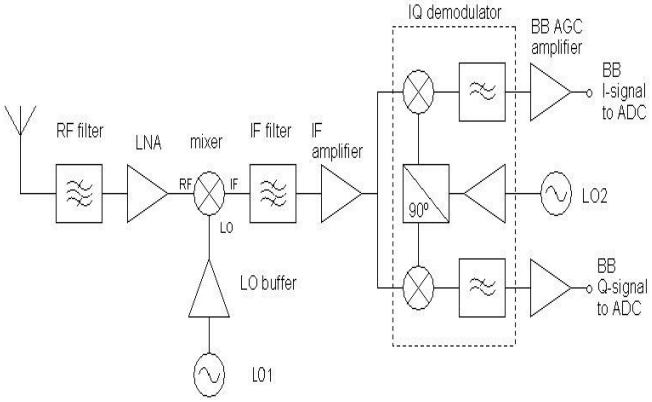

Fig-1 Super Heterodyne Receiver.

Figure1 makes use of a parallel data detector concept. There are two types of detector such serial data and parallel data. Both detector concepts are generally applicable for demodulation. The main difference is that the serial detector makes use of real signal representation whereas the parallel detector uses complex signal representation. As a result the

Serial detector is generally less complicated and lower power consumption is potential. However, the parallel detector generally provides for better performance in fading environments than does the serial detector and as a result the parallel detector is the most widely used. Also, the use of the parallel data detector concept of Figure1generally improves on the image rejection. Ideally, the complex signal representation provided by the parallel detector allows for Complete separation of the desired signal and the corresponding image signal. By prober combining of the I and Q signals it is possible to relocate the desired and the image signal to positive and negative frequencies, respectively. This, however, requires exact matching of the I and Q signal branches which is not possible in a practical implementation. One way of illustrating the effect of I/Q mismatch is to consider a complex input signal consisting of unmodulated single tone signals,

$$s(t)= \cos(2\pi f_{IM} t) + j\alpha \sin(2\pi f_{IM} t + \theta)$$

$$s(t)= \tfrac{1}{2} [e^{j2\pi fIMt}(1+ \alpha.e^{j\theta})] + \tfrac{1}{2}[e^{-j2\pi fIMt}(1 - \alpha e^{j\theta})] \quad (1)$$

As the amplitude α and phase θ errors are relative values these can be assigned to just one of the signal. The term $e^{j2\pi fIMt}$ and $e^{-j2\pi fIMt}$ can be view as the desired and image signal respectively. Hence, from Equation (1) it is seen that in case of ideal matching, i.e. (α,θ) = (1; 0), the image signal component is cancelled. By comparison of the amplitude terms of the desired and the image signal components he approximate amount of I/Q image discrimination.

A. Radio Spectrum

The goal of any radio receiver is to extract and detect selectively a desired signal from the electromagnetic spectrum. This selectivity" in the presence of a plethora of interfering signals and noise is the fundamental attribute that drives many of the tradeoffs inherent in radio design. Radio receivers must often be able to detect signal powers as small as a femtowatt while rejecting a multitude of other signals that may be twelve orders of magnitude larger! Because the electromagnetic spectrum is a scarce resource, interfering signals often lie very close to the desired one in frequency, thereby exacerbating the task of rejecting the unwanted signals.

B. Classical Receiver Architecture

The design of wireless receivers is a complex, multi-faceted subject that has a fascinating history. In this section, we will explore many of the fundamental issues that arise in receiver design through the vehicle of historical examples. These early receiver architectures illustrate an increasing level of sophistication in response to the need for improved selectivity at ever-greater frequencies.

C. Crystal detector

The received signal from the antenna is band pass filtered and immediately rectified by a simple diode. If a sufficiently strong amplitude modulated radio signal is received, the rectified signal will possess an audio frequency component that can be heard directly on a pair of high-impedance headphones. The desired radio channel can be selected via a variable capacitor (or condenser, according to the terminology of the day). Remarkably, this

radio does not require a battery; the received signal energy drives the headphones directly without amplification.

III. GPS System Architecture

SUCCESSFUL radio designs begin with good architectural choices. Unfortunately, there is no radio architecture panacea. Rather, it is essential to select the approach best suited for the task at hand. In this section, we turn our attention to selecting the GPS radio architecture that will permit the maximum level of integration while minimizing power consumption. We begin with the details of the GPS system itself. As will be shown, the GPS system possesses certain unique features that make it particularly well suited for integration.

To motivate the architectural choices described in this chapter, it is important to consider some details of the received GPS signal spectrum. The GPS system uses a direct-sequence spread spectrum technique for broadcasting navigation signals. In such an approach, the navigation data signal is multiplied by a pseudo-random bit sequence (PRBS) code that runs at a much higher rate than the navigation symbol rate. This higher rate is commonly referred to as the "chip rate" of the code. The PRBS codes used in the GPS system are Gold codes that have two possible values (±1) at any given time. Thus, when a code is multiplied by itself, the result is a constant value; however, when two different codes multiply each other, the result is another PRBS sequence. This property can be used to separate overlapping received signals from multiple satellites into distinct data paths for navigation processing. In principle, by multiplying the received signal by a particular satellite's PRBS code, the receiver can recover data from that satellite alone while signals from other satellites pass through with the appearance of pseudo-random noise. Hence, with a unique PRBS code assigned to each satellite, all satellites can broadcast at the same frequency without substantially interfering with each other.

The GPS satellites broadcast navigation signals in two bands: the L1 band, which is centred at 1.57542GHz, and the L2 band, centred at 1.2276GHz. Each satellite broadcasts two different direct-sequence spread-spectrum signals. These are known as the P code (or precision code) and the C/A code (or coarse acquisition code). The P code is broadcast in both frequency bands, while the C/A code is broadcast only in the L1 band. Note that the centre frequencies of the L1 and L2 bands are both integer multiples of 10.23MHz, which is the chip rate of the P code signal. In contrast, the C/A code uses a lower chip rate of 1.023MHz. The P code is intended for military use and is much more difficult to detect, in part because it uses a spreading code that only repeats at 1-week intervals. In addition, the P code is encrypted to restrict its use to authorized (military) users. For this reason, the C/A code is of primary interest in commercial applications.

The spectrum of the GPS L1 band shows that the C/A code and the P code occupy the same 20-MHz spectrum allocation, but their main lobes have different bandwidths due to the different code chip rates. In particular, the C/A code has a main lobe width of 2MHz while the P code has a width of 20MHz. The outlying lobes of the P code are truncated by appropriate filtering so that the entire GPS broadcast fits neatly within the 20-MHz allocation. The immunity to interference that is gained when using the spread-spectrum technique is related to the ratio of the chip rate to the symbol rate.

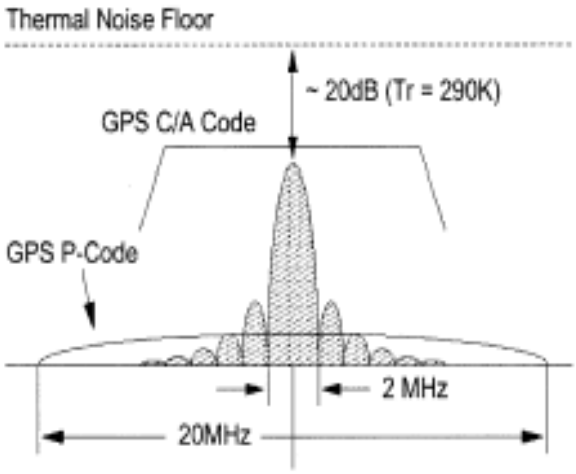

Fig-2 GPS L1 band signal spectrum.

This ratio, called the processing gain, gives an indication of the improvement in SNR that occurs when a signal is de-spread". For the GPS C/A code, the symbol rate is a mere 50Hz. Thus, the processing gain is given by

$$G_p = 10\log\left(\frac{fc}{fb}\right) = 43\text{dB} \qquad (2)$$

Where f_b the symbol rate of the C/A code and f_c is the chip rate. The received signal power is typically 130dBm at the antenna of a GPS receiver. If we assume that we are primarily interested in the 2-MHz main lobe of the C/A code, the noise power in this 2-MHz bandwidth is simply given by kTB≈-111dBm (T = 290K). Hence, the received SNR at the antenna is about 19dB. Once the signal from a given satellite is correlated with its PRBS code, the bandwidth is reduced to only 100Hz. Thus, the post correlation SNR improves by the processing gain of the system. So, with an antenna temperature of 290K and an otherwise noiseless receiver, the post-correlation SNR would be about 24dB.

IV. Chip Design

As stated, the overall design has been geared to a high level of integration and reduction of silicon area at the lowest possible power consumption. Below, the detailed design choices in the various sections are described.

a) RF Section-

The LNA has been designed to have a very low noise since it sets a lower bound for the total receiver sensitivity. A high voltage gain is necessary to sufficiently reduce the noise contribution of the following mixers. A common source configuration with inductive degeneration provides high voltage gain and low NF, as shown in Fig. 3. In fact, in a narrow band, this structure allows achieving a noise factor close to the theoretical minimum.

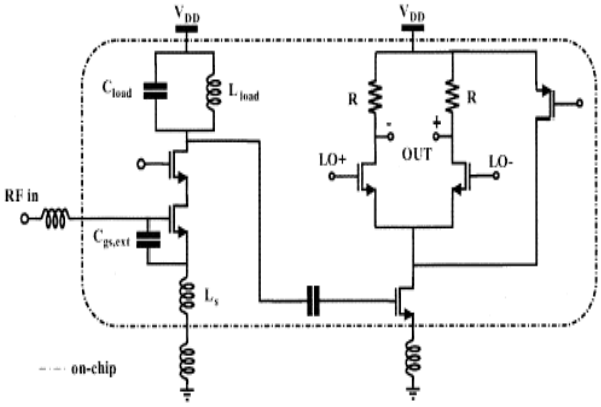

Fig-3 Low noise amplifier and mixer

A single-ended LNA has been preferred to a balanced one to reduce power consumption and silicon area. The input of the mixer is still single ended, but from its output, the signal is taken in a differential fashion. In this topology, at a given frequency, there is an optimum device size for which the sum of gate induced and thermal noise has a minimum. Because of the strong sensitivity of the gate-induced current noise to the intrinsic gate capacitance (it follows a square law), an improvement can be obtained with the introduction of an additional capacitance C_{gset} placed in parallel to the intrinsic gate capacitance C_{gs} of the input transistor. The insertion of this capacitance adds a degree of freedom to play with to achieve a better compromise between thermal and induced-gate noise. Therefore, a new optimum condition, with a lower noise figure minimum, can be achieved. This is paid by a slightly lower transconductance gain.

The LNA is followed by the - mixers that are ac-coupled to the LNA and are based on a modified Gilbert cell. The mixers can be directly driven by the on-chip frequency synthesizer or by a single external local oscillator (LO) signal that drives an integrated RF poly phase filter. Improved linearity and reduced noise are achieved by subtracting dc current from the switching pair. The load is a simple resistor. The current consumption is 1.5 mA for each mixer with an input P1 dB of 12 dBm.

b) IF Section-

After down conversion, the signal is amplified using a variable-gain amplifier (VGA) with 20-dB gain programmability. A second-order integrated passive poly phase filter has been used to recombine the I and Q signal path. The poly phase filter is an *RC* structure with inputs and outputs symmetrically disposed. The relatively small ratio between the signal band and IF frequency allows building the combiner as the cascade of two *RC* passive poly-phase filters. A rejection of 30 dB across the 2-MHz band is achieved for ±20% *RC* time constant spread.

The IF filter is centered at 9.45 MHz To fit the 2-MHz GPS band, even in presence of component values variations, the nominal transfer function features a larger bandwidth (6 MHz) than the one needed (2 MHz). However, a ripple in the GPS band (8.45–10.45 MHz) lower than 0.5 dB is guaranteed in any case. To optimize the power consumption for a given linearity and noise, an active *RC* solution has been chosen. The filter is built as a cascade of a band pass and a low-pass cell, implementing a fourth-order transfer function. The filter also provides an antialiasing function before the baseband ADC, assuring 20-dB attenuation at 28 MHz

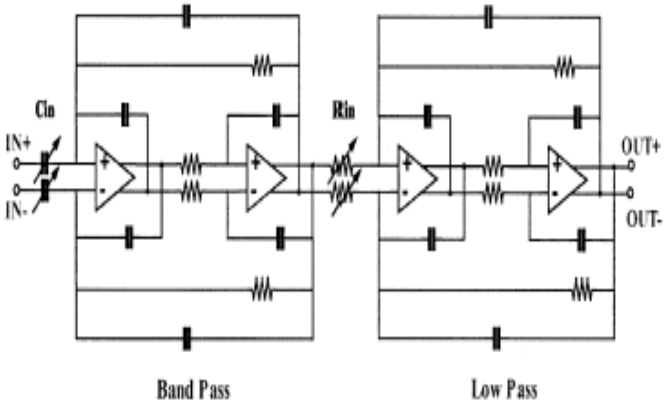

Fig-4 IF Filter

c) Synthesizer

The synthesizer, depicted in Fig, provides LO quadrature signals for the image-reject mixer and two clock signals needed to synchronize the correlator inside the external baseband processor. As for the previously described blocks, the main concern has been a high level of integration and reduction of silicon area at the lowest possible power consumption. The requirement of high integration and the need to reduce risks of LO pulling due

to off-chip components have driven the choice of a fully integrated voltage-controlled oscillator (VCO) and loop filter. For this application, we took advantage of the low requirements on phase noise and spurious rejection using a ring oscillator within a wide-band phase-locked loop (PLL) instead of an inductance-capacitance (*LC*) VCO. This choice resulted in a dramatic reduction of the silicon area, since it does not require integrated inductors or varactors. Furthermore, the ring oscillator directly provides *I-Q* quadrature LO signals needed by the image-reject mixer and simplifies the portability of the GPS radio to a pure CMOS process with associated low-quality factor on-chip inductors. The use of a ring oscillator requires a wide-band PLL to reduce its contribution to the total phase noise. The added benefit of this choice is the integration of the loop filter in a limited silicon area. This is highly desirable to reduce the risk of VCO pulling due to external interferences coupled through the wire bonding. A 500-kHz band is implemented with 12 pF in parallel with the series of 300 pF and 6.4 kΩ.

The synthesizer is comprised of a crystal oscillator that generates the 18.414-MHz reference frequency using an off-chip crystal. Its output is divided by four and used as the comparison frequency. The VCO generates the quadrature local oscillator (LO) signals for the receiver mixers. The LO signal is divided by 342 and input to the PFD along with the comparison frequency.

The PFD has a delay element in its feedback loop to prevent a dead- zone region in the charge pump. The resulting filtered charge-pump output controls the VCO. Here, an off-chip second-order filter was used. GPS is a single-frequency system and a start-up time of less than 5 ms is acceptable. Therefore, synthesizer-settling time was not an important design factor.

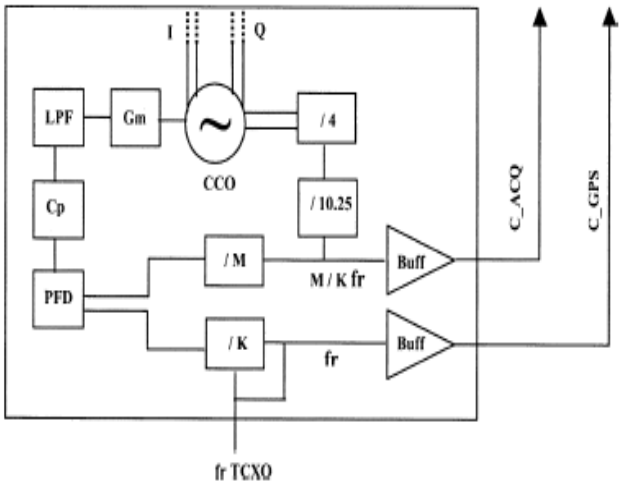

Fig-5 PLL Synthesizer

V. CMOS Mixer

Mixer mixes or multiplies two signals to get a resultant output signal. A time domain multiplication is a convolution in frequency domain so, in the transceiver, mixers perform frequency translation or frequency up-conversion and down-conversion by multiplying an RF input signal, with frequency wRF, and an LO signal, with frequency wLO, present at mixers the RF and the LO ports, respectively. the local oscillator is coupled to the center taps of the two transformers to control which pair of diodes is forward biased. The different mode of operation for the diode ring mixer in which the LO drive is transformer-coupled to the ring. In this case, a different pair of diodes is activated on each phase of the LO that couples the other transformer to the center taps of the two secondary. This connection is widely used when the RF and LO signals are at high frequencies and the IF output is at a relatively low frequency. Center tapping the IF port permits the use of smaller self inductances in the transformer secondary, which only need to present large impedances at the LO and RF frequencies. While diode ring mixers operate on a voltage switching principle, the Gilbert mixer operates on a current switching principle. The mixer employs two bipolar current switches whose outputs are connected in opposition. On one phase of the LO, the input current owes to the output through the outer pair of devices, while on the opposite phase, the input current is diverted to the opposite outputs via the inner pair of devices. If the bases of the transistors are driven symmetrically, the emitters lie at points of symmetry so that, in principle, no local oscillator signal couples to the input or output ports. So, just as in the diode ring case, the Gilbert mixer is nominally a double-balanced mixer.

VI. Conclusion

The vast majority of integrated GPS receivers use a standard super heterodyne architecture with a number of off-chip components, particularly passive IF filters. It was demonstrated how the detailed nature of the GPS signal spectrum presents an opportunity for a low-IF receiver architecture that offers the benefit of complete integration of the receiver signal path. Because the I/Q matching requirements are relaxed in this architecture, adequate image rejection is readily obtained without trimming or calibration. With the goal of minimum power consumption in mind, Beginning with the low-noise amplifier, Low noise operation in CMOS by including an oft-neglected noise source: induced gate noise. This power-constrained" optimization demonstrates that excellent noise performance can be achieved in CMOS with small numbers of milliwatts while delivering a good input impedance match to the off-chip 50 world. This theoretical development enables a 2.4dB noise figure for a differential LNA with only 4.9mA of bias current.

The double-balanced CMOS voltage mixer consumes exceptionally little power with no bias current required in the mixer core. Although conversion gain is a concern in

this architecture, a careful analysis demonstrates that higher conversion gains can be obtained by reactively terminating the IF port of the mixer. A noise figure analysis further demonstrated that SSB noise figures on the order of 6dB are easy to obtain. Finally, the linearity of the mixer is primarily limited by the magnitude of the LO drive. Thus, the CMOS voltage mixer achieves wide dynamic range and excellent noise figure with no static power consumption In the future, process scaling may necessitate a reduction in supply voltage for integrated radio receivers. This trend will present a number of challenges for wide dynamic range receiver design.

Acknowledgement:
This page maintains a list of contributor's names with short descriptions of their contributions to this website. Thanks to everyone for the valuable feedback.

Some of the content of this paper has been influenced by discussions with our colleagues from the EYES project, specifically, Thomas Lentsch, Michele Zorzi, and Paul Havinga; colleagues from FU Berlin, specifically Jochen Schiller and Hartmut Ritter; AdamWolisz; and AndreasWillig. This work has in part been sponsored by the IST EYES project.

VII. REFERENCES

- Aldert van der Ziel, Noise in Solid State Devices and Circuits, John Wiley & Sons, New York, 1986.
- A. Abidi, \High-frequency noise measurements on FET's with small dimensions,"IEEE Transactions on Electron Devices, vol. ED-33, no. 11, pp. 1801-1805, Nov. 1986.
- Norman G. Einspruch, Ed., VLSI Electronics: Microstructure Science, vol. 18, pp. 1{37, Academic Press, New York, 1989.
- Bradford W. Parkinson, \Introduction and heritage of NAVSTAR, the global positioning system," In Parkinson and Spilker [104], pp. 3-28.
- Guglielmo Marconi, \Radio telegraphy," Proceedings of the IRE, vol. 10, pp. 215-238, Aug. 1922.
- Thomas H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press, 1998.
- R. H. Marriott, United States radio development," Proceedings of the IRE, vol. 5, pp. 179-198, June 1917.
- Guglielmo Marconi, \Radio communication," Proceedings of the IRE, vol. 16, pp. 40-69, Jan. 1928.
- Michael Riordan and Lillian Hoddeson, Crystal Fire: The Birth of the Information Age, W. W. Norton & Company, 1997.
- Lee de Forest, \The audion {detector and amplifier," Proceedings of the IRE, vol. 2, pp. 15{36, Mar. 1914.
- Haraden Pratt, \Long range reception with combined crystal detector and audion amplifier," Proceedings of the IRE, vol. 3, pp. 173{183, June 1915.
- Edwin H. Armstrong, \Operating features of the audion," Electrical World, no. 24, pp. 1149{1152, Dec. 1914.
- John L. Hogan, Jr., \The heterodyne receiving system and notes on the recent Arlington-Salem tests," Proceedings of the IRE, vol. 1, pp. 75{97, July 1913.
- Benjamin Liebowitz, \The theory of heterodyne receivers," Proceedings of the IRE, vol. 3, pp. 185{204, Sept. 1915.
- Edwin H. Armstrong, \Some recent developments in the audion receiver," Proceedings of the IRE, vol. 3, pp. 215{247, Sept. 1915.