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Designing and Analysis of 8 Bit SRAM Cell with Low Subthreshold Leakage Power

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Abstract- The power consumption is major concern in Very Large Scale Integration (VLSI) circuit design and reduce the power dissipation is challenging job for low power designers. . International technology roadmap for semiconductors (ITRS) reports that "leakage power dissipation" may come to dominate total power consumption. The sub-threshold leakage power is the main reason to increase the leakage power. So there is some techniques to reduce this leakage power like sleep approach, stack & some new techniques like, sleepy–stack, leakage feedback approach and sleepy keeper techniques which reduces leakage current while saving exact logic state.

As the technology increases integration density of transistors increases, power consumption has become a major concern in today's processors and SoC designs. Considerable attention has been paid to the design of low power and high-performance SRAMs as they are critical components in both handheld devices and high performance processors.

In this paper we design 8 bit S-RAM by using the leakage current reduction techniques. The proposed circuits were designed in 0.18µm CMOS/VLSI technology with-in Micro-Wind tool, and measure power consumption for design approaches, and we achieves up to nearly 50% less power consumption than existing basic SRAM.

Key-words: **sub-threshold leakage power, sleep, stack, sleepy-stack keeper, Leakage Feedback.**

I. INTRODUCTION

Static RAMs are used extensively in modern processors as on chip memories due to their large storage density and small access latency. Low power on-chip memories have become the topic of substantial research as they can account for almost half of total CPU dissipation, even for extremely power-efficient designs. However, static power dissipation is becoming an significant fraction of the total power. Static power is the power dissipated in a design in the absence of any switching activity and is defined as the product of supply voltage and leakage current. The absolute and the relative contribution of leakage power to the total system power is expected to further increase in future technologies because of the exponential increase in leakage currents with technology scaling. The International Technology Roadmap for Semiconductors (ITRS) predicts that leakage power would contribute to 50% of the total power in the next generation processors.

Here we present some VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. In this paper SRAM cell was designed with each technique and analyze the power consumption in each technique.

II. LEAKAGE POWER REDUCTION TECHNIQUES

Here we proposed techniques in circuit level approaches for sub-threshold leakage power reduction. The
Most well-known traditional approach is the sleep approach [2][3]. In the sleep approach, both (i) an additional "sleep" PMOS transistor is placed between VDD and the pull-up network of a circuit and (ii) an additional "sleep" NMOS transistor is placed between the pull-down network and GND. These sleep transistors turn off the circuit by cutting off the power rails. Figure 1 shows its structure. The sleep transistors are turned on when the circuit is active and turned off when the circuit is idle. By cutting off the power source, this technique can reduce leakage power effectively.

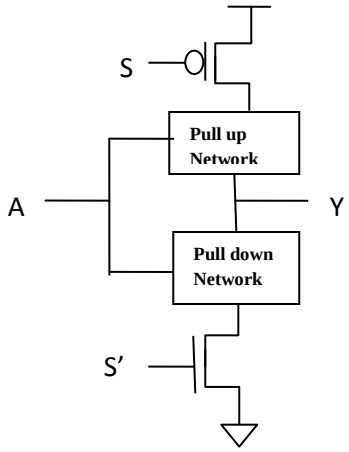

Fig.1 Sleepy approach.

Another technique for leakage power reduction is the stack approach, which forces a stack effect by breaking down an existing transistor into two half size transistors [5]. Figure 2 shows its structure. When the two transistors are turned off together, induced reverse bias between the two transistors results in subthreshold leakage current reduction. However, divided transistors increase delay significantly and could limit the usefulness of the approach.

The sleepy stack approach combines the sleep and stack approaches [6][7]. The sleepy stack technique divides existing transistors into two half size transistors like the stack approach. Then sleep transistors are added in parallel to one of the divided transistors. Figure 3 shows its structure. During sleep mode, sleep transistors are turned off and stacked transistors suppress leakage current while saving state. Each sleep transistor, placed in parallel to the one of the stacked transistors, reduces resistance of the path, so delay is decreased during active mode. However, area penalty is a significant matter for this approach since every transistor is replaced by three transistors and since additional wires are added for S and S', which are sleep signals.

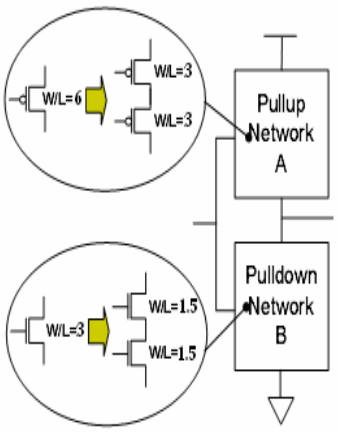

Fig.2 Stack approach

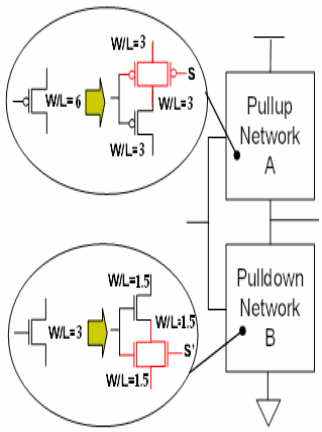

Fig.3 Sleepy Stack approach

The leakage feedback approach is based on the sleep approach. However, the leakage feedback approach uses two additional transistors to maintain logic state during sleep mode, and the two transistors are driven by the output of an inverter which is driven by output of the circuit implemented utilizing leakage feedback [17]. As shown in Figure 4, a PMOS transistor is placed in parallel to the sleep transistor (S) and a NMOS transistor is placed in parallel to the sleep transistor (S'). The two transistors are driven by the output of the inverter which is driven by the output of the circuit. During sleep mode, sleep transistors are turned off and one of the transistors in parallel to the sleep transistors keep the connection with the appropriate power rail.

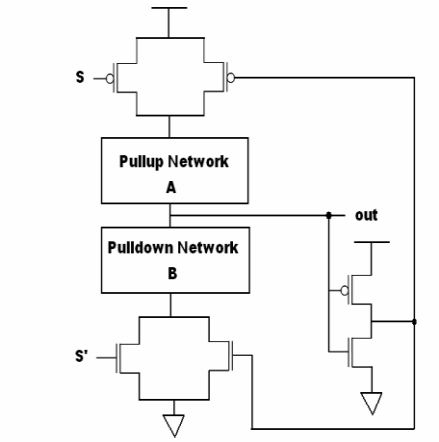

Fig.4 Leakage feedback approach.

For the sleep, zigzag, sleepy stack and leakage feedback approaches, dual Vth technology can be applied to obtain greater leakage power reduction. Since high-Vth results in less leakage but lowers performance, high-Vth is applied only to leakage reduction transistors, which are sleep transistors, and any transistors in parallel to the sleep transistors; on the other hand, low-Vth is applied to the remaining transistors to maintain logic performance [2]-[7].

III. MOTIVATION

The art of power analysis and optimization of integrated circuits used to be a specialty in analog circuit design. Power dissipation of VLSI chips is traditionally a neglected subject. In the past the device density and operating frequency were low enough that it was a constraining factor in the chips. As the technology varies, more transistors, faster and smaller than their predecessors, which leads to the growth in operating frequency and processing per capacity leads to increase in power consumption. There are two types of power dissipation in CMOS Circuits: Dynamic and Static. Dynamic power is caused by switching activities of the circuit and most significant source of dynamic power dissipation in CMOS circuits is the charging and discharging of the capacitance. Static Power dissipation is related to the logical states of the circuits rather than switching activities. In CMOS logic, leakage current is the only source of static power dissipation.

Currently, sub-threshold leakage seems to be the dominant contributor to overall leakage power. Another possible contributor to leakage power is gate-oxide leakage. A possible solution widely reported is the potential use of high k (high dielectric constant) gate insulators. In any case, this papers targets reduction of the sub-threshold leakage component of static power consumption; other approaches should be considered for reduction of gate oxide leakage. Do please note, however, that all results reported in this paper include all sources of leakage power. With application of dual threshold voltage (Vth) techniques, the sleep, zigzag and sleepy stack approaches result in orders of magnitude sub-threshold leakage power reduction.

IV. SRAM

Static Random Access Memory (SRAM) to be one of the most fundamental and vitally important memory technologies today. Because they are fast, robust, and easily manufactured in standard logic processes, they are nearly universally found on the same die with microcontrollers and microprocessors. Due to their higher speed SRAM based Cache memories and System-on-chips are commonly used. Due to device scaling there are several design challenges for nanometer SRAM design. Low power SRAM design is crucial since it takes a large fraction of total power and die area in high performance processors. A SRAM cell must meet the requirements for the operation in submicron/nano ranges. The scaling of CMOS technology has significant impacts on SRAM cell random fluctuation of electrical characteristics and substantial leakage current.

The schematic of SRAM cell is shown in the Fig.9. It has 2 pull up PMOS and 2 NMOS pull down transistors as two cross coupled inverters and two 2 NMOS access transistors to access the SRAM cell during Read and Write operations. Both the bit lines (BL and BLB) are used to transfer the data during the read and write operations in a differential manner. To have better noise margin, the data signal and its inverse is provided to BL and BLb respectively. The data is stored as two stable states, at storing points VR and VL, and denoted as 0 and 1.

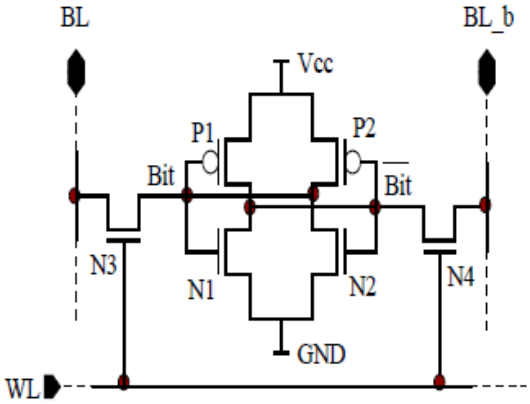

Fig.5 6T SRAM Cell

V. SIMULATION RESULTS

Here the SRAM cell is designed using all leakage power reduction techniques discussed earlier, namely stack, sleep, sleepy stack and leakage feedback approaches. Schematics and layouts are designed for all considered Techniques using Microwind.

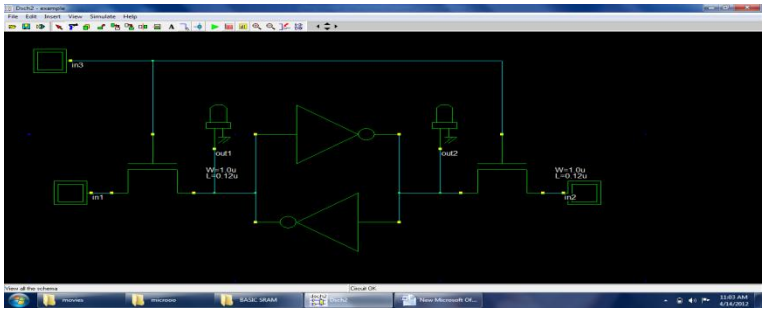

Fig 6: schematic for basic 6T SRAM cell

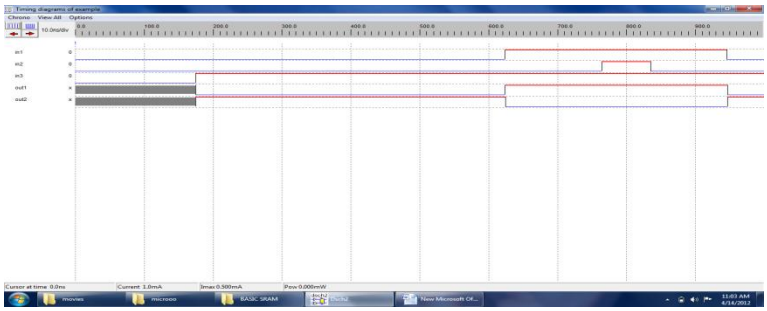

Fig 7: simulation results for basic 6T SRAM cell

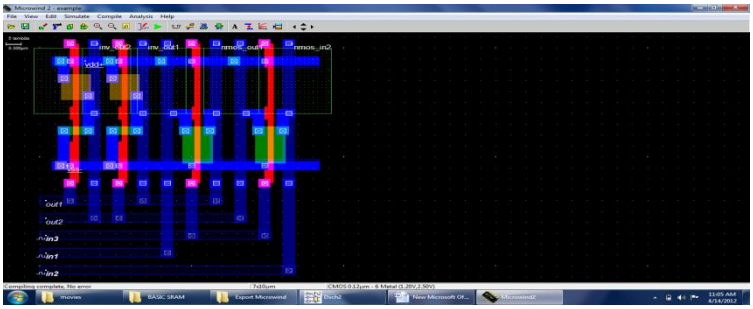

Fig 8: layout for basic 6T SRAM cell

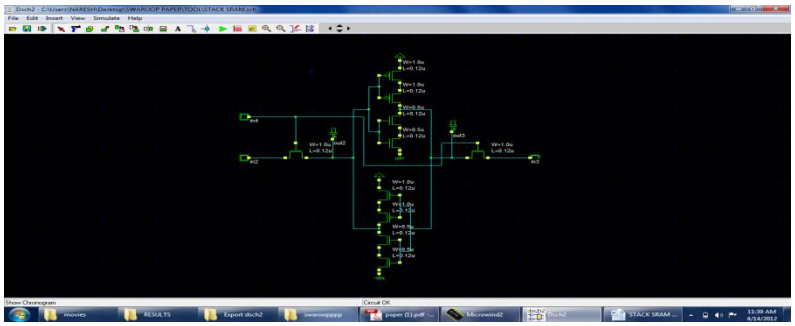

Fig 9: schematic for SRAM cell using stack approach

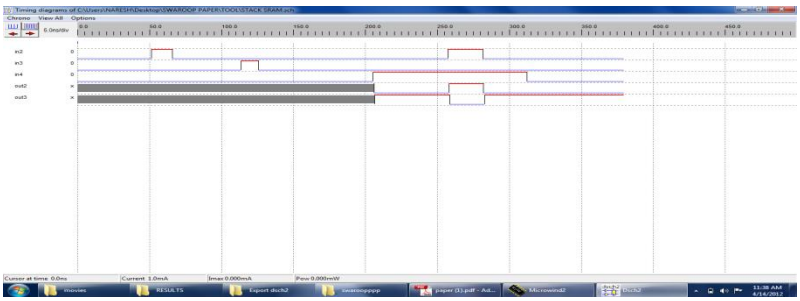

Fig 10: simulation results for SRAM cell using stack approach

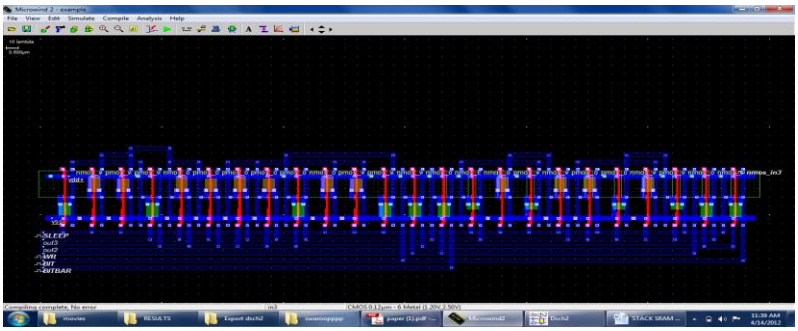

Fig 11: layout for SRAM cell using stack approach

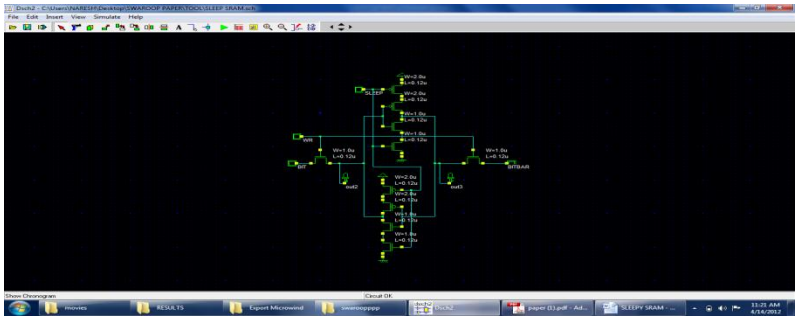

Fig 12: schematic for SRAM cell using sleepy approach

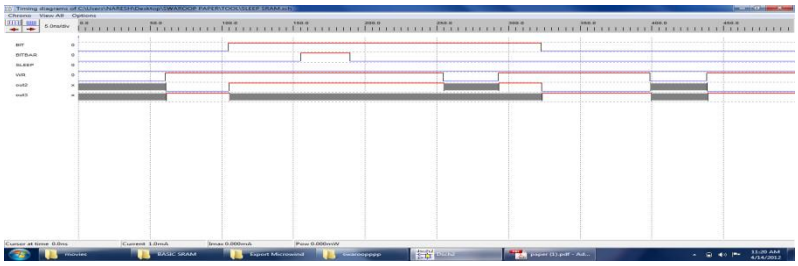

Fig 13: simulation results for SRAM cell using sleepy approach

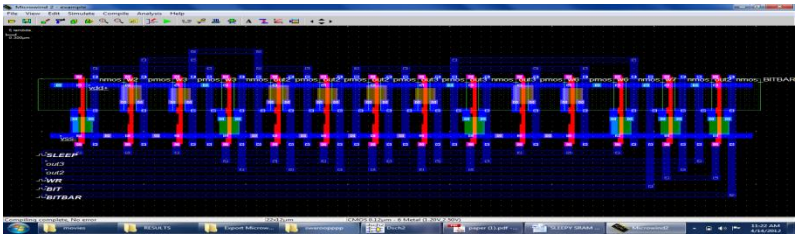

Fig 14: layout for SRAM cell using sleepy approach

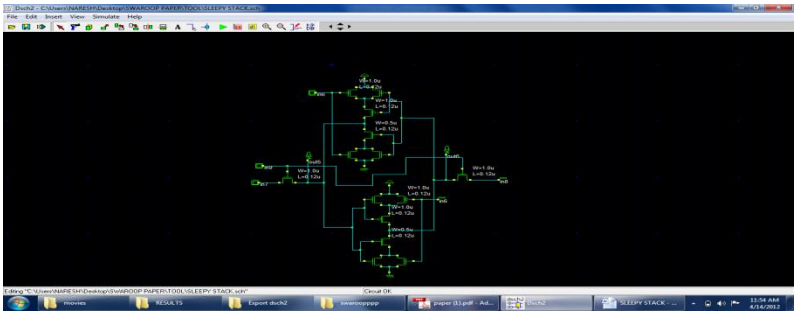

Fig 15: schematic for SRAM cell using sleepy stack approach

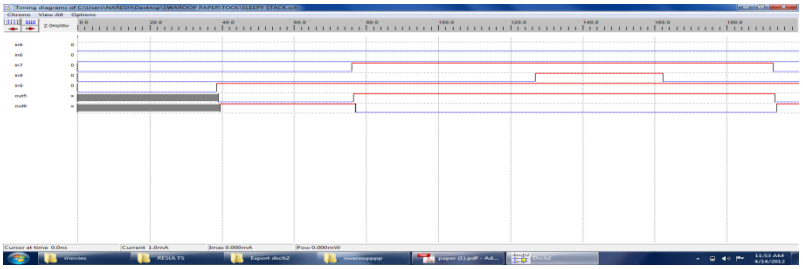

Fig 16: simulation results for SRAM cell using sleepy stack approach

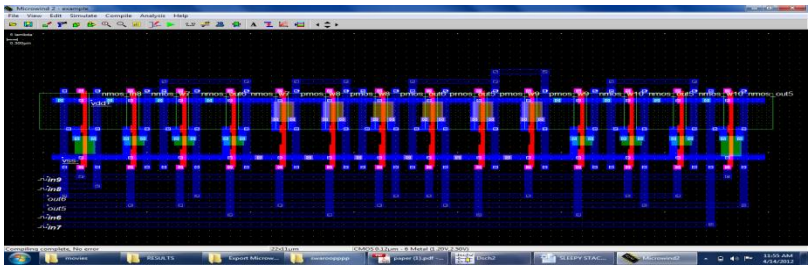

Fig 17: layout for SRAM cell using sleepy stack approach

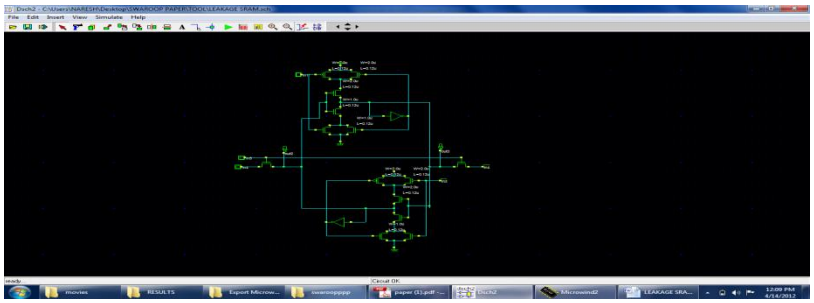

Fig 18: schematic for SRAM cell using leakage feedback approach

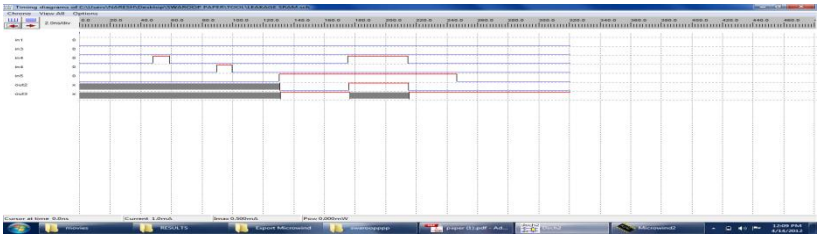

Fig 19: simulation results for SRAM cell using leakage feedback approach

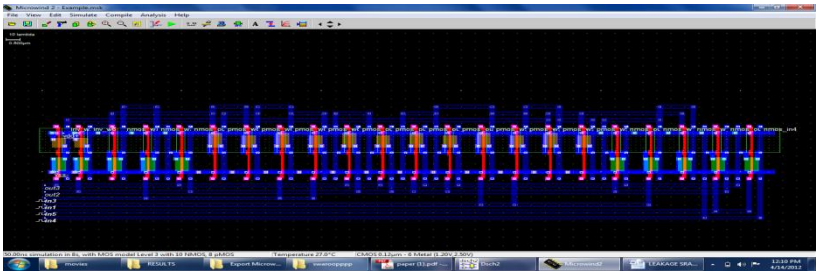

Fig 20: layout for SRAM cell using leakage feedback approach

Power dissipation analysis between Basic SRAM and SRAM using leakage power reduction technique

Topology	Basic SRAM (mw)	SRAM using STACK approach (mw)	SRAM using SLEEPY approach (mw)	SRAM using SLEEPY STACK approach (mw)	SRAM using LEAKAGE feedback approach (mw)	
180nm	10.2	0.26	0.11	0.15	10.2 E-03	
120nm	2.2	0.11	87.3 E-03	0.21	2.2 E-03	
90nm	1.2 E-03	74.6 E-03	57.6 E-03	73.4 E-03	1.2 E-03	
70nm	0.5 E-03	37.03 E-03	29.4 E-03	36.2 E-03	0.5 E-03	
50nm	0.15 E-03	8.9 E-03	7.15 E-03	8.8 E-03	0.15 E-03	

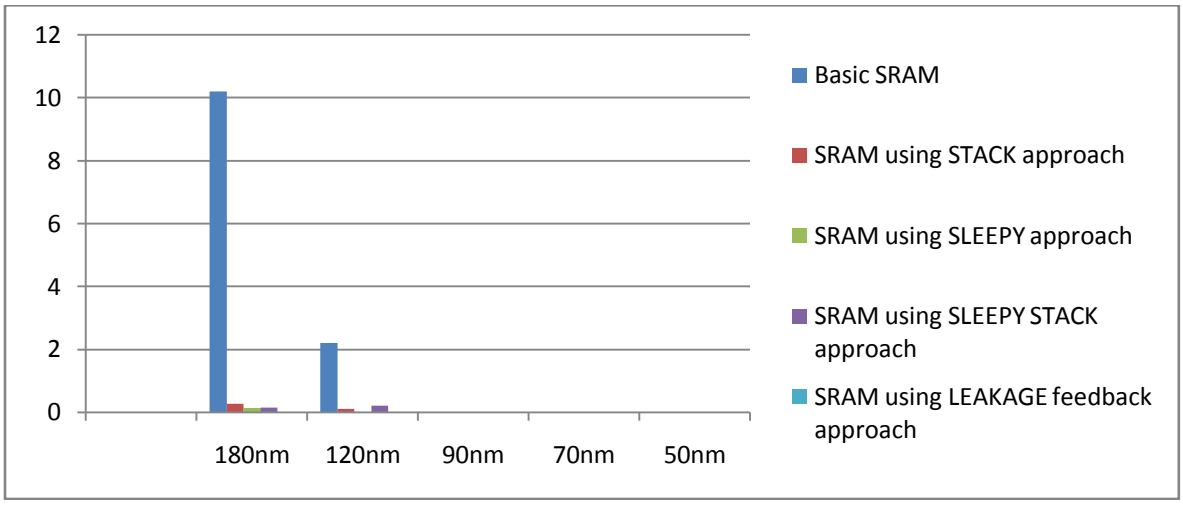

Fig 30: Power consumption graph for basic SRAM and SRAM using leakage power reduction techniques

VI. CONCLUSION

In this paper we designed SRAM cell using Leakage power reduction techniques to reduce sub-threshold leakage power. The proposed circuits were designed in 0.18um technology and analyze the power dissipation between proposed techniques. Here we observed that proposed techniques have low power consumption compared to basic circuit design and having delay and area overhead.

Based on the simulation results of SRAM cell, we observed that by using these techniques we can reduce nearly 50% of power dissipation compared to general SRAM cell. Hence it is concluded that the proposed SRAM Architecture is used for low power designs and these designed techniques are used for high performance and low power applications.

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