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Multilevel Converter for Ac–Dc Harmonic Immunity in VSC Hvdc Transmission

[1]Polisetty Hema Sundar, [2]Aswani Kumar Eedara
[1]*Mtech Student Scholar Department of Electrical and Electronics Engineering, SASI Inst. Of Technology and Engg. , Tadepalligudem, W.G.Dist., A.P, India.*
[2]*Head of the Dept. of Electrical & Electronics Engg., SASI Inst. of Technology and Engg. Tadepalligudem,W.G.Dist., A.P, India*
Email:[1]hemasundar10@gmail.com, [2]aswani@sasi.ac.in

Abstract: The concept of multilevel inverters, introduced about 20 years ago entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. The benefits are especially clear for medium-voltage drives in industrial applications and are being considered for future naval ship propulsion systems. Several topologies for multilevel inverters have been proposed over the years; the most popular cascaded H-bridge apart from other multilevel inverters is the capability of utilizing different dc voltages on the individual H-bridge cells which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher-frequency inverters. Control methods based on selective harmonic elimination pulse-width modulation (SHE-PWM) techniques offer the lowest possible number of switching transitions. This feature also results in the lowest possible level of converter switching losses. For this reason, they are very attractive techniques for the voltage-source-converter-(VSC) based high-voltage dc (HVDC) power transmission systems. The paper discusses optimized modulation patterns which offer controlled harmonic immunity between the ac and dc side. The application focuses on the conventional two-level converter when its dc-link voltage contains a mix of low-frequency harmonic components. Simulation and experimental results are presented to confirm the validity of the proposed switching patterns. Finally a five level Multilevel converter topology is applied for this application

Keywords-Amplitude modulation (AM), dc-ac power conversion, harmonic control, HVDC, insulated-gate bipolar transistor (IGBT), power electronics, power transmission system, pulse-width modulation, voltage-source converter (VSC)**.**

I. INTRODUCTION

The continuous growth of electricity demand and ever increasing society awareness of climate change issues directly affect the development of the electricity grid infrastructure. The utility industry faces continuous pressure to transform the way the electricity grid is managed and operated. On one hand, the diversity of supply aims to increase the energy mix and accommodate more and various sustainable energy sources. On the other hand, there is a clear need to improve the efficiency, reliability, energy security, and quality of supply.With the breadth of benefits that the smart grid can deliver, the improvements in technology capabilities, and the reduction in technology cost, investing in smart grid technologies has become a serious focus for utilities [1].

Advanced technologies, such as flexible alternating current transmission system (FACTS) and voltage-source converter (VSC)-based high-voltage dc (HVDC) power transmission systems, are essential for the restructuring of the power systems into more automated, electronically controlled smart grids. An overview of the recent advances of HVDC based on VSC technologies is offered in [2]. The most important control and modeling methods of VSC-based HVDC systems and the list of existing installations are also available in [2]

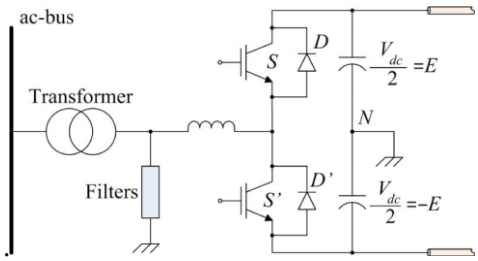

Fig. 1. Phase of the two-level VSC for the HVDC power transmission system[7].

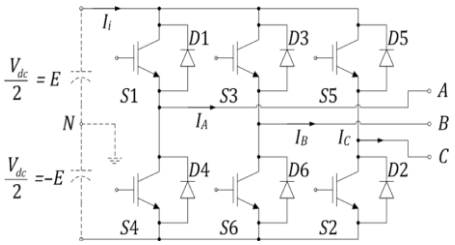

Fig. 2. Three-phase two-level VSC.

The first generation of utility power converters is based on current-source converter (CSC) topologies [3], [4]. Today, many projects still use CSCs due to their ultra-high power capabilities. With the invention of fully controlled power semiconductors, such as insulated-gate bipolar transistors (IGBTs) and integrated gate-commutated thyristors (IGCTs) [5], the VSC topologies are more attractive due to their four-quadrant power-flow characteristics [6]. A typical configuration of the VSC-based HVDC power transmission system is shown in Fig. 1 as it is shown in [7] and [8].

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual

power devices. Among the multilevel Converters [1-4], the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels.

Additionally, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than alternative multilevel converters. The multilevel voltage source inverter is recently applied in many industrial applications such as ac power supplies, static VAR compensators, drive systems, etc. One of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency or decreasing the inverter power output [5-11]. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltage sources. The so-called multilevel starts from three levels. As the number of levels reach infinity, the output THD approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems voltage clamping requirement, circuit layout, and packaging constraints.

On the other hand, optimized modulation methods offer many advantages toward tight control of converter-generated harmonics [19]. A minimization method to find the complete set of solutions by solving the SHE-PWM equations for two-level inverters is discussed in [20]. In this paper, the dc-link voltage is assumed to be constant. In [10], a method is proposed to prevent the dc-link ripple voltage from creating low-order harmonics on the ac side of fixed and variable frequency inverters. However, only one of the multiple SHE-PWM sets [20] of solutions is reported.

An investigation of the harmonic interaction between the ac and dc side for STATCOM is presented in [21] including the so-called dynamic SHE-PWM scheme based on precalculated angles for better THD. However, the dynamic SHE-PWM scheme is applied only for a three-level converter and can be applied only for known magnitude and frequency of the ripple. Another method for improving the harmonic performance of a two-level VSC with SHE-PWM is studied in [22]. However, only one set of SHE-PWM solutions is considered for the method of [22] which requires the exact values of magnitude, phase, and frequency of the ripple in order to be implemented.

Control strategies to compensate unbalances are reported in the literature. Mild imbalances caused by unbalanced loads of the ac side are regulated by using separate control loops for the positive- and negative-sequence components of the voltage as proposed in [23]. Efficient control of unbalanced compensator currents can be achieved by a control algorithm based on the D-STATCOM model [24]. D-STATCOM allows separate control of positive- and negative-sequence currents and decoupled current control of the d-q frame. An advanced strategy based on direct power control under unbalanced grid voltage conditions has been recently presented for a doubly fed induction generator [25]. To take the full advantages of VSCs for HVDC power transmission systems, an auxiliary controller is added to the main controller which is conventionally implemented in the positive-sequence d-q frame [26]. To compensate for unbalanced ac-side loads, the auxiliary controller is implemented in the negative-sequence d-q frame.

The objective of this paper is to discuss the effectiveness of optimized modulation based on precalculated SHE-PWM in a two-level three-phase VSC to make the ac side immune from the fluctuations of the dc link without the use of passive components. However, since the VSC studied here does not include a closed-loop controller, strategies to compensate unbalances are not addressed in this paper.

This paper is organized in the following way. In Section II, a brief analysis of the VSC and the modulation method is provided. Section III contains the characteristics of the method on a VSC with dc-side ripple voltage. Section IV provides extensive experimental results to support the theoretical arguments. Conclusions are documented in Section V.

II. Analysis Of The Pwm Converter And She-Pwm

The optimized SHE-PWM technique is investigated on a two level three-phase VSC topology with IGBT technology, shown in Fig. 2. A typical periodic two-level SHE-PWM waveform is shown in Fig. 3.

The waveforms of the line-to-neutral voltages can be expressed as follows:

$$V_{LN} = \begin{bmatrix} V_{AN} \\ V_{BN} \\ V_{CN} \end{bmatrix} = V_{dc} \begin{bmatrix} \sum_{n=1}^{\infty} A_n \sin n\omega_0 t \\ \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t - \frac{2\pi}{3}\right) \\ \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t + \frac{2\pi}{3}\right) \end{bmatrix} \quad (1)$$

When ω_0 is the operating frequency of the ac, and V_{dc} is the dc-link voltage.

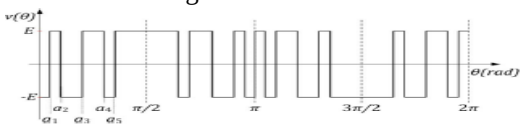

Fig. 3. Typical two-level PWM switching waveform with five angles perquarter cycle.

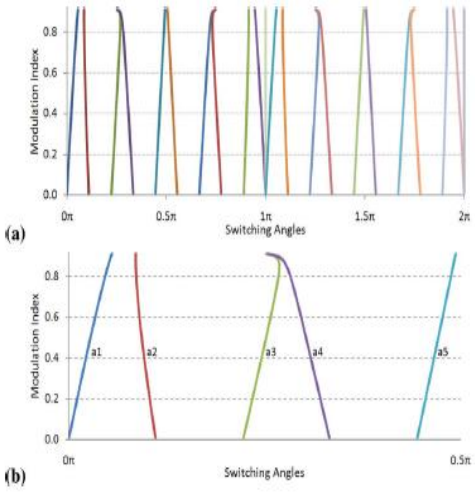

Fig. 4. Solution trajectories. (a) Per-unit modulation index over a complete periodic cycle. (b) Five angles in radians.

Thus, the line-to-line voltages are given by

$$V_{LL} = \begin{bmatrix} V_{AB} \\ V_{BC} \\ V_{CA} \end{bmatrix} = \sqrt{3}.V_{dc} \begin{bmatrix} \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t + \frac{\pi}{6}\right) \\ \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t - \frac{\pi}{2}\right) \\ \sum_{n=1}^{\infty} A_n \sin n\left(\omega_0 t + \frac{5\pi}{6}\right) \end{bmatrix} \quad (2)$$

The SHE-PWM method offers numerical solutions which are calculated through the Fourier series expansion [20] of the waveform

$$M = 1 + 2 \sum_{i=1,2,3...}^{N+1} (-1)^i \cos(\alpha_i)$$
$$0 = 1 + 2 \sum_{i=1,2,3...}^{N+1} (-1)^i \cos(k\alpha_i) \quad (3)$$

Where N+1 are the angles that need to be found.

Using five switching angles per quarter-wave in (N=4)SHE-PWM, k= 5, 7, 11, 13 to eliminate the 5th, 7th, 11th,and 13th harmonics. During the case of a balanced load, the third and all other harmonics that are multiples of three are cancelled, due to the 120 symmetry of the switching function of the three-phase converter. The even harmonics are cancelled due to the half-wave quarter-wave symmetry of the angles, being constrained by

$$0 < \alpha_1 < \alpha_2 \ldots\ldots < \alpha_{N+1} < \pi/2$$

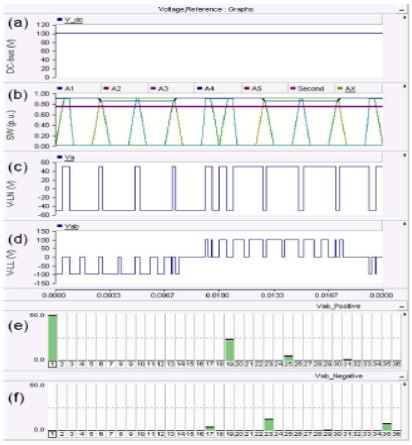

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Fig. 5. Simulation results for SHE-PWM eliminating 5th, 7th, 11th, and 13th harmonics. (a) DC-link voltage. (b) Solution trajectories to eliminate harmonics and intersection points with the modulating signal (M=0.75). (c) Line-to-neutral voltage. (d) Line-to-line voltage. (e) and (f) Positive- and negative-sequence line-to-line voltage spectra, respectively.

III. Cascaded H-Bridge Multilevel Converter

2.1 Full H-Bridge

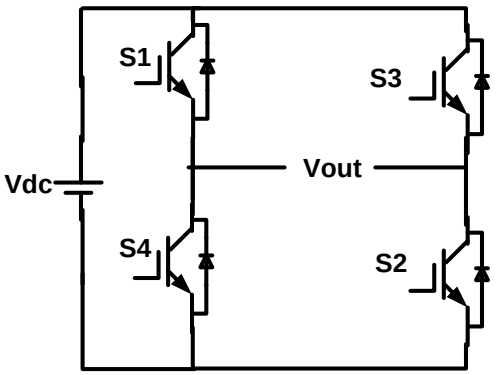

Figure. 6 Full H-Bridge

Switches Turn ON	Voltage Level
S1,S2	Vdc
S3,S4	-Vdc
S4,D2	0

Table 1. Switching table for H-Bridge

Fig.6 shows the Full H-Bridge Configuration. By using single H-Bridge we can get 3 voltage levels. The number output voltage levels of cascaded Full H-Bridge are given by 2n+1 and voltage step of each level is given by Vdc/n. Where n is number of H-bridges connected in cascaded. The switching table is given in Table 1 and 2.

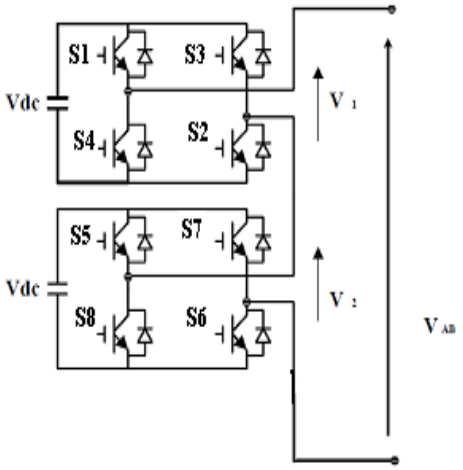

Table 2. Switching table for Cascaded H-Bridge

Switches Turn On	Voltage Level
S1, S2	Vdc
S1,S2,S5,S6	2Vdc
S4,D2,S8,D6	0
S3,S4	-Vdc
S3,S4,S7,S8	-2Vdc

IV. SIMULATION RESULTS

4.1 Modeling of Cascaded H-Bridge Multilevel Converter

Fig.7 shows the Matlab/Simulink Model of five level Cascaded H-Bridge multilevel converter. Each H-bridge DC voltage is 50 V. In order to generate three phase output such legs are connected in star/delta. Each llege gating pulses are displaced by 120 degrees.

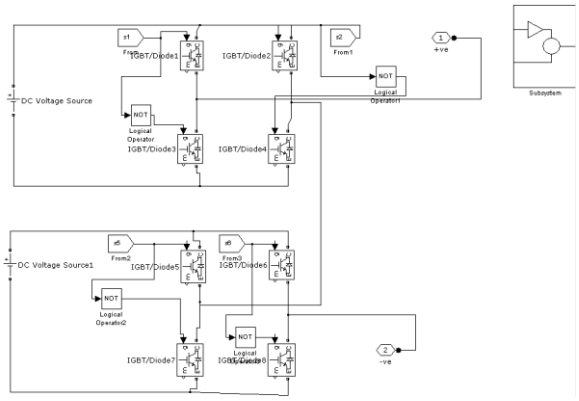

Figure. 7 Matlab/SImulink Model of CHB

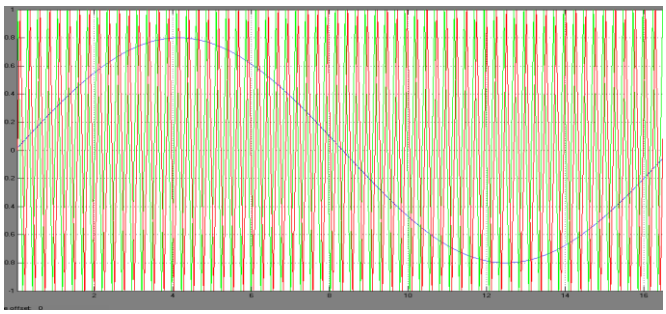

Figure. 8 Carrier Signals of Phase Shifted Carrier PWM

Fig.8 shows the Phase shifted Carrier PWM wave form. Here four carriers each are phase shifted by 90 degrees are compared with sine wave.

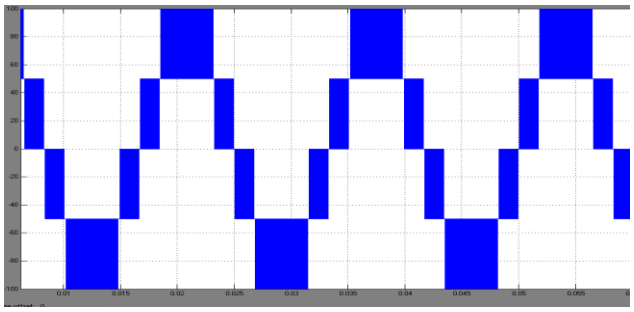

Figure. 9 Five Level output

Fig.9 shows the phase voltage of phase shifted carrier PWM CHB inverter. Fig.10 shows the line voltage of phase shifted carrier PWM CHB inverter. Here phase voltage has five voltage levels where as line voltage has nine voltage levels.

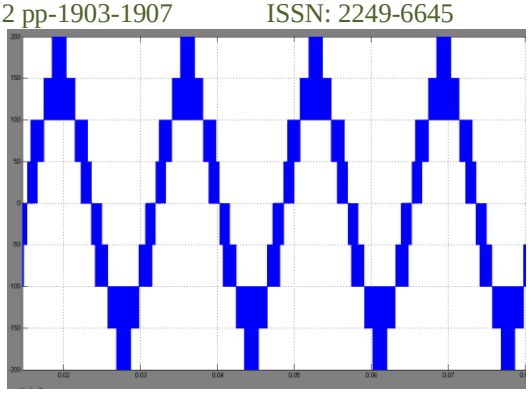

Figure. 10 Nine Level Line Voltage

Fig.10 shows the Level shifted Carrier PWM wave form. Here four carriers each are level shifted by 0.5 in positive and negative side are compared with sine wave.

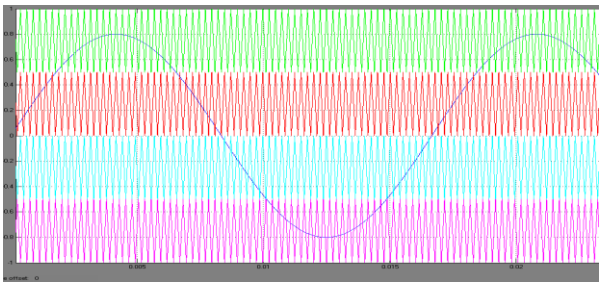

Figure. 11 Carrier Signals of Level Shifted PWM

Fig.11 shows the phase voltage of level shifted carrier PWM CHB inverter. Fig.12&13 shows the phase and line voltage of level shifted carrier PWM CHB inverter. Here phase voltage has five voltage levels where as line voltage has nine voltage levels.

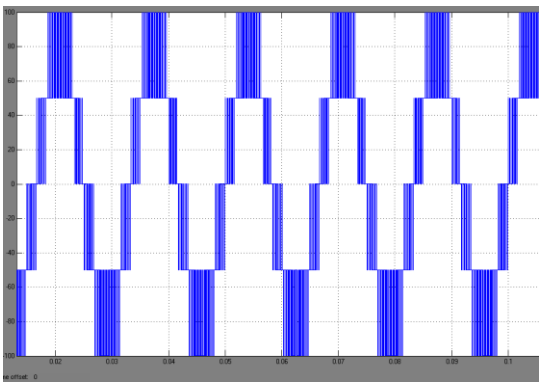

Figure. 12 Five Level Phase Voltage

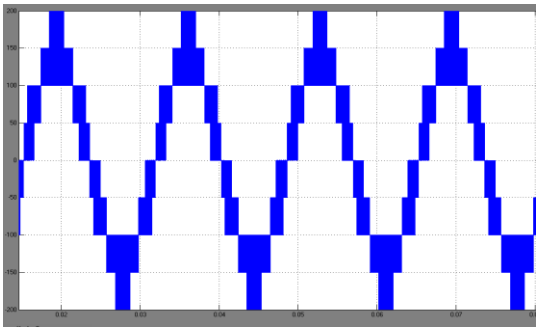

Figure. 13 Nine Level Line Voltage

V. CONCLUSIONS

This paper presents Novel Hybrid H-Bridge multilevel converter. The proposed converter produces more voltage levels with less number of switches compared to H- bridge configuration. This will reduce number of gate drivers and protection circuits which in turn reduces the cost and complexity of the circuit. Finally a five level single H-bridge is proposed. A SIMULINK based model is developed and Simulation results are presented.

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P. HEMA SUNDAR, pursuing M.Tech in SASI institute of Technology and Engineering with the specialization Power Electronics. I completed my under graduation in the stream of Electrical and Electronics Engineering in SASI institute of Technology and Engineering, Tadepalligudem, Andhra Pradesh. My areas of intrest are Power Electronic drive systems, Harmonic studies in power systems.

ASWANI KUMAR EEDARA received the B.Tech. degree in Electrical and Electronics Engineering from the JNTU college of Engineering Hyderabad, India in 2005 and the M.E. degree in Power Systems from the University College of Engineering Osmania university Hyderabad in 2008.He worked as Project Trainee at GE-consumer and Industrial Hyderabad for one year. He has been on the faculty of SASI Institute of Technology and Engineering at Tadepalligudem as an Assistant Professor in Department of Electrical and Electronics Engineering Since 2008.He has been working as Head of the Department of E.E.E. since MAY 2012. He is member of IAENG .He has one international journal publication. He is presently doing his research in the area of Power Electronics applications in Power systems at JNTUK.His areas of interest are FACTS Controllers, Evolutionary algorithms, Modeling and simulation of Power Electronics and Power Systems.