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A Survey of Power Management in Embedded System Using Transistor Sizing

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ABSTRACT: *This paper describes a transistor sizing methodology for both analog and digital CMOS circuits. Various techniques are used for power optimization in CMOS VLSI circuits. Transistor sizing is one of the important techniques for the determination of circuit performance. The aim of the power optimization is to minimize the power and power-delay product or the energy consumption of the circuit. Thus, the main purpose of transistor sizing in CMOS VLSI circuits is to obtain the minimum power dissipation under certain performance requirements. Transistor sizing is based on different algorithms. Analysis is based on some simulation parameter like No. of transistors, power, delay, power delay product, different technologies, aspect ratio. Each of these circuits cell exhibits different power consumption, delay and area in different VLSI technology. This survey paper discusses the different algorithms for transistor sizing analog and digital CMOS circuits and that will be beneficial for the circuit designers.*

Key-Words: *Algorithm, Delay, Low Power, Optimization, Transistor sizing.*

I. INTRODUCTION

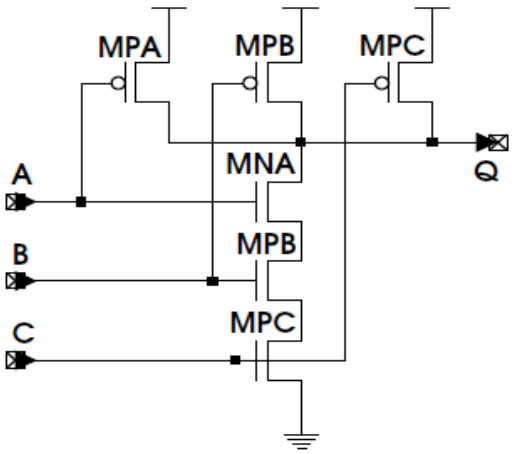
Transistor size optimization is a traditional obligation in VLSI (Very Large Scale Integration) design. It is used to improve the performance of a circuit to achieve a design goal in a specific technology. This design goal can either be boosting operating speed, lowering power consumptions or lowering area requirements. Design of VLSI circuits involves tradeoff between high speed (low delay) and low power. Design requires optimum balance between delay and power, in smaller constituent circuits and also in the larger circuit. This can be achieved by careful iterative optimization of transistor sizes. In this paper, the net list of the circuit is determined by adjusting the length and width of the MOS transistors. The figure of merit depends in a complex way on the individual size of the transistors. Changing transistor sizes in a circuit often leads to surprising results, which are not easily predicted in the low power design embedded system design.

The different algorithms have been presented for transistor sizing. The reminder of the paper is organized as follows. In section [2.1] the Monte Carlo and Genetic algorithm optimize the three digital CMOS circuits and in section [2.2] annealing and ACM compact model are discussed. Then after a simple declaration of Genetic Algorithm on consuming energy for basic arithmetic circuits, the Genetic circuit optimizer is proposed in section [2.3]. In section [2.4] optimisation techniques using geometric programming are discussed. Comparison of different transistor sizing analog and digital CMOS circuits performance and results are shown in section [3] and the conclusion is presented in section [4].

II. LITERATURE SURVEY

2.1 MONTE CARLO AND GENETIC ALGORITHM

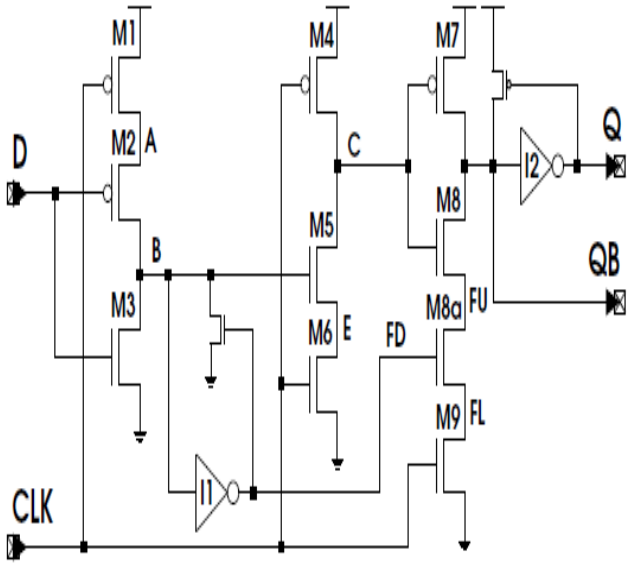
This paper [1] presents the Schoastic methods for transistor size optimization of CMOS analog and digital circuits. The performance of CMOS circuits depends on transistor sizes. The transistor sizes of digital circuits are optimized using Monte Carlo and Genetic Algorithm (GA), and also comparison is done between the two algorithms. GA is found to be more effective for larger circuits while for smaller circuits Monte Carlo optimization performs better than GA. Even nowadays, GA is one of the most used algorithms for optimization problem. This paper reviews three techniques a standard optimizer, a Monte Carlo scheme and a method based on genetic algorithms combined with very accurate spice simulations to automatically optimize transistor sizes of three digital CMOS circuits as three input NAND gate, Dynamic edge triggered DFF, Complementary pass gate full adder (CPLFA). This paper improves the performance to achieve a design goal. This design goal can either be boosting operating speed, lowering power consumption or lowering area requirements.



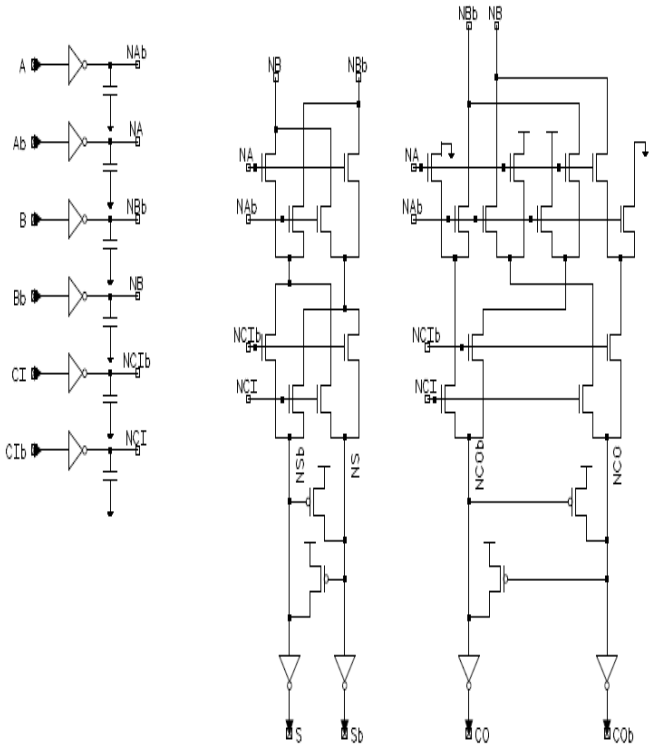
"Fig 1" 3-Input CMOS NAND Gate

The Monte Carlo algorithm used in this paper results in minimum duration because the step size is first set to four times the minimum feature size and then to twice the minimum feature size and the minimum for the last third. The genetic algorithm is based on ranking selection, uniform cross over and the optimal mutation rate. In this paper the optimization of transistor sizes can be accurately performed by stochastic optimization. The paper compared

four stochastic optimization methods on three CMOS subcircuits of different complexity (6, 16, 64 MOSFETS).



"Fig 2" Dynamic Edge triggered DFF

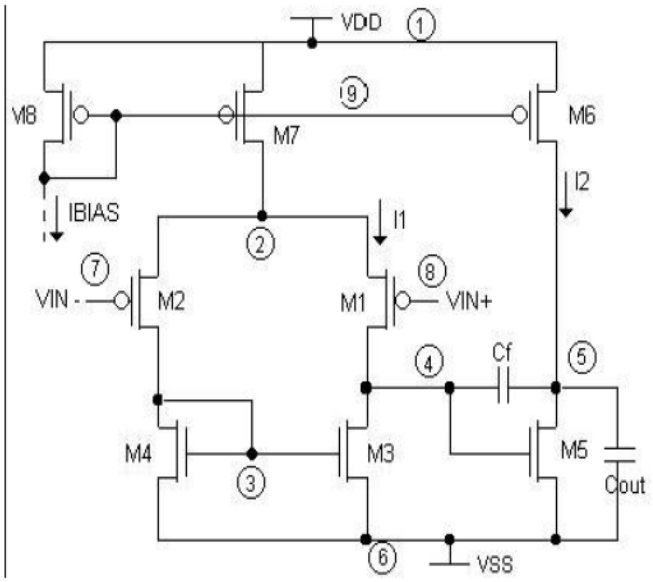


"Fig 3" Complementary Pass Gate Full Adder (CPLFA)

On the smaller two subcircuits, the Monte Carlo method has been found to yield better results than the genetic algorithms investigated. On the largest of the three circuits, the genetic algorithms were found to yield significantly smaller variances provided they were allowed to run for a significant number of generations which suggests that the monte carlo methods tends to end up in a suboptimal solution more frequently as problem size increases.

2.2. ANNEALING AND ACM COMPACT MODEL

The paper [2] described a transistor sizing methodology for analog CMOS circuits that combines the physics-based *gm*/*ID* characteristics provided by the ACM compact model and the simulated annealing technique for the circuit optimization. This methodology exploits different transistor widths and lengths and provides good solutions in a reasonable CPU time, with a single technology dependent curve and accurate expressions for transconductance and current in all operation regions. The advantage of constraining the optimization within a power budget is of great importance for the designer. The optimization results obtained for the design of a two-stage operational amplifier. This paper discussed a methodology for analog design automation that combines the simulated annealing optimization technique, a physics-based transconductance to- current ratio characteristics and the electrical simulation. The



"Fig 4" Schematics of a two-stage operational amplifier

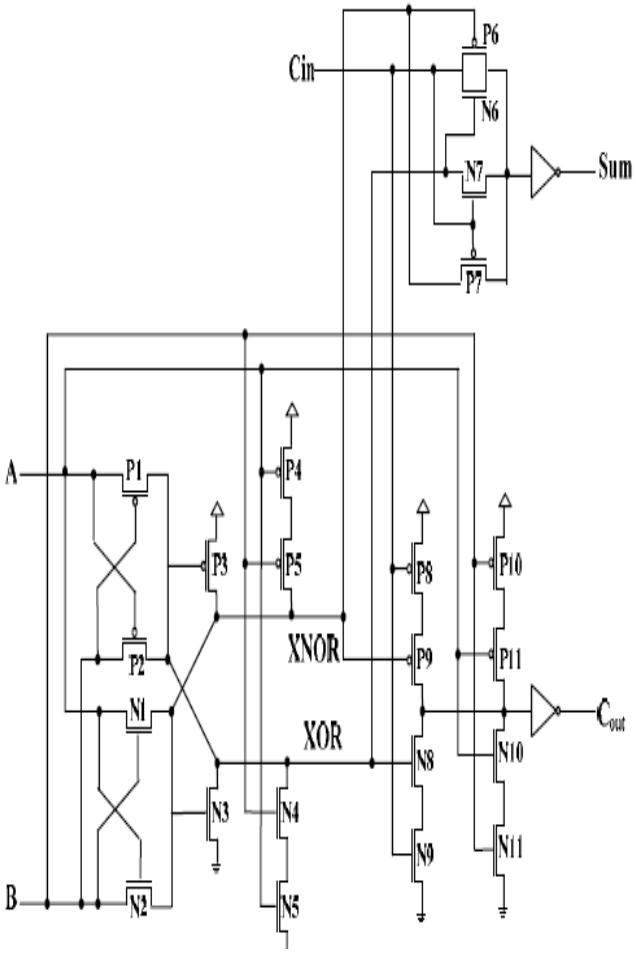
Synthesis of a two-stage operational amplifier is shown in order to demonstrate the capabilities of the methodology. The paper describes simulated annealing process in which metal cools and freezes into a minimum energy crystalline structure. This algorithm employs a random search which does not only accept solutions that decrease the objective cost function fc but also some changes that increase it. This paper exploits different transistor lengths and provides an acceptable solution in a reasonable CPU time. It is a simple sizing method based on transistor inversion coefficient which is calculated by curve gm/ID versus I.

2.3. BASED ON GENETIC ALGORITHM

In this paper, transistor sizing is very important for determination of the circuit performance. This paper [3] is based on the methodology of genetic algorithm for energy consumption optimization. Simulation results in this paper show that, compared with the hybrid tree structure, the GA transistor sizing exhibits better simplicity, initial values, independency, optimization parameter independence and short runtime. The average improvement in PDD is 7% for

XOR/XNOR circuits and 17% for full adder. In this technique, all the circuits are simulated using Hspice circuit simulated based on two techniques 0.13um and 0.18um based on BS1M3V and TSMC model.

The main objective of annealing and compact model is to minimize the power delay product on the energy consumption. The energy consumption was optimized. The transistor size run time is reduced by using Genetic algorithm in transistor sizing optimization. Finally compared

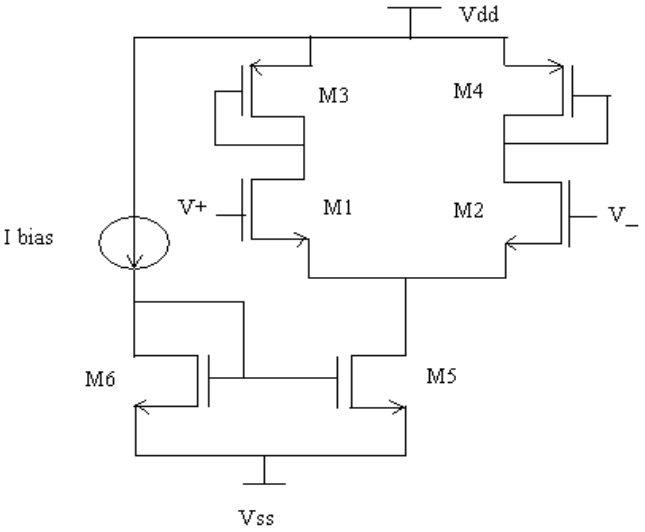


"Fig 5" The New HPSC Full adder

to the hybrid tree structure algorithm, the PDP characteristics are improved by 7% in XOR/XNOR circuit and 17% in full adder for the supply voltage range of 0.6 to 0.2 V. The saving in PDP increases in the larger circuit.

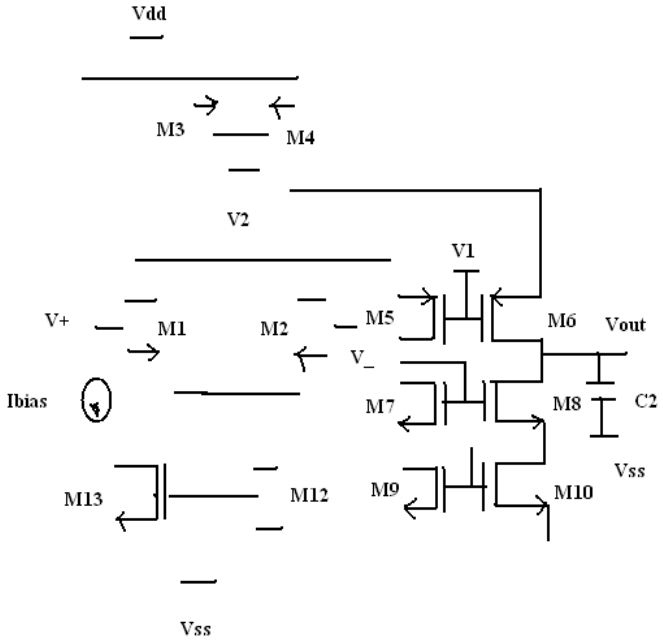
2.4. OPTIMIZATION USING GEOMETRIC PROGRAMMING

This paper describes a design of folded cascade operational amplifier with power optimization using geometric programming. The basic idea of the folded-cascode operational amplifier is to apply cascode operational amplifier transistors to the input differential pair. In this study, the main concepts of power optimization using geometric programming are introduced. Geometric Programming, a method for optimizing and automating component and transistor sizing will apply to the power optimization of Folded Cascode operational amplifier. The simulation of the folded cascode circuit is done using TSPICE simulation tool and 0.035 μm CMOS technology is used. Design of the circuit and simulation results are presented demonstrating the amplifier power optimization. In this paper we introduced a new method, geometric programming, for determining the component values and transistor dimensions for CMOS op-amps. The method handles a wide variety of specifications and constraints, is extremely fast, and results in globally optimal designs.



"Fig 6" Differential amplifier with cascade arrangement

This paper describes geometric programming, for circuit sizing and optimization. Initially our work describes the design of differential amplifier with cascade arrangement and then the design of folded-cascode operational amplifier. The simulation folded cascode op-amp circuit is done using TSPICE simulation tool and the T-spice parameters are mentioned.



"Fig 7" Folded Cascode operational amplifier

Simulated result shows that this op amp exhibits the average power is 1.007X10-13 that is 100 fW or 0.1 nW operating at 100 KHz frequency. The Geometric Programming is successfully applied and the optimized

average power is obtained 9.0658X10-14 that is 90 fW or 0.09 nW operating at 100 KHz frequency.

"Table 1" Comparison of different transistor sizing analog and digital CMOS circuits

S.No	Transistor Sizing	Algorithm	Circuit	Technology	Power	Run time	No of Transistors
1.	Robert Rogenmoser, Hubert Kaeslin, Tobias Blickle in 1996	Schoastic Monte Carlo and genetic algorithm	NAND3 DFF CPLFA	1.0µm 1.0µm 0.6µm	3.0 5.8 36.7	Less	6 12 26
2.	Alessandro Girandi and Sergio Bampi in 2006	Annealing and ACM compact model	OPAMP	0.35µm	-	More	8
3.	M. Grailoo, T. Nikoubin, K. Navi in 2009	Genetic algorithm	HPSC Full adder (XOR/XNOR gate)	0.13µm 0.18µm	0.406 1.292	More	18
4.	Amol W. Pardhi and Dr.A.Y. Deshmukh in 2012	Geometric programming	Folded cascode operational amplifier	0.035µm CMOS	$9.0658x\ 10^{-14}$	Less	12

III. CONCLUSION

Transistor sizing is an effective technology for reducing the power, delay in the analog and digital CMOS circuits of an embedded system. In this way different technique such as genetic algorithm, geometric programming, Monte Carlo algorithm are reviewed and compared the performance from the most recent published research work. Different algorithms are discussed to reduce the size of the transistors in which genetic algorithm is more efficient and it leads to better circuit performance in the case of power consumptions. The size of the transistor size is reduced under 180º and further proceeding should be carried our below 100º. By using the analysis of different algorithms the low power circuit can be implemented in embedded system.

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