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# Ring-Oscillator-Based Injection-Locked Frequency Divider with Vernier Method

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***Abstract:*** *Frequency synthesizers are one of the most critical blocks for multi-standard multi-band systems. This paper presents a low power and wide locking range Injection frequency divider. Ring-oscillator-based injection-locked frequency divider has merits of compact and low power devices. Two injection-locked frequency dividers, with divide-by-3 and divide-by-5 operations respectively, were simulated by TSMC 0.18 µm CMOS technology to verify the proposed design. The locked ranges of divide-by-3 and divide-by-5 are 1.9 GHz and 1.4 GHz, with 0.25mw and 0.93mw power consumption at 1 V supply voltage, respectively.*

***Keywords:*** *Differential injection, frequency divider, ring oscillator, wide tuning range, low power, Vernier.*

## I. INTRODUCTION

A frequency divider is widely used for quadrature signal generators and high frequency systems such as frequency synthesizers. The inductance/capacitance (LC) resonator-based injection-locked frequency divider (ILFD) [1] is widely used because of high frequency operation. However, its locking range is generally narrow. In the recent years, the ILFDs have attracted much attention due to their high frequency and lower power consumption [2, 3]. The ILFDs are based on the injection-locked oscillators. There are two types of ILFDs. The former is LC-oscillator-based ILFD, which can operate at very high frequency with low power consumption, but its locking range is narrow and the area is too large due to the LC tank. The latter type of ILFD can be based on RC ring oscillator, which has the merits of low power, large locked range, and small area. In the last years, lots of researchers have focused on ring-oscillator-based ILFDs [2–4]. Ref. [4] and [5] both demonstrated that multi-phase injection with a specific phase difference can maximize the locking range of the ring-oscillator-based ILFD. Ring oscillators, on the other hand, occupy extremely small area. In addition, they generally have a larger locking range because of their lower quality factor (Q). Although the phase noise of traditional ring oscillators is high, the noise performance improves dramatically when locked to a clean reference. A drawback is that, in general the exact multi-phase inputs are difficult to be obtained directly in conventional LC differential voltage-controlled oscillator (VCO). In addition, the locking range will become worse if the phase difference of inputs departs from the optimum value [6]. We use single injection instead of multi-phase injection in this paper to achieve a wide locked range for ring oscillator frequency divider.

## II. BACKGROUND

As multi-standard multi-band systems emerge in today wireless market, one of the most critical blocks to be realized is the frequency synthesizer, which at least must satisfy two main criteria: operating over a wide range of frequencies and low power consumption. Locking of injection based oscillator is a well- known and deeply studied phenomenon. When an external signal is applied to an oscillator, the oscillator stops to be an autonomous circuit and synchronizes to the external signal. The conditions under which this phenomenon happens have been deeply investigated by Adler in 1946 [7], and by many other authors [8, 9]. Consider the conceptual block of a free-running oscillator shown in Fig. 1(a): it consist of a gain block $f(v_o)$ and a linear filter h(t). The Barkausen's amplitude and phase criteria define the conditions under which the oscillation can be sustained at a given frequency ω. Those conditions are presented by denoting:

$$|F(\omega)\,H(\omega)| = 1 \qquad (1)$$

$$\angle F(\omega)\,H(\omega) = 2\pi \qquad (2)$$

Where F (ω) and H(ω) are the transfer function of the filter and the gain block respectively. Suppose that the gain block is capable to set its gain in such a way which (1) can be satisfied at any frequency, then, oscillation happens at the frequency, $\omega_0$, where the phase of the filter satisfies (2). $\omega_0$ is the oscillator's natural frequency, which is the oscillation frequency of the oscillator when any external signal is applied to it.

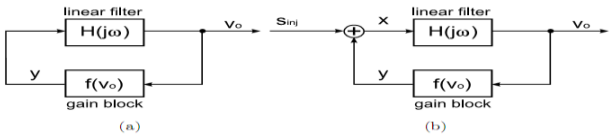



Figure 1: (a) Block diagram of a free-running oscillator. (b)Block diagram of an injection locked oscillator.

As illustrate in Fig. 1(b), the external signal $s_{inj}$ at frequency $\omega_{inj}$ is applied to the oscillator. The signal X that feeds the linear filter is sum of the feedback signal Y and the injection signal $s_{inj}$. Then the total phase shift across the loop at $\omega_0$ is not any longer $2\pi$, because of the extra phase shift introduced by $s_{inj}$, and the oscillation cannot be sustained at that frequency. However, under particular conditions the phase response of the filter at the frequency $\omega_{inj}$ compensates this extra phase shift and the Barkhausen's phase criterion is satisfied at $\omega_{inj}$, instead of $\omega_0$. It is said that the oscillator is injection locked by $s_{inj}$ and its oscillation frequency moves from the natural frequency $\omega_0$ to the injection frequency $\omega_{inj}$ [7, 10]. The range of frequencies $\omega_0 \pm \omega_L$ where synchronization occurs defines the locking range of the oscillator. $\omega_L$ depends on the strength of the injecting signal $s_{inj}$, and the selectivity of filter, it's usually results in a small fraction of $\omega_0$.

## III. DESIGN CONSIDERATIONS OF THE ILFD

The design consideration of the ILFD includes the operating frequency, power consumption and locking range. The operating frequency of the ILFD is set by the speed of both blocks, the injector and the frequency selective block. Ring-oscillator-based ILFDs (Ring-ILFDs) feature wide locking ranges, small silicon area and large division module [3-11]. Ring-ILFDs' operation frequencies are mainly depend on the dimension of the devices and the power consumption. Although the phase noise of the conventional ring-oscillator is poor, the noise performance of ring-ILFDs can be further improved by injecting a clean signal [9]. In order to widen the locking range, to overcome process, voltage, and temperature (PVT) variations, the multiple-input injection technique for Ring-ILFDs with even division ratios has been proposed in [5] and [8]. However, the locking range of Ring-ILFDs with odd division ratios can rarely overcome the PVT variations. Usually when the number of ring-oscillator stages increases, the locking range becomes smaller severely [12]. Since low division ratios can decrease the speed and power in the following building blocks, to widen the locking range of large odd-division-module Ring-ILFDs still desired.

For conventional single-phase injection, the locking range of the ILFD is narrow since the extra phase shift around the loop is generated by only one injection. For multi-phase injection, the extra phase shift can be provided by multiple injection currents. The locking range of this ILFD will be widened if the phase of the injections progress with the ring oscillator's intrinsic delays. However, as mentioned previously, the requirement of specific multi-phase inputs makes this technique impractical in low power application [13]. We analyse the proposed divide-by-3 ILFD, as shown in Fig. 2, to demonstrate the base of our idea. The concept of this prototype can be applied to other ring-oscillator-based ILFDs. Each node $v_i$(i =1, 2, 3) is connected to every other node in the ring oscillator through an injection transistor to form a symmetrical injection circuit.

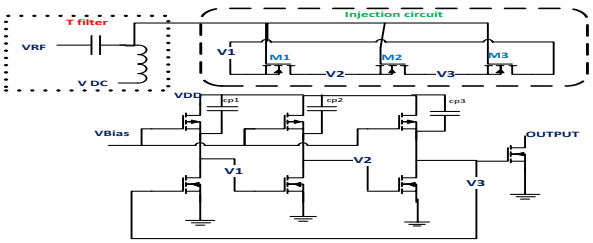



Figure 2: Schematic of proposed divide-by-3 ILFD

RF signal apply to $V_{inj}$ node by T filter block, where all gate injection transistors ($M_i$) connected there. Bias voltage ($V_{DC}$) is necessary for injection circuit driver. Bias Tee used for this work, salience that must said elevate of quality bias tee circuit. In this schematic DC voltage ($V_{Bias}$) is used for inverter stage PMOS gate bias; this node can be used for control of frequency operation. $C_{PI}$ represents the parasitic capacitance in the node $V_I$. In the qualitative analysis, the injection transistor can be treated as a mixer. Assume that the injection voltage is introduced as:

$$V_{inj} = V_{dc} + A_{inj}\, cos(\omega_{inj} + \theta_{inj}) \quad (3)$$

Where and are the dc voltage, amplitude, and phase of injection signal, respectively. The voltage at each oscillation node $V_i$ ($i$=1, 2, 3) in Fig. 2 is $cos(\omega t + \theta_i)$, where $\theta_i = (i-1)(2\pi/3)$, is angle of $2\pi/3$ with different $i$. Thus, the injection current (generated by $M_i$ through mixing) can be described as:

$$I_{inj,i} = \sum_{m=0}^{\infty} \sum_{n=0}^{\infty} a_{mn} \cos(m\omega_{inj} t + m\theta_{inj}) \times \cos(n\omega t + n\theta_{ds,i}) \quad (4)$$

Where is an intermediation transconductance coefficient of the mixer, and in the case of divide-by-3? We have considered only the fundamental current because other harmonics will be suppressed by the intrinsic low-pass filter in the loop of ring oscillator, so the fundamental current is. For simplicity, only the terms with $m$=0, n=1 and $m$=1, $n$=2, 4, are taken into consideration. Therefore, Eq. (4) expanded as:

$$I_{inj,i} = \frac{a_{01}}{2}\cos(\omega t + \theta_{ds,i}) + \frac{a_{12}}{2}\cos(\omega t + \theta_{inj} - 2\theta_{ds,i}) + \frac{a_{14}}{2}\cos(\omega t - \theta_{inj} + 4\theta_{ds,i}). \quad (5)$$

For each in Eq. (5), the parameters, and are the same, and only is different. , and have the same amplitude and form the angle of with each other. To simplify the qualitative analysis, we assume that the current flows from drain to source. The total current injected into the node $V_i$ will be

$$\left|I_{inj\ \_tot\ ,i}\right| = \sqrt{3}\left|I_{inj\ ,i}\right| (6)$$

Where the angle between each$I_{inj\ _tot\ ,i}$ is also$\frac{2\pi}{3}$. Therefore, the phase of the total injection currents progress with the intrinsic phase in the ILFD.

Fortunately, the number of injection transistors in our proposed *N*-stage ILFD is *N (N-1)/2*, which increases rapidly with *N*. Therefore, even while the division ratio is large, the injection efficiency will not degrade severely since much more currents can be injected into the ILFD.

We assume that the injection current$I_{inj\ ,i}$ is much smaller than the oscillation current,$I_{osc\ ,i}$ . By using the same method in [13], the one-sided locking range for our proposed divide-by-3 ILFD at the fundamental frequency can be derived as:

$$\frac{\Delta\omega}{\omega_0} \leq 4\left|\frac{I_{inj}}{I_{osc}}\right| . \left(1 - 3\left|\frac{I_{inj}}{I_{osc}}\right|^2\right)^{\frac{-1}{2}} (7)$$

In addition we have substituted the NMOS transistors in Fig.2 which is proposed by Yi et al [13], with Vernier inverter circuit. The resultant circuit scheme is the same as fig. 2 for divide-by-3 frequency dividers. For the divide-by-5 frequency divider, the circuit scheme is like fig. 3. The proposed circuit is faster than the circuit which is proposed in [13].

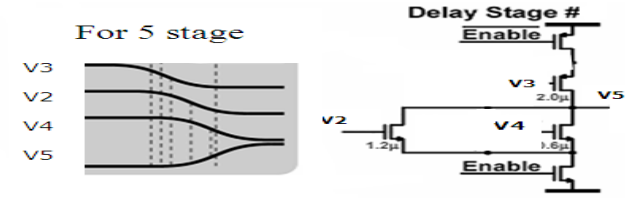
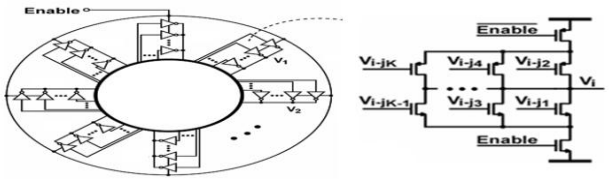



Figure 3: Vernier method inverter

Vernier method is usually used for designing high-speed oscillator. The frequencies that can be achieved by this method increase by increasing the number of successive stages (vernier) of the ring oscillator. This is noteworthy that the increase performance of the proposed method is optimized for more than 3 stage rings; in other words in the higher frequencies application, this way is better than other methods. Fig. 4 show this method, we applied signals from outputs of before stages to input of current inverter stage that increase speed of rising and falling time in vernier inverter, such as Fig.4(b). As demonstrated in Fig. 4(a), loop of several inverter stages considered as ring oscillator.




(a) (b)

Figure 4: Schematic of frequency divider using Vernier method.

## IV. SIMULATION RESULTS

Two circuits, three and five stage of vernier ring as illustrated in Fig.2 and Fig. 4(b), have been designed and simulated by TSMC 0.18 µm CMOS technology. Fig. 4(b) demonstrated schematic of inverter with more than one input from vernier method.

In both ILFDs, the single-end delay cell is designed as a NMOS inverter with a PMOS current-source load. A simple open-drain NMOS inverter is used for the output buffer. Note that the bodies of all NMOS (PMOS) transistors are connected to ground (VDD). The external bias voltages of PMOS load, $V_{Bias}$, is used to tune ILFD's free running frequency. To realize a large modulation conductance of injection transistors, the DC voltage of injection signal, $V_{DC}$, is set to 0.3 V as the optimize value. The supply voltage $V_{DD}$ is set to 1V, and can be further reduced to 0.8 V.

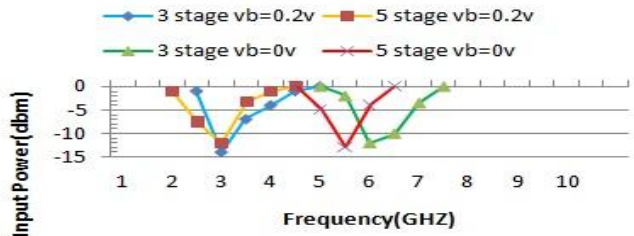



Figure 5: Measured input sensitivity of proposed ILFDs

The input sensitivity (that is very mainstay at quality of L and C input filter) of divide-by-3 ILFD and divide-by-5 ILFD operating at 1 V supply voltage are depicted in Fig. 5. When $V_{Bias}$=0 V, the locking frequency is from 5.6 to 7.5 GHz and the power consumption is 0.25 mw for divide-by-3 ILFD.

In divide-by-5 ILFD, thanks to the 10 injection transistors, its locking frequency is from 5 to 6.4 GHz and the power consumption is 0.93 mw while VDD =1V. Table 1 illustrated the results in different proposed ILFDs.

FOM is maximum operating frequency/ power [2] which is a good criterion for comparing oscillators. The higher FOM shows the better performance of an oscillator. We have calculated the FOM for several proposed methods in the literature. These results are shown in table 1. The results illustrate that our proposed scheme has the best FOM.

Table1. Comparsion results with other RC ILFDs in CMOS technology.

| Ref. | Tech. µm | VDD (v) | Div. Ratio | Locking Freq. (GHz) | Power (mw) | FOM* (GHz/mw) |
|---|---|---|---|---|---|---|
| ***[6]*** | 0.18 | 1.0 | 3 | 2.51-3.50 | 0.4 | 8.75 |
| ***[7]*** | 0.18 | 1.8 | 3 | 4.85-5.7 | 12.51 | 0.46 |
| ***[8]*** | 0.18 | 1.8 | 3 | 8.28-11.4 | 12.5 | 0.92 |
| ***[9]*** | 0.18 | 1.8 | 3 | 1.2-4.9 | 0.74 | 6.62 |
| | 0.18 | 1.8 | 7 | 1.4-4.4 | 0.88 | 5 |
| ***[10]*** | 0.065 | 1.2 | 7 | 4.1-5.1 | 0.516 | 9.88 |
| ***[11]*** | 0.13 | 1.5 | 3 | 24-30.8 | 13 | 2.27 |
| ***This work*** | 0.18 | 1 | 3 | 5.6-7.5 | 0.25 | 30 |
| | 0.18 | 1 | 5 | 5-6.4 | 0.93 | 6.88 |

## V. CONCLUSION

In this paper, we improve the locking range in conventional single-phase injection ILFD by introducing symmetrical injection structure. Analysis reveals that the proposed design can realize multi-phase injection with only single-phase input. Two ILFDs, with division ratio of 3 and 5, respectively, were designed and simulation to verify our analysis. Measurement results show that our design can achieve a reasonable performance with low power and small area due to absence of inductors in our design. The locked ranges of divide-by-3 and divide-by-5 dividers are 1.9 GHz and 1.4 GHz, while dissipating 0.25mw and 0.93mw at 1 V supply voltage, respectively.

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