International Journal of Modern Engineering Research (IJMER)
www.ijmer.com Vol.3, Issue.1, Jan-Feb. 2013 pp-530-537 ISSN: 2249-6645

Modelling and Simulation of High Step up Dc-Dc Converter for Micro Grid Application

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Abstract: *The distributed generation (DG) systems based on the renewable energy sources have rapidly developed in recent years. These DG systems are powered by micro sources such as fuel cells, photovoltaic (PV) systems, and batteries. The micro grid concept consists of two stages, in the first stage the low level voltage from the pv cell is converted to high level voltage by using DC-DC converter. In the second stage the high level DC voltage is converted into AC voltage by using an inverter and is supplied to load. This paper proposes a novel High Step-up DC-DC converter for micro grid application. The proposed converter is modelled and simulated along with pv cell and inverter through MATLAB/SIMULINK for AC load. The proposed converter has high voltage gain and efficiency. The results are successfully verified.*

Keyword: *Coupled inductor, distributed generation (DG) system, high step-up, Multilevel Inverter, Cascaded H Bridge multilevel inverter***.**

I. Introduction

Distributed generation (DG) systems based on renewable energy sources (RES) have experienced a fast development in recent years. With more DG units being integrated into the power system, a recent concept, called microgrid, is developed by grouping a cluster of loads and parallel DG units in a local area. The microgrid can operate in grid-connected mode or autonomous islanding mode and benefits both the utility and customers in terms of efficiency, reliability and power quality.

Each DG system has an energy source and a storage system, a grid-interfacing voltage source inverter (VSI) and output LC filters. In the grid-connected operation, the microgrid is connected to the grid at the point of common coupling (PCC) through a static transfer switch (STS), and each DG unit generates proper real and reactive power (according to the dispatched references or from the maximum power point tracking). In islanding operation, the DG units continue to supply power to the microgrid loads and they should be able to share the total load demand according to their respective ratings.

Numerous industrial applications have begun to require higher power apparatus in recent years. Some medium voltage motor drives and utility applications require medium voltage and megawatt power level. For a medium voltage grid, it is troublesome to connect only one power semiconductor switch directly. As a result, a multilevel power converter structure has been introduced as an alternative in high power and medium voltage situations. A multilevel converter not only achieves high power ratings, but also enables the use of renewable energy sources and drive applications.

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classic semiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. Among the multilevel Converters, the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels.

These converter topologies can generate high-quality voltage waveforms with power semiconductor switches operating at a frequency near the fundamental [5]. Although, in low-power applications, the switching frequency of the power switches is not restricted, a low switching frequency can increase the efficiency of the converter. Additionally, multilevel converters feature several dc links, making possible the independent voltage controls.

In this paper, a load-connected PV power system with high voltage gain is proposed. The steady-state model analysis and the control strategy of the system are presented. The load connected PV system includes two power-processing stages: a high step-up ZVT-interleaved boost converter for boosting a low voltage of PV array up to the high dc-bus voltage, which is not less than load side voltage level; and a multilevel inverter for inverting the dc current into a sinusoidal waveform synchronized with the utility system.

The distributed generation (DG) systems based on the renewable energy sources have rapidly developed in recent years [1], [2]. These DG systems are powered by micro sources such as fuel cells, photovoltaic (PV) systems, and batteries [3]–[7]. Fig. 1 shows a PV distributed system in which the solar source is low dc input voltage. PV sources can also connect in series to obtain sufficient dc voltage for generating actuality voltage; however, it is difficult to realize a series connection of the PV source without incurring a shadow effect [8], [9].high step-up DC-DC converters are generally used as the front end converters to step from low voltage (12–40 v) up to high voltage (380–400 v) [10]. High step-up DC-DC converters are required to have a large conversion ratio, high efficiency, and small volume.

This paper proposes a high efficiency, high step-up voltage gain, and clamp-mode converter and applied to load with the help of multilevel inverter. The proposed converter adds two pairs of additional capacitors and diodes to achieve high step-up voltage gain. The coupled inductor is used as both a forward and fly back type; thus, the two capacitors can be charged in parallel and discharged in series via the coupled inductor. The transit current does not flow through the main switch compared with earlier studies. Thus, the proposed converter has low conduction loss. Additionally, this converter

allows significant weight and volume reduction compared with other converters. Another benefit is that the voltage stresses on the main switch and output diode are reduced. However, the leakage inductor of the coupled inductor may cause high power loss and voltage spike. Thus, a passive clamping circuit is needed to recycle the leakage-inductor energy of the coupled inductor and to clamp the voltage across the main switch. The reverse-recovery problems in the diodes are alleviated, and thus, high efficiency can be achieved.

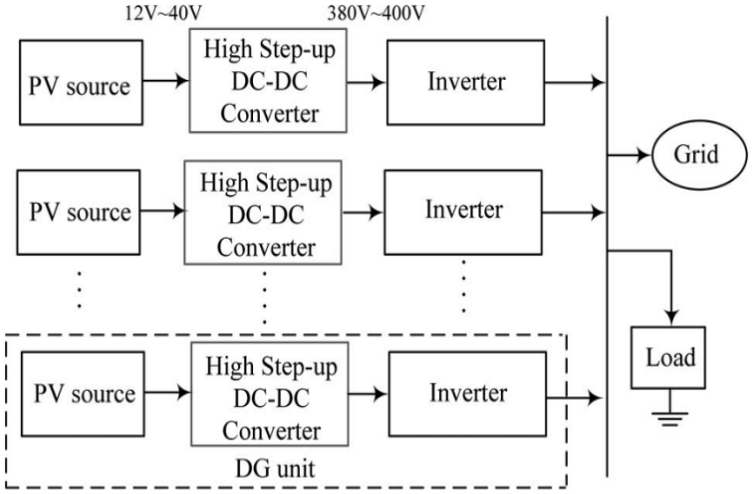


Fig. 1. PV distributed system

II. Proposed Converter

Fig. 2 shows the circuit topology of the proposed converter. This converter consists of dc input voltage V_{in} , power switch S, coupled inductors N_p and N_s, one clamp diode D_1, clamp capacitor C_1 , two blocking capacitors C_2 and C_3, two blocking diodes D2 and D3 , output diode Do, and output capacitor C_0. The coupled inductor is modeled as the magnetizing inductor L_m and leakage inductor L_k. To simplify the circuit analysis, the following conditions are assumed.

1) Capacitors C_2, C_3, and C_0 are large enough that V_{c2}, V_{c3}, and V_0 are considered to be constant in one switching period.
2) The power MOSFET and diodes are treated as ideal, but the parasitic capacitor of the power switch is considered.
3) The coupling coefficient of coupled inductor k is equal to $L_m/(L_m+L_k)$ and the turns ratio of coupled inductor n is equal to N_s/N_p.

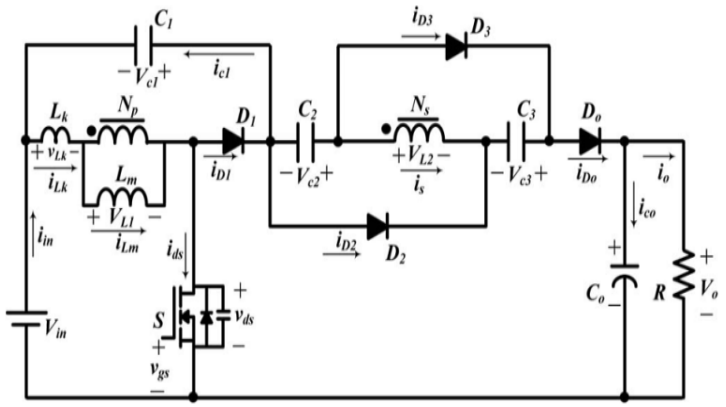


Fig. 2. Circuit configure of the proposed converter.

A. Continuous-Conduction Mode (CCM) Operation

1) Mode I [t_0, t_1]: During this time interval, S is turned on. Diodes D_1, D_2, and D_3 are turned off, and D_0 is turned on. The current-flow path is shown in Fig.3. The primary-side current of the coupled inductor i_{Lk} is increased linearly. The magnetizing inductor Lm stores its energy from dc source V_{in}. Due to the leakage inductor L_k, the secondary-side current of the coupled inductor i is decreased linearly. The voltage across the secondary side winding of the coupled inductor V_{L2}, and blocking voltages V_{c2} and V_{c3} are connected in series to charge the output capacitor Co and to provide the energy to the load R. When the current is becomes zero, dc source V_{in} begins to charge capacitors C_2 and C_3 via the coupled inductor. When i_{lk} is equal to i_{Lm} at t= t_1, this operating mode ends.

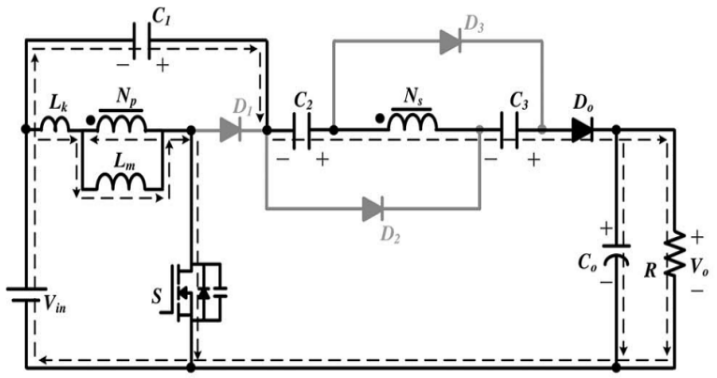


Fig.3. Current flowing path of Mode-I during one switching period at CCM operation.

2) Mode II [t_1, t_2]: During this time interval, S is still turned on. Diodes D_1 and D_0 are turned off, and D_2 and D_3 are turned on. The current-flow path is shown in Fig. 4. The magnetizing inductor L_m is stored energy from dc source V_{in}. Some of the energy from DC source V_{in} transfers to the secondary side of the coupled inductor to charge the capacitors C_2 and C_3. Voltages V_{c2} and V_{c3} are approximately equal to nV_{in}. Output capacitor C_0 provides the energy to load R. This operating mode ends when switch S is turned off at $t = t_2$.

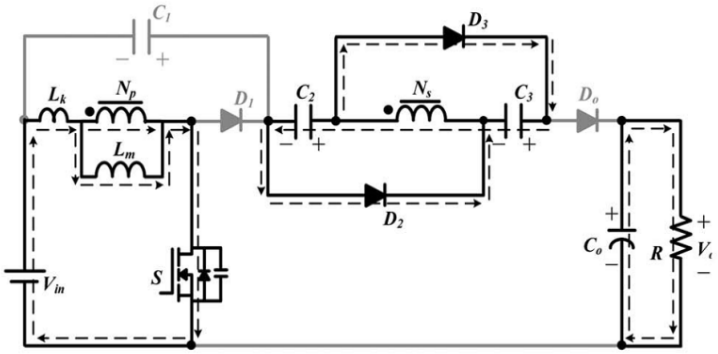


Fig.4. Current flowing path of Mode-II during one switching period at CCM operation.

3) Mode III [t_2, t_3]: During this time interval, S is turned off. Diodes D_1 and D_0 are turned off, and D_2 and D_3 are turned on. The current-flow path is shown in Fig. 5. The energies of leakage inductor L_k and magnetizing inductor L_m are released to the parasitic capacitor C_{ds} of switch S. The capacitors C_2 and C_3 are still charged by the DC source V_{in} via the coupled inductor. The output capacitor C_0 provides energy to load R. When the capacitor voltage $V_{in}+V_{ds}$ is equal to V_{c1} at $t = t_3$, diode D_1 conducts and this operating mode ends.

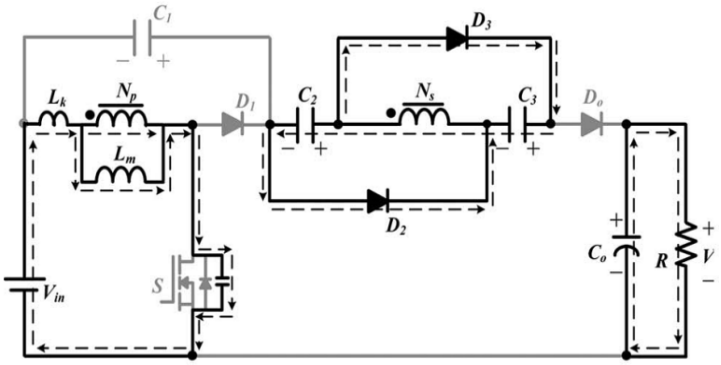


Fig.5. Current flowing path of Mode-III during one switching period at CCM operation.

4) Mode IV [t_3, t_4]: During this time interval, S is turned off. Diodes D_1, D_2, and D_3 are turned on and D_0 is turned off. The current-flow path is shown in Fig.6. The energies of leakage inductor L_k and magnetizing inductor L_m are released to the clamp capacitor C_1. Some of the energy stored in L_m starts to release to capacitors C_2 and C_3 in parallel via the coupled inductor until secondary current is equals to zero. Meanwhile, current i_{Lk} is decreased quickly. Thus, diodes D_2 and D_3 are cut off at $t = t_4$, and this operating mode ends.

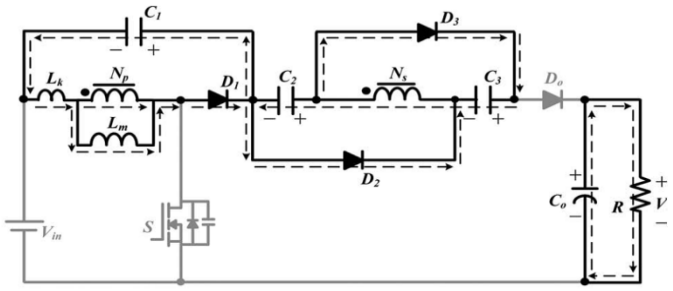


Fig.6. Current flowing path of Mode-IV during one switching period at CCM operation.

5) Mode V [t_4, t_5]: During this time interval, S is turned off. Diodes D_1 and D_0 are turned on, and D_2 and D_3 are turned off. The current-flow path is shown in Fig.7. The energies of leakage inductor L_k and magnetizing inductor L_m are released to the clamp capacitor C_1. The primary and secondary windings of the coupled inductor, DC sources V_{in}, and capacitors C_2 and C_3 are in series to transfer their energies to the output capacitor C_0 and load R. This operating mode ends when capacitor C_1 starts to discharge at $t = t_5$.

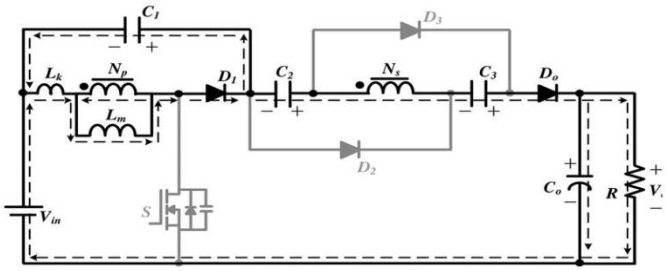
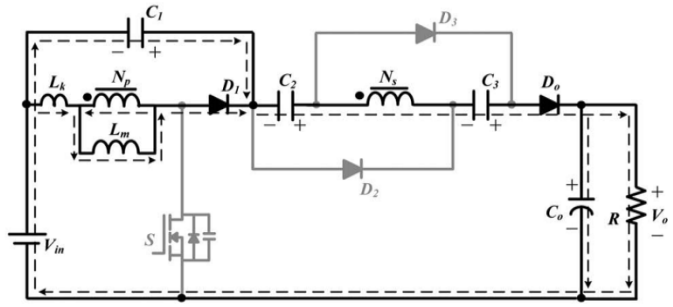


Fig.7. Current flowing path of Mode-V during one switching period at CCM operation.

6) Mode VI [t_5, t_6]: During this time interval, S is still turned off. Diodes D_1 and D_0 are turned on, and D_2 and D_3 are turned off. The current-flow path is shown in Fig.8. The primary-side and secondary-side windings of the coupled inductor, DC sources V_{IN}, and capacitors C_1, C_2, and C_3 transfer their energies to the output capacitor C_0 and load R. This mode ends at $t = t_6$ when S is turned on at the beginning of the next switching period.

$$V_{c2} = V_{c3} = v_{L2}^{II} = nkV_{\text{in}}$$



$$\int_0^{DT_s} v_{L1}^{II}\,dt + \int_{DT_s}^{T_s} v_{L1}^{VI}\,dt = 0$$

Fig.8. Current flowing path of Mode-VI during one switching period at CCM operation.

III. STEADY-STATE ANALYSIS OF THE PROPOSED CONVERTER

A. CCM Operation

At modes IV and V, the energy of the leakage inductor L_k is released to the clamped capacitor C_1. According to previous work [15], the duty cycle of the released energy can be expressed as

$$\mathbf{D_{C1}} = \frac{\mathbf{t_{C1}}}{\mathbf{T_S}} = \frac{2(1-\mathbf{D})}{\mathbf{n}+1} \quad \ldots\ldots\ldots\ldots (1)$$

Where T_s is the switching period, D_{c1} is the duty ratio of the switch, and t_{c1} is the time of modes IV and V. By applying the voltage-second balance principle on L_m, the voltage across the capacitor C_1 can be represented by

$$\mathbf{V_{C1}} = \frac{\mathbf{D}}{1-\mathbf{D}}\mathbf{V_{in}}\frac{(1+\mathbf{K})+(1-\mathbf{K})\mathbf{n}}{2} \quad \ldots\ldots\ldots\ldots \quad (2)$$

Since the time durations of modes I, III, and IV are significantly short, only modes II, V, and VI are considered in CCM operation for the steady-state analysis. In the time period of mode II, the following equations can be written based on Fig.:

$$v_{L1}^{II} = \frac{L_m}{L_m + L_{k1}} V_{\text{in}} = kV_{\text{in}} \quad \ldots\ldots\ldots\ldots \quad (3)$$

$$v_{L2}^{II} = nv_{L1}^{II} = nkV_{\text{in}}. \quad \ldots\ldots\ldots\ldots \quad (4)$$

Thus, the voltage across capacitors C2and C3can be written as

$$V_{c2} = V_{c3} = v_{L2}^{II} = nkV_{\text{in}}. \quad \ldots\ldots\ldots\ldots \quad (5)$$

During the time duration of modes V and VI, the following equation can be formulated based on Fig.:

$$v_{L2}^{V} = v_{L2}^{VI} = V_{\text{in}} + V_{c1} + V_{c2} + V_{c3} - V_o \quad \ldots\ldots \quad (6)$$

Thus, the voltage across the magnetizing inductor Lm can be derived as

$$v_{L1}^{V} = v_{L1}^{VI} = \frac{v_{L2}^{VI}}{n} = \frac{V_{\text{in}} + V_{c1} + V_{c2} + V_{c3} - V_o}{n} \quad \ldots\ldots \quad (7)$$

Using the volt-second balance principle on Lm, the following equation is given

$$\int_0^{DT_s} v_{L1}^{II}\,dt + \int_{DT_s}^{T_s} v_{L1}^{VI}\,dt = 0. \quad \ldots\ldots \quad (8)$$

Substituting (2), (3), (5), and (7) into (8), the voltage gain is obtained as

$$M_{\text{CCM}} = \frac{1+nk}{1-D} + nk + \frac{D}{1-D}\cdot\frac{(1-k)(n-1)}{2} \quad \ldots\ldots \quad (9)$$

The schematic of the voltage gain versus the duty ratio under various coupling coefficients of the coupled inductor is shown in Fig... It is seen that the voltage gain is not very sensitive to the coupling coefficient. When k is equal to 1, the ideal voltage gain is written as

$$M_{\text{CCM}} = \frac{1+n}{1-D} + n \quad \ldots\ldots \quad (10)$$

If the proposed converter is operated in boundary condition mode, the voltage gain of CCM operation is equal to the voltage gain of DCM operation. From (10), the boundary normalized magnetizing inductor time constant τ_{LmB} can be derived as

$$\tau_{LmB} = \frac{D(1-D)^2}{2(1+n)(1+2n-nD)} \quad \ldots\ldots \quad (11)$$

IV. Matlab/Simulink Modelling And Simulation Results

The Converter Proposed in Section II is Modelled and Simulated as shown in figure 9.
Here the simulation is carried out in two cases
1. Proposed high step-up DC/DC converter.
2. Proposed high step-up DC/DC converter applied to AC load.

Case 1: Proposed high step-up DC/DC converter:

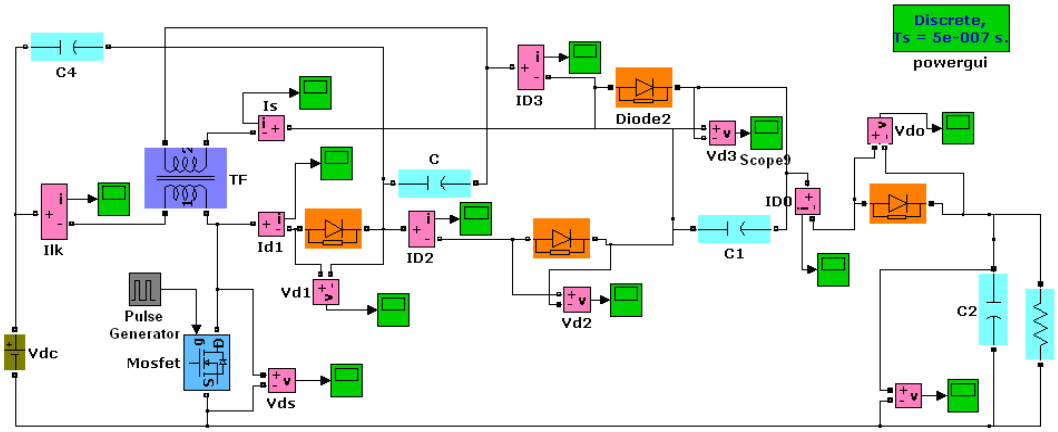


Fig.9. MATLAB/SIMULINK circuit of the converter

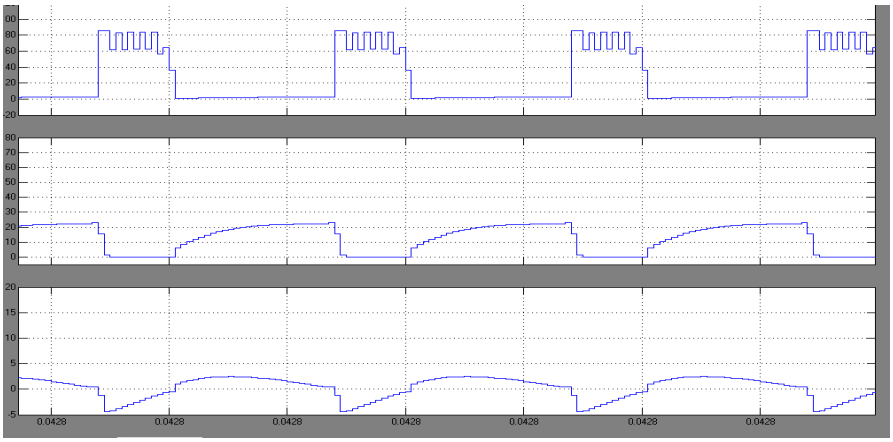


Fig.10. Shows the proposed converter Output waveforms of proposed converter V_{DS}, I_{LK}, I_S

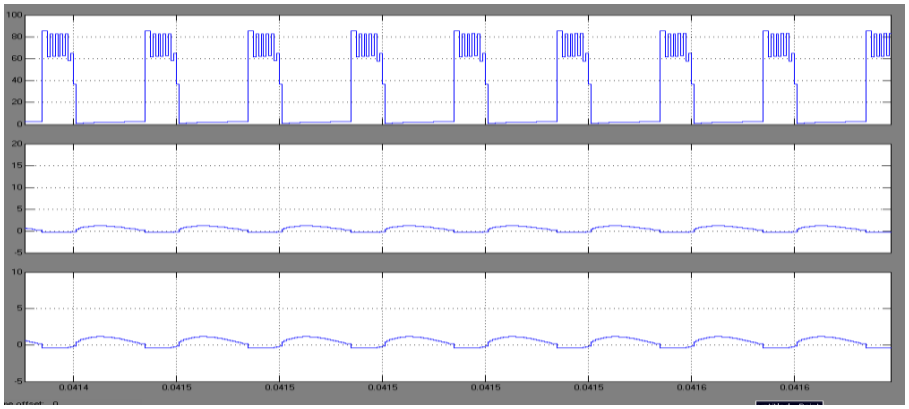


Fig 11: waveforms of V_{DS}, I_{D2}, I_{D3}

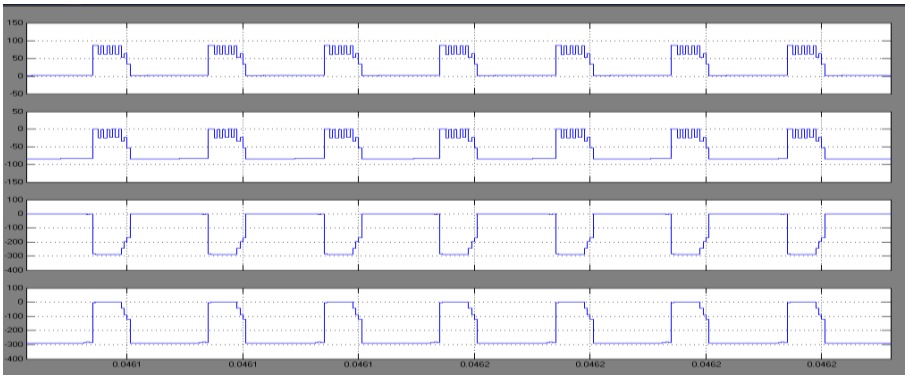


Fig.12: Waveforms of V_{DS}, V_{D1}, V_{D2}, V_{D0}

Case 2: Proposed high step-up DC/DC converter applied to AC load.

The above Fig 10, Fig 11, Fig12 shows the waveforms of current through leakage inductor $I_{LK,}$ current Through secondary $I_{S,}$ current through diode D_2 I_{D2}, current through diode D_3 $I_{D3,}$voltage across diode D_1 V_{D1}, Voltage across diode D_2 $V_{D2,}$ voltage across output diode D_0 V_{D0}

Fig.13 shows the MATLAB/SIMULINK circuit of the proposed high step-up DC/DC converter applied to AC load with photo voltaic cell as the input.

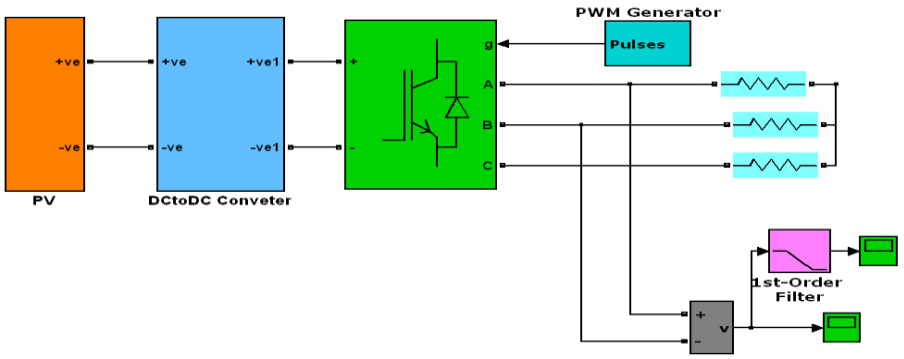


Fig.13 SIMULINK model of the micro grid with pv cell,DC-DC converter, inverter

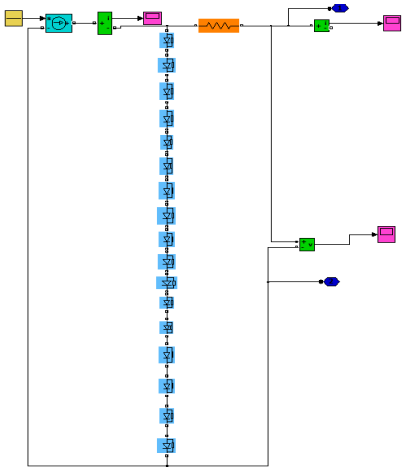


Fig.14 Photovoltaic cell model

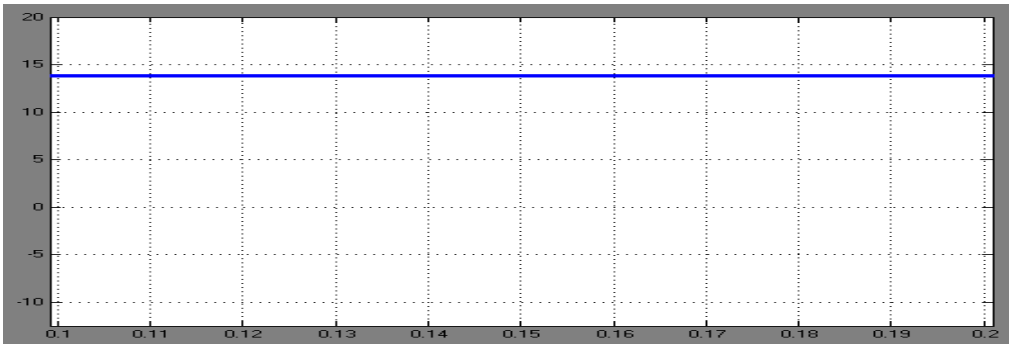


Fig.15 PV model voltage waveform

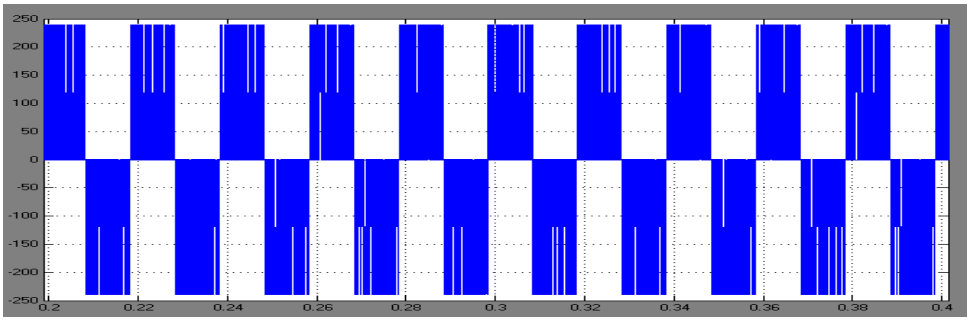


Fig.16 Inverter output voltage without filter

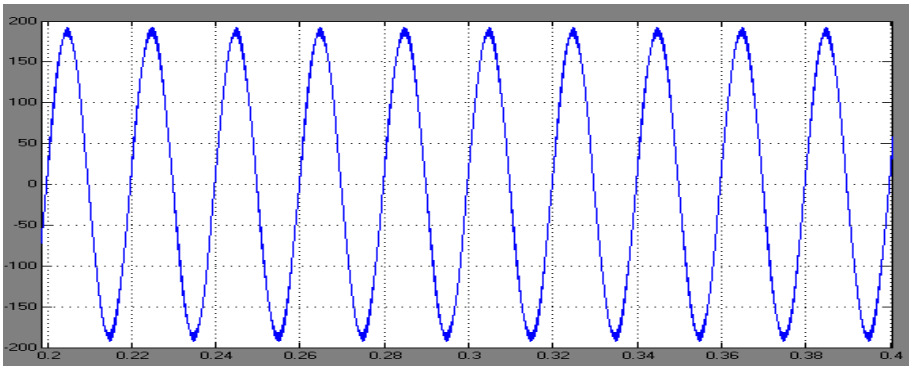


Fig.17 Inverter output voltage with filter

V. Conclusion

This paper proposed a novel, high efficiency, and high step-up DC–DC converter applied to AC load with the help of inverter. By using the capacitor charged in parallel and discharged in a series by the coupled inductor, high step-up voltage gain and high efficiency are achieved. The steady-state analyses of voltage gain and boundary operating condition are discussed in detail. A prototype circuit of the proposed converter is built in the MATLAB/SIMULINK environment. The voltage stress on the main switches is 90V; thus, low voltage ratings and low on-state resistance levels R_{DS} (ON) switch can be selected. Moreover, the proposed converter has simple structure.

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