

## Study of Floating Body Effect in SOI Technology

Vandana B.

(M.Tech, Member IEEE), Electronic Engineering, Citd, Hyderabad, India

**ABSTRACT:** The paper presents the floating body effects of PD/FD of SOI technology and also discusses the issues behind the effects, gives the clear description of factors effecting floating body such as threshold voltage, drain current, gate-to-body tunneling kink effect. And also shows the merits/demerits of PDSOI/FDSOI.

**KEY WORDS:** FDSOI, PDSOI, Floating body effect, Kink effect

### I. INTRODUCTION

Silicon on Insulator is a semiconductor electronic device which is now used as an integrated chip in almost all highly reliable/efficient in digital/analog electronic devices. Before the use of SOI in market BULK technology was leading technology in electronic industry, due to following reasons such as latch up, parasitic capacitance and leakage currents in bulk technology fail to continue in developing highly effective devices. The design rules which help in developing SOI technology was extracted from bulk technology by incorporating oxide layer over the silicon substrate, 50% of the problem was solved such as leakage currents, eliminating wells, scaling of the device effect threshold voltage is reduced and latch up problem. SOI, new device architectures allow optimum electrical properties to be obtained for low power and high performance circuits. In SOI an interesting observation is that the body terminal is either tied to gate or left free for floating called as "floating body" as when the floating body is considered it has some important features in reducing power consumption and improving the device efficiency, about these features an important description is shown in upcoming sections and the reasons for the body tied are also shown.

### II. ADVANTAGES OF SOI OVER BULK TECHNOLOGY

The description of SOI technology is described briefly in [1]. SOI advantages is given below, according to these advantages it has been given clearly that what factors are superior to bulk technology and is described for each and every advantage.

#### 2.1 SOI Advantages:

The SOI wafer structure has several important advantages over CZ bulk or epitaxial starting wafer architectures. SOI wafers potentially offer "perfect" transistor isolation (lower leakage), tighter transistor packing density (higher transistor count/higher IC function at the same lithographic resolution), reduced parasitic drain capacitance (faster circuit performance and lower power consumption), and simplified processing relative to bulk or epitaxial silicon wafers. Due to these advantages, SOI wafers appear ideal for leading edge integrated circuits with high speed, high transistor count, low voltage/low power operation, and battery operated systems requirements, such as portable logic or microprocessor ICs. Silicon-on-insulator (SOI) wafers have traditionally been used for extreme environmental applications, such as high temperature and severe environments (e.g., outer space). However, they are expected to expand into mainstream CMOS applications due to these advantages:

- Excellent lateral and vertical isolation of active devices from substrate:
  1. Elimination of inter-device leakage and latch-up in CMOS structures
  2. Effective reduction of substrate coupling in RF circuits (allows higher quality inductors with increased Q factor)
  3. Effective reduction of interference and cross-talk between devices in mixed-signal ICs
  4. Reduced soft errors (e.g., in SRAM) from radiation effects (electron hole pair generation)
  5. Different voltages may be used on different devices without the added processing steps required for triple wells.
- Faster device operation (speed/power product) due to reduction of parasitic capacitance (primarily due to reduced source-drain junction capacitance, but also from gate-to-substrate capacitance and metal-to-substrate capacitance):
  1. IBM reported a 20% to 35% increase in chip speed for their PowerPC chips [2, 3]
- Lower power consumption (speed/power product) due to lower operating voltages on devices and lower parasitic capacitance:
  1. IBM reported a 35% to 70% reduction in power consumption for their PowerPC chips
  2. More functions per die area or reduced die area per function; SOI allows tighter layout design rules (higher integration density), mainly due to reduced STI layout area required for lateral junction isolation (resulting from the absence of wells and the possibility of direct contact of the source-drain diodes in the NMOS and PMOS transistors) [2, 3, 4]
  3. Performance improvement equivalent to next technology node without scaling (e.g., performance of 0.25 micron devices on SOI wafers equivalent to performance of 0.18 micron devices on bulk wafers)
  4. Potential to simplify device fabrication steps:
  5. Fewer masks and ion implantation steps, made possible by the elimination of well and field isolation implants
  6. Less complex (costly) lithography and etching required to achieve next-generation performance
  7. As noted above, SOI wafers offer the potential to simplify the process presently used for CMOS devices fabricated in bulk wafers. The process used for deep submicron

- CMOS on bulk wafers may be described in the following (highly simplified) way:
  1. Formation of shallow trench isolation (STI) regions, which surround and define the active areas where transistors will be fabricated
  2. Formation of deep n-type and p-type wells in the active areas, using high energy ion implantation; these wells are vertically “profiled” using multiple ion implantation steps to achieve:
    - 2a) A deep doping peak (the “deep well”), which suppresses latch-up, reduces soft errors (caused by charge pairs generated from radiation effects), and which provides part of the ESD protection path NOTE: if a deeper “triple well” (which is typically a deep n-well structure beneath and around a shallower p-well) is used for voltage isolation from substrate, it is formed just prior to formation of these n-type and p-type “twin wells”
    - 2b) A shallower doping peak (the “field channel stop”), located just below the STI trench bottom, which suppresses lateral leakage between adjacent transistors within the wells (intra-well) and between adjacent transistors at the well boundaries (inter-well)
    - 2c) A very shallow doping peak at the silicon surface (the “ $V_t$  adjust”), which sets the threshold voltage of the transistors
  3. Formation of the gate stack, including the gate oxide insulator and the Poly silicon gate on top of it (the poly silicon gate is highly doped, n-type for the n-channel transistors and p-type for the p-channel transistor); the gate electrode is subsequently defined by lithography and anisotropic etching.
  4. Formation of the transistor body and contacts, including:
    - 4a) Formation of source-drain extensions using ultra-low energy ion implantation (which is self aligned to the gate electrode) and rapid thermal annealing (RTA)
    - 4b) Formation of halo (punch-through stop) regions by self-aligned, high tilt implantation (and RTA)
    - 4c) Following the formation of a sidewall space on the gate, formation of source-drain contact regions by high dose, low energy implantation (and RTA)
    - 4d) Formation of salicide (Self-Aligned siLICIDE) contact metal on the top of the gate and source-drain regions. [8]

The opportunity for fabrication process simplification mainly occurs in step 2 (specifically 2a and 2b), above. The use of SOI wafers eliminates the need for the high-energy ion implantation processes that form the deep n-type and p-type “twin” wells (step 2a) and field channel stop isolation regions (step 2b), which are presently required in leading edge bulk CMOS IC fabrication. Also, the formation of deep “triple well” structures using high energy ion implantation processes (see note in step 2a, above) is unnecessary with SOI wafers to achieve voltage (electrical) isolation from the substrate. Note that the ion implantation and RTA processes for the formation of transistors, e.g., extension and contact source/drain formation (steps 4a and 4c), poly-silicon gate doping (in step 3), and threshold voltage adjustment (step 2c) are still required with SOI wafers.

### III. FD/PD SOI

SOI (silicon on insulator) which means silicon device is fabricated on insulator using silicon dioxide, it is fabricated as three layered device such as the bottom most layer is the substrate which is lightly doped. The insulating layer is created by flowing oxygen onto a plain silicon wafer and then heating the wafer to oxidize the silicon, thereby creating a uniform buried layer of silicon dioxide which is called as buried oxide layer (BOX). The insulating layer increases device performance by reducing junction capacitance as the junction is isolated from bulk silicon. The decrease in junction capacitance also reduces overall power consumption. And the top most layer is same as bulk CMOS which help in channel creation. SOI is also a 4 terminal device source, drain, gate and the body; here source and drain terminals are interchange. The width of the silicon film decides whether the SOI is fully depleted or partially depleted fig 1(b). If the width of silicon film laid over the buried oxide is thin then the device is said to be fully depleted and if the width of the silicon film is thick then it is said to be partially depleted fig 1(a). Silicon on Insulator fabrication process helps in achieving greater performance and offers less power consumption as compared to bulk CMOS process.

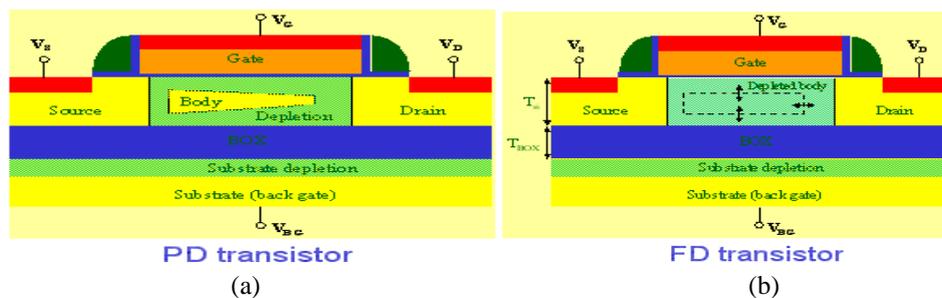
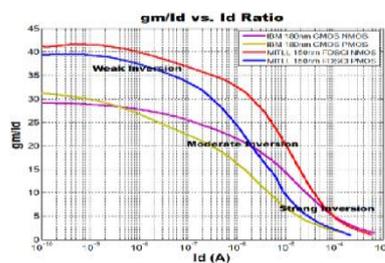


Figure 1 1(a) PD SOI, 1(b) FD SOI transistor

The FD devices have several advantages compared to the PD devices; however, there are some drawbacks also. These are some of the tradeoffs in use of the FD versus PD SOI MOSFETs:

- Fully-depleted SOI devices are naturally free from kink effect, because the majority carriers can penetrate more easily into the source; thus, preventing the excess carriers accumulation [7].

- FD SOI has an enhanced sub-threshold swing,  $S$  (see Figure 4). For the bulk and PD devices,  $1/S = 85$  to  $90$  mV/decade, and for FD SOI,  $1/S = 65$  to  $70$  mV/decade, which is close to an ideal characteristic of a MOS transistor at room temperature ( $1/S = 60$  mV/decade) [10].
- Fully-depleted SOI devices have the highest gains in circuit speed, reduced power requirements and highest level of soft-error immunity [9]. FD devices operate faster because of a sharper sub-threshold slope, and a reduced threshold voltage that allows for faster switching of the MOS transistors. These transistors also have increased drive currents at relatively low voltages.
- Several drawbacks of the FD SOI design and process come along with their benefits:
- Although FD MOSFETS are naturally free from the kink effect, the interface coupling effect affects their operation [7, 5]. The interface coupling is inherent to fully depleted SOI devices, where all parameters (threshold voltage, trans-conductance, interface-trap response etc.) of one channel are insidiously affected by the opposite gate voltage (at the buried oxide).

Figure 2  $\frac{g_m}{I_d}$  vs  $I_d$  ratio

- While FD SOI MOSFETs offer a reduced body effect and a nearly ideal  $g_m/I_d$  ratio when biased in the weak or moderate inversion region, a weak (not fully eliminated) current voltage kink still exists in the strong inversion region. Therefore, additional technology optimization is required to use these transistors for baseband analog applications [12]. Besides, accumulation at the back interface can lower the breakdown voltage and introduce the kink effect.
- The threshold voltage fluctuation due to SOI thickness variation is one of the most serious problems in FD SOI MOSFETs. In comparison, partially depleted SOI devices are built on a thicker silicon layer and are simpler to manufacture.
- Most design features for developing PD devices can be imported from the bulk silicon devices and used in the SOI environment with only modest changes. This makes circuit redesign for the PD devices simpler than for the FD microcircuits.

#### IV. SOI MOSFET TRANSISTORS

The major difference between a bulk-Si MOS transistor and a SOI MOS transistor from the circuit designer point of view is that the later has smaller junction capacitance and has a floating body [16]. These effects include parasitic bipolar current, self-heating and body contact resistance, some other effects and characteristics associated with SOI MOSFETs:

**IV.1 Threshold Voltage:** For a thick-film SOI device, which essentially behaves like a bulk device due to absence of interaction between the front and back depletion regions, the threshold voltage is same as in a bulk device and is given as:

$$V_{th} = V_{FB} + 2\phi_F + \frac{qN_a x_{dmax}}{C_{ox}} \quad (1)$$

For a thin-film SOI device, the expressions for threshold voltage as a function of the different possible steady-state charge conditions at the back interface are given as [16]: the below equations shows the threshold voltage equation in three operating regions

$$V_{th1,inv2} = \phi_{ms} - \frac{Q_{ox1}}{C_{ox1}} + 2\phi_F - \frac{Q_{depl}}{2C_{ox1}} \quad (2)$$

$$V_{th1,depl} = V_{th1,acc2} - \frac{C_{si}C_{ox2}}{C_{ox1}(C_{si}+C_{ox2})}(V_{G2} - V_{G2,acc}) \quad (3)$$

$$V_{th1,acc2} = \phi_{MS1} - \frac{Q_{ox1}}{C_{ox1}} + \left(1 + \frac{C_{si}}{C_{ox1}}\right)2\phi_F - \frac{Q_{depl}}{2C_{ox1}} \quad (4)$$

**IV.2 Body Effect:** In a bulk device, the body effect is defined as the dependence of the threshold voltage on the substrate bias. In an SOI transistor, it's similarly defined as the dependence of the threshold voltage on the back-gate bias. In a thick film device, the body effect (or, more aptly back-gate effect) is negligible due to absence of coupling between the front and back gate. In a thin-film fully depleted device, the body effect parameter, is obtained from eqn. (3),

$$\gamma \equiv \frac{\partial V_{th1}}{\partial V_{G2}} = -\frac{C_{si}C_{ox2}}{C_{ox1}(C_{si}+C_{ox2})} \quad (5)$$

It can be seen from eqn. (5) that the threshold voltage dependence on back-gate bias is linear in case of thin-film SOI transistors.

**IV.3 Floating-Body Effects:** Floating body effect (FBE) is the major parasitic effect in SOI-MOSFETs and is a consequence of the complete isolation of the transistor from the substrate. The effect is related to the built-up of a positive charge in the silicon body of the transistor, originating from the holes created by impact ionization. This charge cannot be removed rapidly enough, primarily because no contact with the Si film (body) is available.

When the drain voltage is large enough, the channel electrons can obtain sufficient energy in the high electric field near the drain and to generate electron hole pairs via the impact ionization mechanism. The generated electrons rapidly flow into the drain, and the holes migrate toward the lowest potential region, i.e., the p-type floating body. Then the holes caused at the lowest potential region will be swept into the source since the source/body diode is forward biased

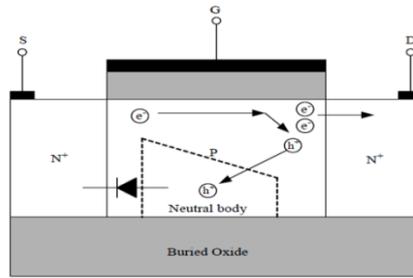


Figure 3 Representing FLOATING body effect in PD SOI

There are various consequences of this built up charge, which are generally referred to as the floating-body effects, such as [5]: kink-effect; negative conductance and trans-conductance; hysteresis and instabilities, single transistor latch (the transistor cannot be turned off by reducing gate voltage), bipolar transistor action, and premature breakdown. The FBE can lead to circuit instabilities, frequency-dependent delay time, and pulse stretching. Many of the negative consequences of the FBE could be eliminated by using a body contact for every MOSFET, but this is generally not an optimum solution. It should be noted that these typical SOI effects can be observed even in the bulk-Si MOSFETs at low temperatures when the substrate becomes semi-insulating and if the substrate contact is left floating.

Considering the MOS portion of the partially-depleted SOI NMOS device, the threshold voltage is subject to the floating body effect. The accumulated holes near the body-emitter junction in the thin-film due to the parasitic bipolar device caused by the floating body increase the body-emitter voltage ( $V_{BE}$ ). As a result, the threshold voltage is lowered. Considering this effect, the threshold voltage model ( $V_T$ ) and the conducting current through the front channel ( $I_{CH}$ ) under the front gate oxide have been reported in [5]. In this subsection, the current conduction mechanisms for the MOS portion and the parasitic bipolar portion of the partially-depleted SOI NMOS device have been explained. In the next subsection, the temperature-dependent kink effect model is derived for the device biased in the triode region ( $V_{DS} < V_{DSAT}$ ) and the saturation region

( $V_{DS} > V_{DSAT}$ )

**1) Triode Region  $V_{DS} < V_{DSAT}$ :** Fig. (4,6) shows the current conduction mechanism of the partially-depleted SOI NMOS device biased in the triode region. In the front channel region near the drain, there is no impact ionization. Therefore, no holes are injected into the floating body. As a result, the body-emitter voltage ( $V_{BE}$ ) is small.

Consequently, the parasitic bipolar device does not turn on. Under this situation, the floating body can be regarded as two diodes connected back to back. At the body-emitter junction, which is forward biased, the conducting current is  $I_F$ . At the body-collector junction, which is reverse biased, the conducting current is  $I_R$ . Considering the impact ionization effect at the body-collector junction, the conducting current is magnified by a factor of MB—the conducting current becomes MBIR. Considering the current conduction of the parasitic bipolar device ( $I_F = MBIR$ ), from [5-7], the body-emitter voltage can be obtained

$$V_{BE} = \frac{2kT}{q} \ln \left[ \frac{-I_{reco} + \sqrt{I_{reco}^2 + 4I_{ES} M_B (I_{gen} + I_{diff})}}{2I_{ES}} \right] \quad (6)$$

**2) Saturation Region  $V_{DS} > V_{DSAT}$ :** For the partially-depleted SOI NMOS device biased in the saturation region, the current conduction mechanism is shown in Fig. (6,4). In this region, due to  $V_{DS} > V_{DSAT}$ , the impact ionization in the front channel region near the drain is important. As a result, a large amount of holes due to the front channel impact ionization are injected into the floating body. [11,13,14]

Consequently, the accumulated holes near the body-emitter junction turn on the bottom parasitic bipolar device since the body-emitter voltage  $V_{BE}$  becomes large. From [5], in the saturation region,  $V_{BE}$  can be expressed as

$$V_{BE} = V_{BE1} + V_{BE2} - (V_{BE1} + V_{BE2})^{1/m} \quad (7)$$

Where  $V_{BE1}$  is the  $V_{BE}$  when recombination current dominates the parasitic bipolar device;  $V_{BE2}$  is the  $V_{BE}$  when diffusion current dominates the parasitic bipolar device. Based on the above analysis as shown in Fig. 1(a) and (b), the drain current of the partially depleted, SOI NMOS device is composed of the front channel current in the front MOS portion and the collector current in the bottom parasitic bipolar device. The above formulas are the closed-form analytical temperature-dependent kink effect model for the partially-depleted SOI NMOS device.

(In order to estimate the Floating body voltage, especially its transient characteristics in PD-SOI circuits, we consider physics-based models consisting of the body capacitance associated with the body region and various current components. The equivalent circuit representation of the PD-SOI NMOSFET is shown in Fig. 1. The transient Floating body (node 'B') potential  $V_B(t)$  can be determined from the net current and the time-varying body capacitance as follows:

$$\frac{dQ_B(t)}{dt} - I_{ii}(t) - I_{diode}(t) + I_h(t) = 0, C_B(t) = C_{of} || C_{ch}(t) + C_{js}(t) + C_{jd}(t) + C_{ob}, \quad (8)$$

where  $I_{ii}(t)$ ,  $I_{diode}(t)$ , and  $I_h(t)$  represent the impact ionization current in the body-drain junction, the net electron current component ( $i_B(t)$  and  $i_C(t)$ ) into floating body region which is the base region of the parasitic npn bipolar transistor, and the out-going hole current from the body-source junction, respectively [15]

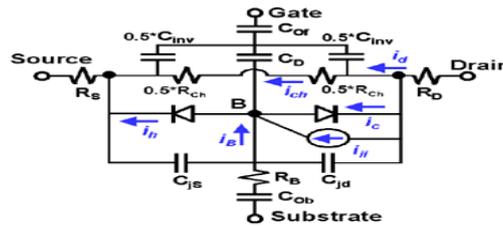


Figure 4 Equivalent circuit and floating body current components for the PD-SOI NMOSFET model.

**IV.4 Self Heating Effects:** Due to thermal isolation of substrate by the buried insulator in an SOI transistor, removal of excess heat generated by the Joule effect within the device is less efficient than in bulk, which leads to substantial elevation of device temperature. The excess heat mainly diffuses vertically through the buried oxide and laterally through the silicon island into the contacts and metallization. Due to the relatively low thermal conductivity of the buried oxide, the device heats up to 50 to 150C. This increase in device temperature leads to a reduction in mobility and current drive, thus degrading the device performance over a period of time.[5,7]

**IV.5 Impact Ionization:** The semi-conductor equations that we have used to derive our approximate formulae have explicitly excluded the physical phenomena that lead to the kink effect. To account for the rise in the drain-source current we introduce a simple conceptual model to justify a phenomenological correction term. If we attribute the kink effect entirely to impact ionization effects then we can write  $I_{ds} = I_{dso} + I_{kink}$  with  $I_{kink} = M I_{dso}$  where  $I_{dso}$  is the current that would be obtained if impact ionization effects were absent. When impact ionization is present it provides a source of current and the electron current equation has the modified form  $\nabla J_n = G_{I-I}$

Where the impact ionization source is usually modeled by  $G_{I-I} = -\alpha_n J_n$  with  $\alpha_n = A_n \exp(-\beta n / F)$  with  $n$  a strongly dependent on the electric field strength  $F$  [24]. Adopting the assumptions of Jacunski *et al.* [25], but introducing a more accurate approximation, leads to the fitting function.

**IV.6 Floating Body and Parasitic Bipolar Effects:**

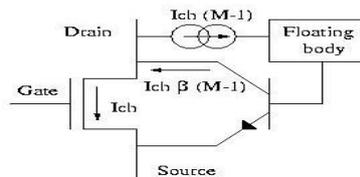


Figure 5: Parasitic bipolar transistor of the SOI MOSFET

The presence of a floating volume of silicon beneath the gate is at the origin of several effects unique to SOI, generically referred to as floating body effects [21]. There exists a parasitic bipolar transistor in the MOS structure. If we consider an n-channel device, the N+ source, the P-type body and the N+ drain indeed form the emitter, the base, and the collector of an NPN bipolar transistor, respectively. In a bulk device, the base of the bipolar transistor is usually grounded by means of a substrate contact. But, due to the floating body in an SOI transistor, the base of the bipolar transistors is electrically floating. This parasitic bipolar transistor (fig.5) is origin of several undesirable effects in SOI devices.

Next, we discuss some important floating body and parasitic bipolar effects in SOI devices.

**IV.7 Kink Effect:** The kink effect consists into the appearance of a *kink* in the output characteristics of an SOI MOSFET working in strong inversion, as shown in. The kink is very strong in n channel transistors but, is usually absent from p-channel devices.

Let us consider a thick-film, partially depleted SOI n-channel transistor. When the drain voltage is high enough, the channel electrons can acquire sufficient energy in the high electric field zone near the drain to create electron-hole pairs, due to an impact ionization mechanism. The generated electrons move into the channel and the drain, whereas the holes, which are majority carriers in the p-type body, migrate towards the place of lowest potential *i.e.*, the floating body.

The injection of holes into the floating body forward biases the source-body diode. The floating body reaches a positive potential, as given by the following equation [8]:

$$I_{holes,gen} = I_{so} \left[ \exp \left[ \frac{qV_{BS}}{nKT} \right] - 1 \right] \tag{8}$$

The increase of body potential gives rise to lowering of threshold voltage and source-body potential barrier. More minority carriers are able to flow from source to the channel, thereby causing an excess drain current and producing many more pairs through the avalanche process. This positive feedback results in a sudden increase in  $I_D$  or “kink” in output characteristics. If the minority carrier lifetime in the silicon film is high enough, the kink effect can be reinforced by the NPN

bipolar transistor (fig. 5). The “base” hole current is amplified by the bipolar gain, which gives rise to an increased net drain current, sometimes referred to as *second kink* [22].

Now, let us consider the case of a thin-film, fully depleted SOI n-channel MOSFET. It has been shown [23] that the electric field near the drain is lower in the fully depleted device than in partially depleted one. As a result, less electron-hole pair generation takes place in the fully depleted device. Also, contrary to the case of a partially depleted transistor, the source-to-body diode is “already forward biased” due to the full depletion of the film, and therefore, holes can readily combine in the source without having to raise the body potential there. This explains why thin film fully depleted n-channel MOSFETs are free of kink effect. [16, 22, 23]

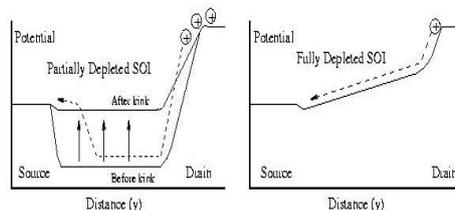


Figure 6: Potential in neutral region from source to drain in PD and FD SOI Devices

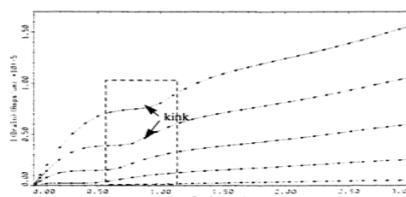


Figure 7 kink effect

The p-channel devices are free of kink effect because coefficient of electron-hole pair generation by energetic holes is much lower than that by energetic electrons. The kink effect is not observed in bulk devices as the majority carriers generated by impact ionization can escape into the substrate or to a well contact. The kink effect can be eliminated from the partially depleted SOI MOSFETs if a body contact is provided for removal of excess majority carriers from the device body. Self heating, bipolar currents and kink effect are said to be the major disadvantages of SOI technology when the body is left floating.

**IV.8 Effect of Changes in Back Oxide Thickness on Kink Voltage:** The kink voltage is found to have a significant dependence on the thickness of the back oxide in a SELBOX structure. The dependence of kink voltage, on back oxide thickness for a fixed gap length is  $0.03 \mu\text{m}$ . Keeping the gap length constant, if we vary the back oxide thickness we can expect a change in the gap resistance. For the estimation of gap resistance, back oxide thickness is the length of the resistance and the gap length is the width of the gap resistance. As we increase the back oxide thickness keeping the gap length constant, the effective gap resistance increases. This will lead to an increase in the body potential. Consequently, the body potential at which kink occurs will be reached at a lower drain voltage. With reduced oxide thickness, the back oxide gap resistance also reduces and the rise in the body voltage will be reduced. In this case, the body voltage needed to cause the kink will occur at a higher drain voltage and hence the kink voltage will be higher. Therefore, a device with thinner back oxide is more bulk-like and will be less susceptible to kink phenomenon. Even though a very small gap length is required to virtually eliminate kink phenomenon from the device characteristics, producing a small gap length can be technologically challenging [18]. Fabrication of devices with large gap length is likely to be easier. But, with increase in the gap length, the device tends to become more bulk-like and thus lose the associated advantages of SOI such as reduced source-body and drain-body capacitances.

**IV.9 Output Characteristics:** The expression of the current characteristics  $I_D (V_{G1}, V_{G2}, V_{DS})$  of a thick-film SOI MOS transistor is identical to that of a bulk MOSFET, with some modifications due to the parasitic bipolar effects coming up due to the presence of an electrically floating body.

The derivation of the current characteristics of a thin film, fully depleted SOI device can be done [4] using assumptions of the classical gradual channel approximation [17]. The saturation current in an SOI MOSFET is given as:

$$I_{Dsat} \cong \frac{1}{2} \frac{W}{L} \frac{\mu_n C_{ox1}}{(1+\alpha)} (V_{G1} - V_{th})^2 \quad (9)$$

Where

$$\alpha = \frac{C_{si}}{C_{ox1}} \text{ FD device with back interface in accumulation}$$

$$\alpha = \frac{C_{si} C_{ox2}}{C_{ox1} (C_{si} + C_{ox2})} \text{ FD device with back interface in depletion}$$

$$\alpha = \frac{\epsilon_{si}}{x_{dmax} C_{ox}} \text{ For bulk and partially depleted devices}$$

Since, a fully depleted SOI < a bulk < a back accumulation SOI, the drain saturation current is highest in the fully depleted device, lower in the bulk device, and even lower in the device with back accumulation. This high saturation current

in a thin-film, fully depleted SOI MOSFETs brings about an increase in current drive, which contributes to excellent speed of fully depleted SOI CMOS circuits

**IV.10 Edge Effects :** The lateral edges of the SOI MOSFETs represent a parasitic conduction path between the source and the drain. This sidewall transistor operates in parallel with the main transistor, and strong coupling and charge sharing between the front, back, and the edge channels dictate its threshold voltage. Special edgeless devices (e.g. H-gate transistor, which has two p+ body contacts that inhibit any conduction path along the sidewalls) may be designed, but this is a space-consuming alternative [7,8].

## V. METHODS FOR REDUCING FLOATING BODY EFFECTS

In order to achieve the full potential of SOI technology, it is increasingly important to reduce the floating body effects. Many different schemes have been proposed in the past [19]

**V.1 Body contact:** Contacting silicon underneath the gate region to the ground effectively suppresses the kink effect as well as the parasitic lateral bipolar effects. Several schemes exist to provide the transistor with body contact. Figure 7a shows the normal body contact. It consists of a P+ region which is in contact with the P-type silicon underneath the gate. However, in transistors with a large gate width, the presence of single body contact at one end of the channel may not be sufficient to suppress the kink and BJT effects, especially when considering the high resistance of the weakly doped channel region.

The H gate MOSFET design, shown in Figure 7b. Helps to solve this problem, since body contacts are presented at both ends of the channel [19]. However, the efficiency of such a contact scheme depends on channel resistance, which is usually very high in modern processes. In addition, such body contacts occupy a lot of area

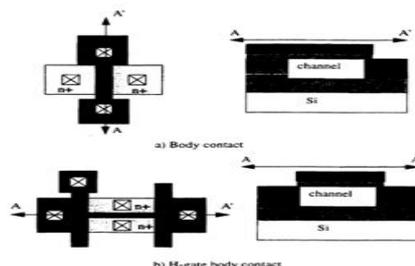


Figure 7 NMOS transistor with body contact

**V.2 Source Body Tie Structure:** A more compact method, source body tie structure, has been proposed by Omura and Izumi [20]. As illustrated in Figure 1. 10a, the P+ body ties are created on the side of the N+ source diffusion. If the device width is large, additional P+ regions can be formed in the source (such that a P+ N+ P+ N+ structure is introduced). Such a device has the main drawbacks of being asymmetrical (source and drain cannot be switched), and the effective channel width is smaller than the width of the active area. An alternative method involving Schottky contact in source drain region has been proposed by Sleight and Mistry [21] as shown in Figure 8. It provides symmetrical operation. However, increased leakage current associated with Schottky contact degrades device performance.

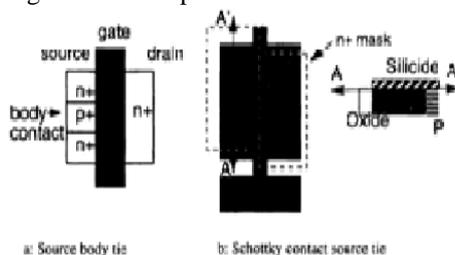


Figure 8 source body tie body contact in SOI structure

The methods discussed above are effective in reducing the floating body effects but have either a limited area of applications or they cannot fully fulfill the advantages of the SOI structure.

## VI. CONCLUSION

Finally the paper conclude by presenting brief description about the floating body and the factors that effecting floating body in both partially and fully depleted SOI technology. In FDSOI n-MOSFET has lower leakage current than PDSOI n-MOSFET. The leakage current is inversely proportional to the threshold voltage, channel length and gate oxide thickness. The threshold voltage in PD SOI n-MOSFET is more than that of FDSOI n-MOSFET.

The main drawback in PDSOI n-MOSFET is kink effect, which is eliminated in FDSOI n-MOSFET. A careful trade-off between these two effects must be achieved in order to optimize the circuit performance. The Silicon-On-Insulator (SOI) fabrication process is quickly becoming the answer to the technical challenges facing the integrated circuits (IC) industry.

## REFERENCES

- [1]. SILICON ON INSULATOR TECHNOLOGY REVIEW Rahul Kr. Singh, Amit Saxena, Mayur Rastogi International Journal Of Engineering Sciences & Emerging Technologies May 2011. ISSN: 2231 – 6604 Volume 1, Issue 1, Pp: 1-16 ©IJESSET
- [2]. SPECIAL REPORT SOI Wafer Technology For CMOS Ics Robert Simonton President, Simonton Associates
- [3]. [Www.Chips.Ibm.Com/Bluelogic](http://www.chips.ibm.com/bluelogic)
- [4]. J.P. Colinge, “SILICON-ON-INSULATOR TECHNOLOGY: Materials To VLSI, Second Edition”, Kluwer Academic Publishers, 1997, Chapters 4 & 5.
- [5]. TEMPERATURE-DEPENDENT KINK EFFECT MODEL FOR PARTIALLY-DEPLETED SOI NMOS DEVICES S. C. Lin And J. B. Kuo
- [6]. RELIABILITY EVALUATION OF FULLY DEPLETED SOI (FDSOI) TECHNOLOGY FOR SPACE APPLICATIONS. Ashok K. Sharma NASA/GSFC, Greenbelt, MD Alexander Teverovsky QSS Group,
- [7]. S.Crisoloveanu, “ELECTRICAL CHARACTERIZATION OF SOI MATERIALS AND DEVICES”, Kluwer Academic Publishers, 1995.
- [8]. S.Crisoloveanu, “SOI TECHNOLOGIES, MATERIALS AND DEVICES,” 1996 IEEE International SOI Conference, 1996, Pp. 3-12.
- [9]. M.I. Current, S.W. Bedell, I.J. Malik, L.M. Feng, F.J. Henley, “WHAT IS THE FUTURE OF SUB-100NM CMOS: ULTRA SHALLOW JUNCTIONS OR ULTRATHIN SOI?”, Solid State Technology, V.43, N9, September, 2000
- [10]. R. Berger, J. Burns, C-L Chen, C. Chen, M. Fritze, P. Gouker, J. Knecht, A. Soares, V. Suntharalingam, P. Wyatt, D-R Yost, Craig L. Keast, “LOW POWER, HIGH PERFORMANCE, FULLY DEPLETED SOI CMOS TECHNOLOGY”, DARPAJMT0 AME Review, 31 August, 1999.
- [11]. S.Crisoloveanu, “Architecture Of SOI Transistors: What’s Next?”, 2000 IEEE International SOI Conference, 2000, Pp. 1-2.
- [12]. Ying-Che Tseng; W. Margaret Huang, David J. Monk, P. Welch, J. M. Ford, J.S. Woo, “AC Floating Body Effects And The Resultant Analog Circuit Issues In Submicron Floating Body And Body- Grounded SOI MOSFET's,” IEEE Transactions On ED, V.46, N 8, August 1999
- [13]. 0.5 Mw Sub-Threshold Operational Transconductance Amplifiers Using 0.15 Mm Fully Depleted Silicon-On-Insulator (FDSOI) Process Piotr Olejarz 1, Kyoungchul Park 2, Samuel Macnaughton 2, Mehmet R. Dokmeci 3 And Sameer Sonkusale 2,\*
- [14]. Chi-Hon Ho, Jun-Yi Pon, And Yao-Tsung Tsai\* “THE BRANCH-CUT METHOD AND ITS APPLICATION TO PARTIALLY DEPLETED SOI MOSFET SIMULATION FOR KINK EFFECT DEFINITION” *Journal Of The Chinese Institute Of Engineers, Vol. 31, No. 7, Pp. 1219-1224 (2008) 1219*
- [15]. Jeong-Hyong Yi, Young-June Park And Hong Shick Min “ANALYTICAL MODEL FOR AND SCALE-DOWN EFFECT OF A FLOATING BODY VOLTAGE IN SOI MOSFETS”*Journal Of The Korean Physical Society, Vol. 40, No. 4, April 2002, Pp. 668\_671*
- [16]. B. Cheng, V. Ramgopal Rao, And J.C.S. Woo, “Sub 0.18 Um SOI Mosfets Using Lateral Asymmetric Channel Profile And Ge Pre-Amorphization Salicide Technology,” *Proceedings Of The IEEE SOI Conference*, October 5-8, Stuart, Florida, USA, 1998.
- [17]. S.M. Sze, “*Physics Of Semiconductor Devices*,” 2nd Ed., New York, J. Wiley & Sons,
- [18]. 1981 M. Y. Hammad, “Analytical Modeling Of The Partially-Depleted SOI MOSFET,” IEEE Transactions On Electron Devices, Vol. 48, No. 2, Pp. 252–258, 2001. [View At Publisher](#) · [View At Google Scholar](#) · [View At Scopus](#)
- [19]. N. Annamalai And M. Biwer, "Leakage Current In SOI Mosfets", IEEE Trans. On Nuclear Science, Vol. 35, Pp. 1372 - 1378, 1988
- [20]. Y Omura And K. Izumi, "Simplified Analysis Of Body-Contact Effect For MOSFETISOI", IEEE Trans. On Electron Devices, Vol. 35, Pp. 1391 - 1393, 1988.
- [21]. J. Sleight And K. Mistry, "A Compact Schottky Body Contact Technology For SOI Transistors" International Electron Devices Meeting, (IEDM) Digest, Pp. 4 19 - 422. 1997.
- [22]. S. Cristoloveanu, And S.S. Li, “*Electrical Characterization Of Silicon-On-Insulator Materials And Devices*,” Kluwer Academic Publishers, 1995.
- [23]. C.E.D. Chen, M. Matloubian, R. Sundaresan, B.Y. Mao, C.C. Wei, And G.P. Pollack, “Single Transistor Latch In SOI MOSFET’s,” *IEEE Electron Device Lett.*, Vol. 9, P. 636, 1988.
- [24]. H. C. De Graaff And F. M. Klaassen, “*Compact Transistor Modelling For Circuit Design*,” Springer-Verlag, 1990.
- [25]. M. D. Jacunski, M. S. Shur, A. A. Owusu, T. Ytterdal, M. Hack And B. Iniguez, “A Short Channel DC SPICE Model For