

Design and Simulation of Dynamic voltage restorer (DVR) using SPWM and SVPWM Techniques for Voltage Sags & Voltage Swells Mitigation

G Mohan¹ (M.Tech), Prof. A Lakshmi Devi²

¹DEPARTMENT OF E.E.E, SVUCE, TIRUPATI, INDIA

²DEPARTMENT OF E.E.E, SVUCE, TIRUPATI, INDIA

ABSTRACT: This paper presents design and simulation of Dynamic voltage restorer(DVR) using sinusoidal pulse width modulation (SPWM) & space vector pulse width modulation(SVPWM). It describes the problems of voltage sags & swells and its severe impact on nonlinear loads (or) sensitive loads. DVR is a series connected device used for compensating the voltage sags & swells in distribution system. The detection of sags/swells is carried out with the help of dq0 theory, whereas the control of voltage source inverter is done with help of SPWM & SVPWM. This paper compares the total harmonic distortion(THD) of the DVR using SPWM & SVPWM. The simulation was carried out with the help of SIMULINK & MATLAB and the results were found to be in accordance with theoretical values.

Keywords: Dynamic voltage restorer (DVR), sinusoidal pulse width modulation (SPWM), space vector pulse width modulation (SVPWM),dq0 theory, voltage sag/swell.

I. INTRODUCTION

The term power quality is something that describes the quality of power, it is the quality of voltage rather than power (or)current. Power Quality problems encompass a wide range of disturbances such as voltage sags/swells, flicker, harmonics distortion, impulse transient, and interruptions .Because of the voltage deviation the electrical utility is not able to supply the pure sinusoidal voltage of required magnitude and frequency. Voltage sags can occur at any instant of time, with amplitudes ranging from 10 – 90% and a duration lasting for half a cycle to one minute .Voltage swell, on the other hand, is defined as a swell is defined as an increase in rms voltage or current at the power frequency for durations from 0.5 cycles to 1 min. typical magnitudes are between 1.1 and 1.8 up. These voltage problems can be solved using a series connected custom power device called dynamic voltage restorer(DVR). The emphasis has been given for switching control strategy i.e, pulse width modulation techniques and their results are presented.

II. DVR

The main function of a DVR[1] is the protection of sensitive loads from voltage sags/swells coming from the network The following steps are used to implement the DVR in injection mode.

Step 1: To find out whether there is any sag/swell in the source voltage. It is done by comparing the terminal source voltages with reference load voltages. The difference between the source voltages and reference load voltages is the required amount of voltage that has to be injected by the DVR.

Step 2: To generate switching commands to the VSI in order to track the reference voltages (generated in step 1) using a suitable switching scheme such as PWM.

Step 3: To filter out the harmonics that are present in the output of the voltage source inverter.

Step 4: To inject the filtered output through the three single phase series isolation transformers present between the source and the load.

Following above mentioned steps, the DVR should work only if there is any difference between the terminal source voltage and the load voltage. To implement above steps, the following building blocks are required to realize the DVR.

- i. Detection and control block
- ii. Voltage source inverter
- iii. Filter components
- iv. Isolation transformers

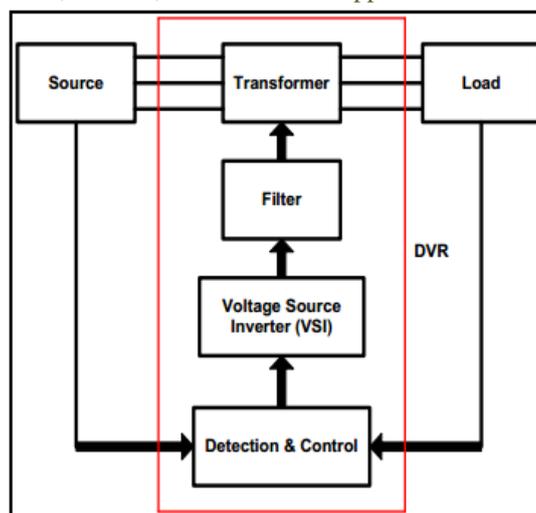


fig2.1: Block diagram of DVR

III. PWM TECHNIQUES

There are two types pulse width modulation (PWM) techniques used in this dynamic voltage restorer

3.1 Sinusoidal pulse width modulation (SPWM)

The most common PWM strategy for a two-level phase leg is a "sine-triangle" comparison of a (sinusoidal) low-frequency fundamental reference waveform against a high-frequency carrier waveform. The phase leg switches to the upper or the lower dc rail supply, depending on whether the reference waveform is greater or less than the carrier waveform. The carrier waveforms are classified as triangular, saw-tooth, trapezoidal. Triangular waveforms are most popular and used for PWM. The SPWM[2] technique has been widely used in conventional two-level inverter due to its simplicity and low distortion characteristics.

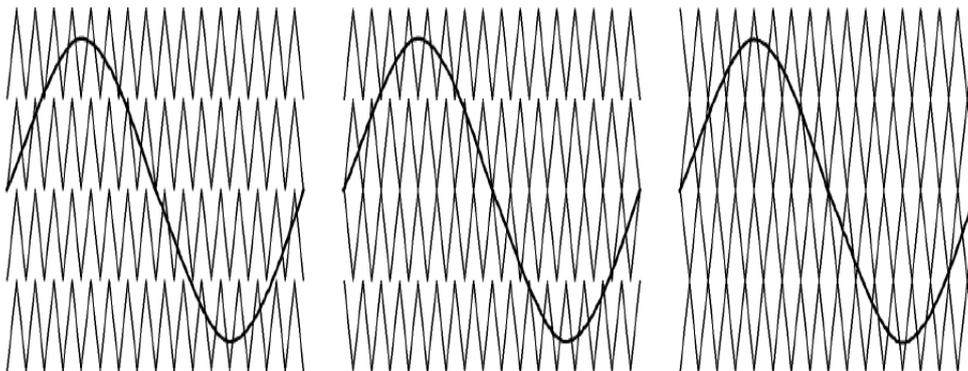


Fig3.1: Carrier (triangular) and reference (sinusoidal) waveform for five-level inverter.

3.2 space vector pulse width modulation (SVPWM)

Space vector PWM[3] refers to a switching scheme of the six power switches of a 3-phase VSI. It generates minimum harmonic distortion and also provides more efficient use of DC supply voltage in comparison with the sinusoidal modulation method. SVPWM treats the inverter as a single unit. Specifically the inverter can be driven to eight unique states. Modulation is accomplished by switching the state of inverter. Space vector pulse width modulation treats the sinusoidal voltage as a constant amplitude vector rotating at constant frequency.

In a two level three phase inverter total eight (2^3) vectors are possible among those six are non-zero vectors and two are zero vectors. Six non-zero vectors (V_1 - V_6) shape the axes of a hexagonal as depicted in Fig. 3.2, supplies power to the load. The angle between any adjacent two non-zero vectors is 60 degrees. Meanwhile, two zero vectors (V_0 and V_7) and are at the origin and apply zero voltage to the load. The eight vectors are called the basic **space vectors** and are denoted by ($V_0, V_1, V_2, V_3, V_4, V_5, V_6, V_7$). The same transformation can be applied to the desired output voltage to get the desired reference voltage vector, V_{ref} in the d-q plane. The objective of SVPWM technique is to approximate the reference voltage vector V_{ref} using the eight switching patterns. One simple method of approximation is to generate the average output of the inverter in a small period T_Z to be the same as that of V_{ref} in the same period.

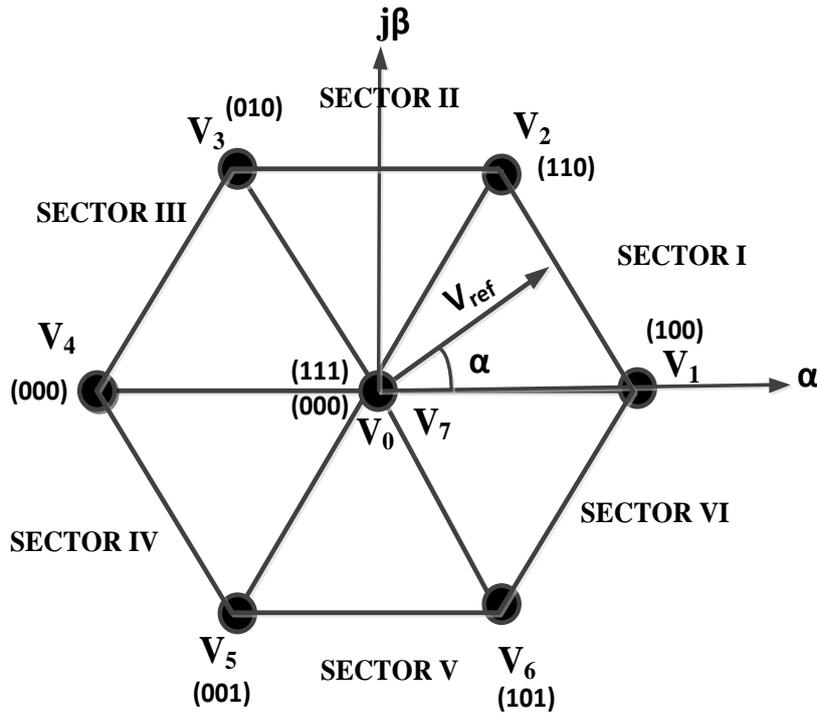


Fig. 3.2: Two-level space vector diagram

IV. SIMULATION RESULTS AND DISCUSSION

The designed DVR is used to compensate sags/swells of magnitude in the range (0.1p.u - 0.9 p.u). But in reality a DVR can compensate a maximum of 0.5p.u. For the purpose of demonstration sag of magnitude 0.2 p.u and a swell of magnitude 0.2 p.u are considered. The VSI is implemented using both SPWM as well as SVPWM and the results were compared

Table1:parameter values for simulation

Parameter	Value
RMS line-to-line voltage	400V
Resistance and Inductance of the line	0.1Ω,0.5mH
Transformer turns ratio	1: 1
Transformer no load losses	0.002p.u
Filter parameters	R=5Ω ; C=1μF; L=10mH
Active and Reactive power of load	1000W,200W
Line frequency	50HZ

4.1 voltage sags:

4.1.1:spwm waveforms

The first simulation shows of three phase voltage sag is simulated. The simulation started with the supply voltage 20% sagging as shown in Figure 3.1.1 (a).In Figure 3.1.1 (a) also shows a 20% voltage sag initiated at 0.2s and it is kept until 0.8s, with total voltage sag duration of 0.6s. Figures 3.1.1 (b) and (c) show the voltage injected by the DVR and the corresponding load voltage with compensation. As a result of DVR, the load voltage is kept at 1 p.u.

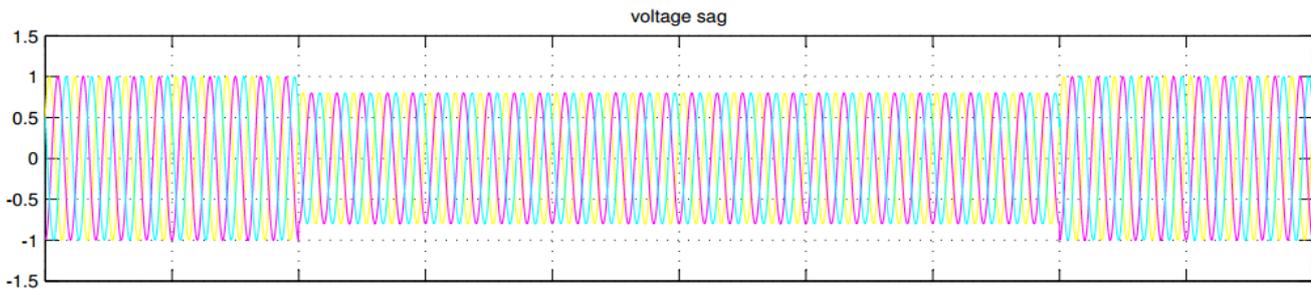


fig 4.1.1 (a):voltage sag of 0.2 p.u

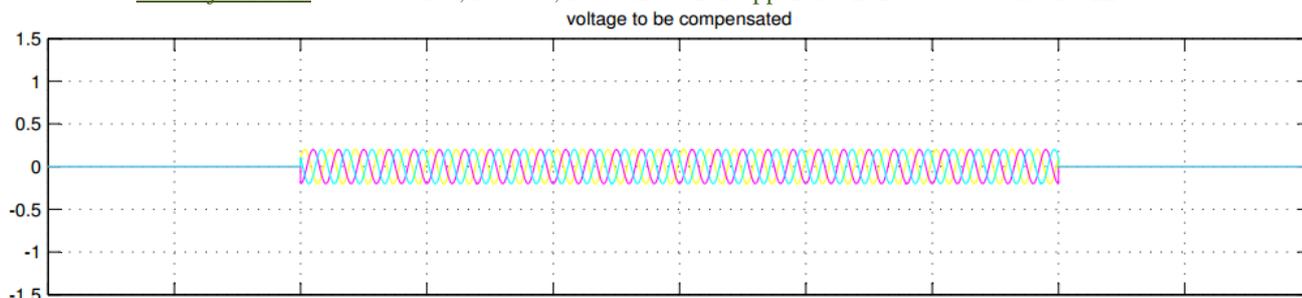


fig 4.1.1 (b): injected voltage

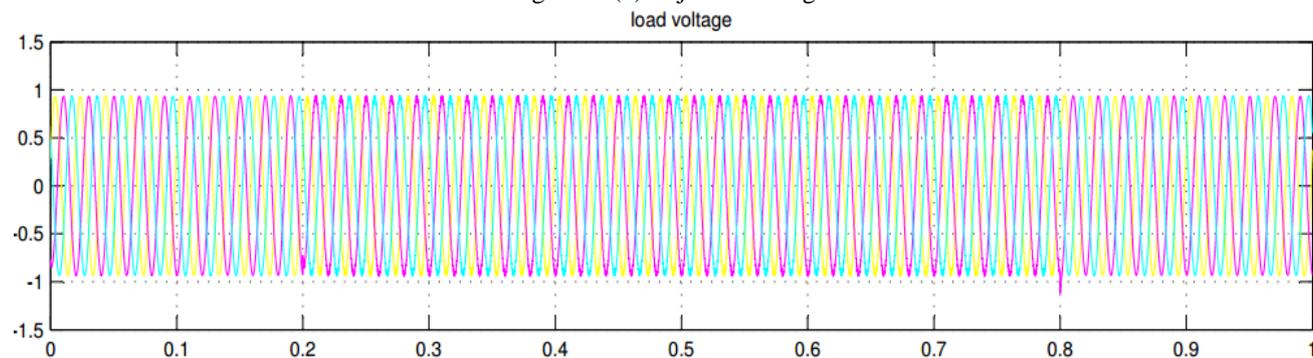


fig 4.1.1(c):load voltage

4.1.2:svpwm waveforms

The first simulation shows of three phase voltage sag is simulated. The simulation started with the supply voltage 20% sagging as shown in Figure 3.1.2 (a). In Figure 3.1.2 (a) also shows a 20% voltage sag initiated at 0.2s and it is kept until 0.8s, with total voltage sag duration of 0.6s. Figures 3.1.2 (b) and (c) show the voltage injected by the DVR and the corresponding load voltage with compensation. As a result of DVR, the load voltage is kept at 1 p.u.

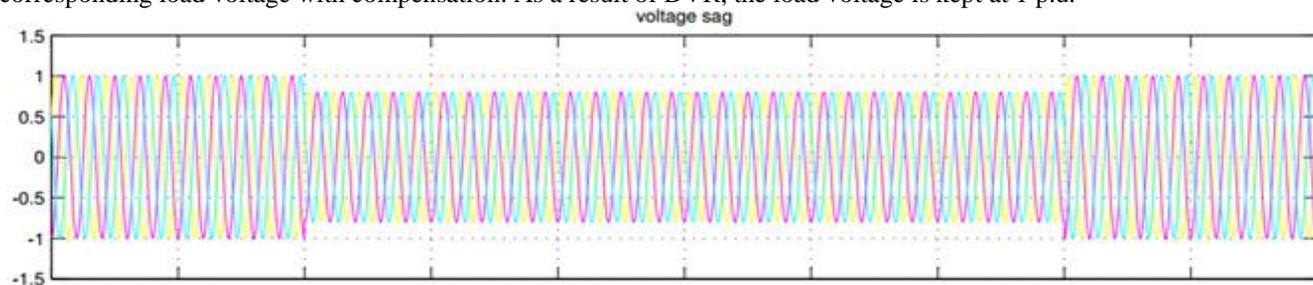


fig 4.1.2 (a):voltage sag of 0.2 p.u

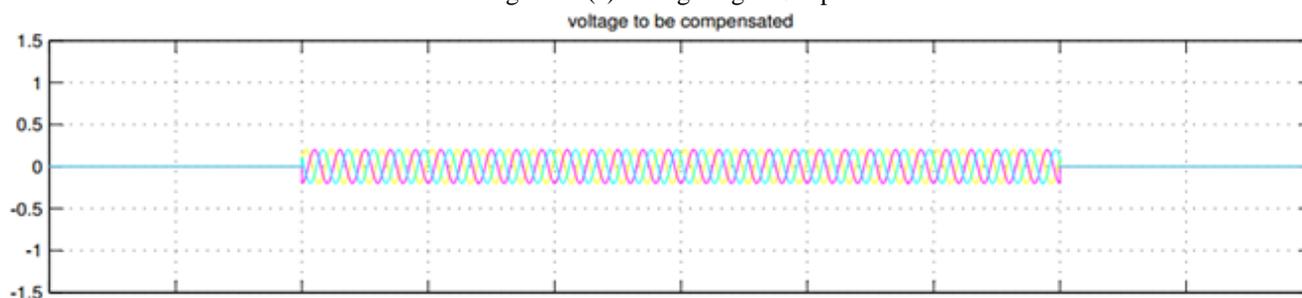


fig 4.1.2 (b): injected voltage

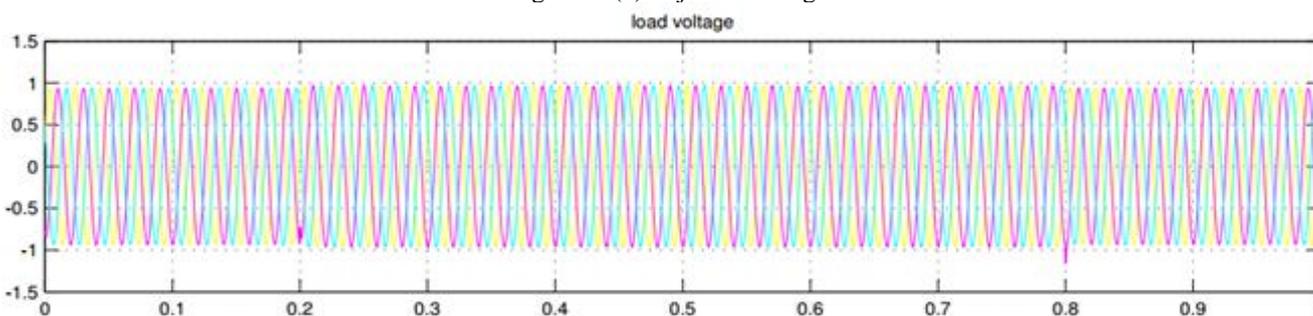


fig 4.1.2(c):load voltage

4.2 voltage swells:**4.2.1: spwm waveforms**

The first simulation shows of three phase voltage swell is simulated. The simulation started with the supply voltage 20% swell as shown in Figure 3.2.1 (a). In Figure 3.2.1 (a) also shows a 20% voltage swell initiated at 0.2s and it is kept until 0.8s, with total voltage sag duration of 0.6s. Figures 3.2.1 (b) and (c) show the voltage injected by the DVR and the corresponding load voltage with compensation. As a result of DVR, the load voltage is kept at 1 p.u.

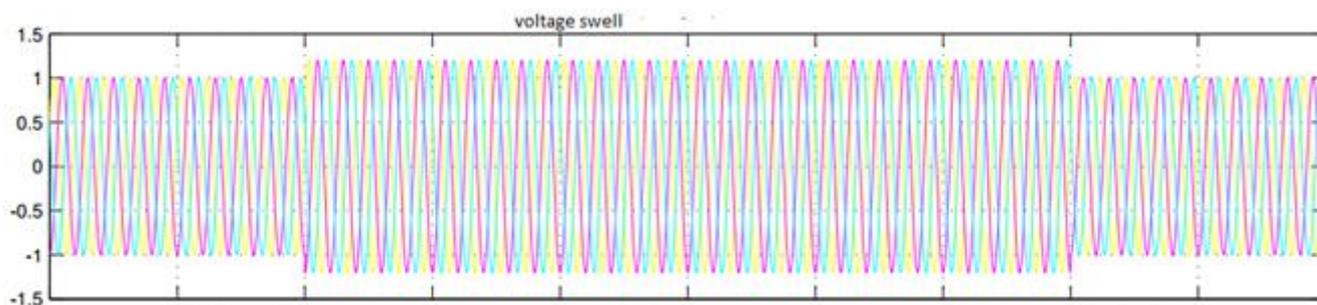


fig 4.2.1 (a):voltage swell of 0.2 p.u

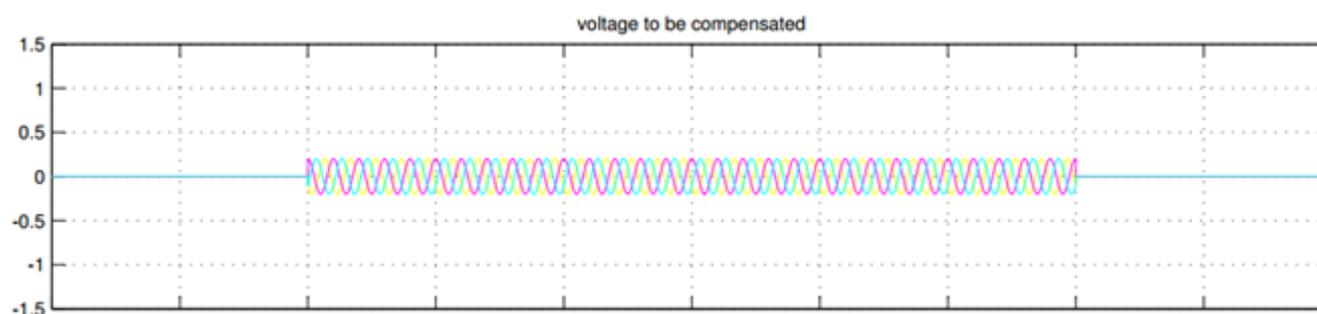


fig 4.2.1 (b): injected voltage

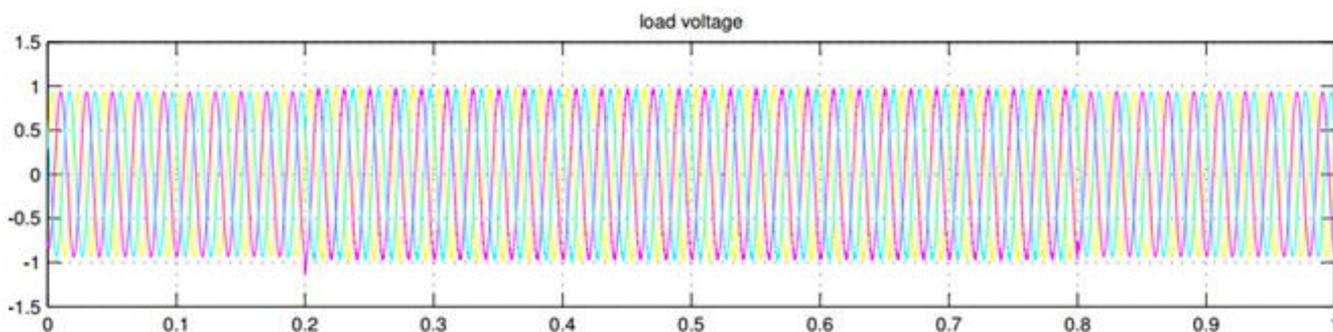


fig 4.2.1(c):load voltage

4.2.2:svpwm waveforms

The second simulation shows of three phase voltage swell is simulated. The simulation started with the supply voltage 20% swell as shown in Figure 3.2.2 (a). In Figure 3.2.2 (a) also shows a 20% voltage swell initiated at 0.2s and it is kept until 0.8s, with total voltage sag duration of 0.6s. Figures 3.2.2 (b) and (c) show the voltage injected by the DVR and the corresponding load voltage with compensation. As a result of DVR, the load voltage is kept at 1 p.u.

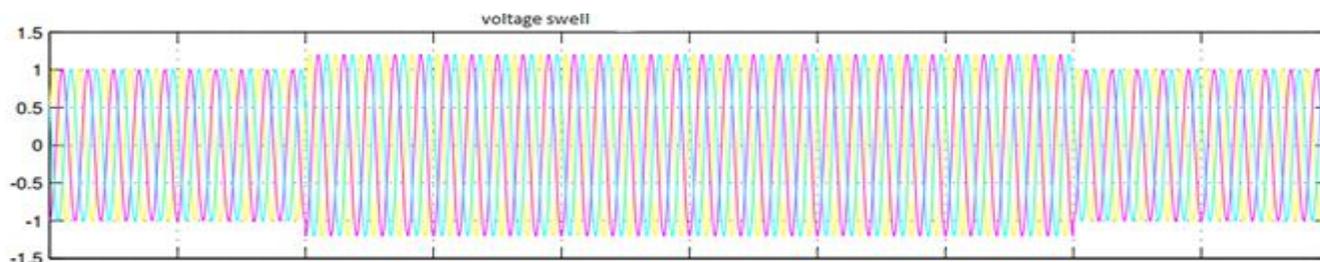


fig 4.2.2 (a):voltage swell of 0.2 p.u

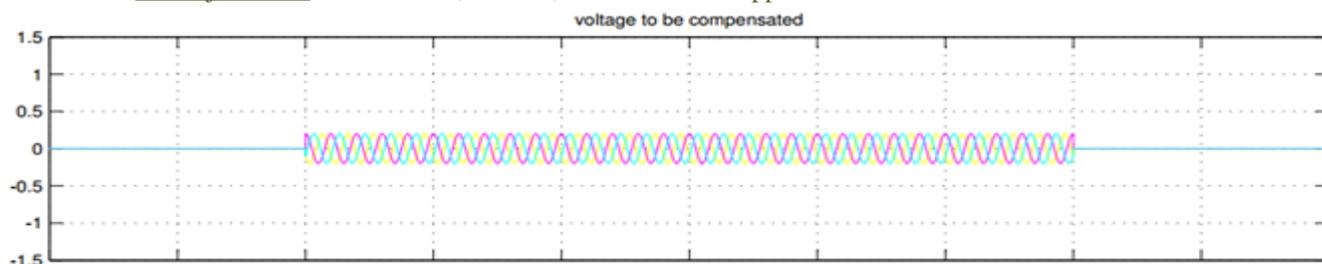


fig 4.2.2 (b): injected voltage

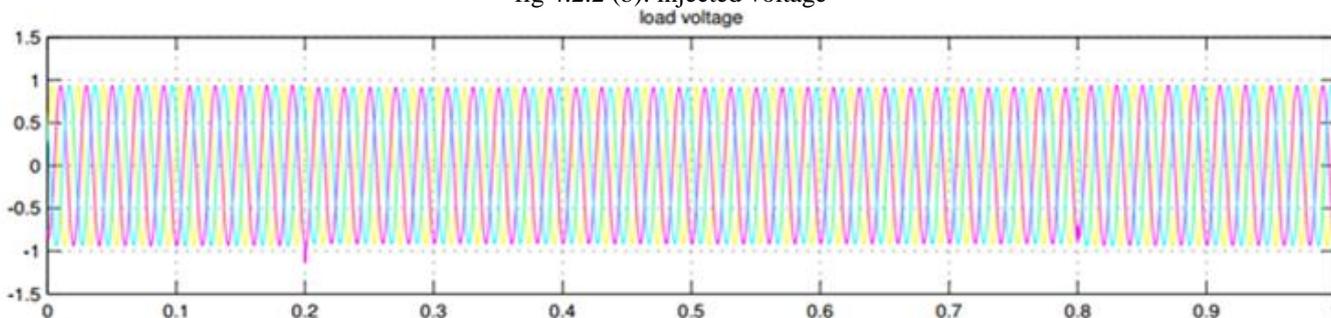


fig 4.2.2 (c): load voltage

4.3:FFT analysis of spwm & svpwm

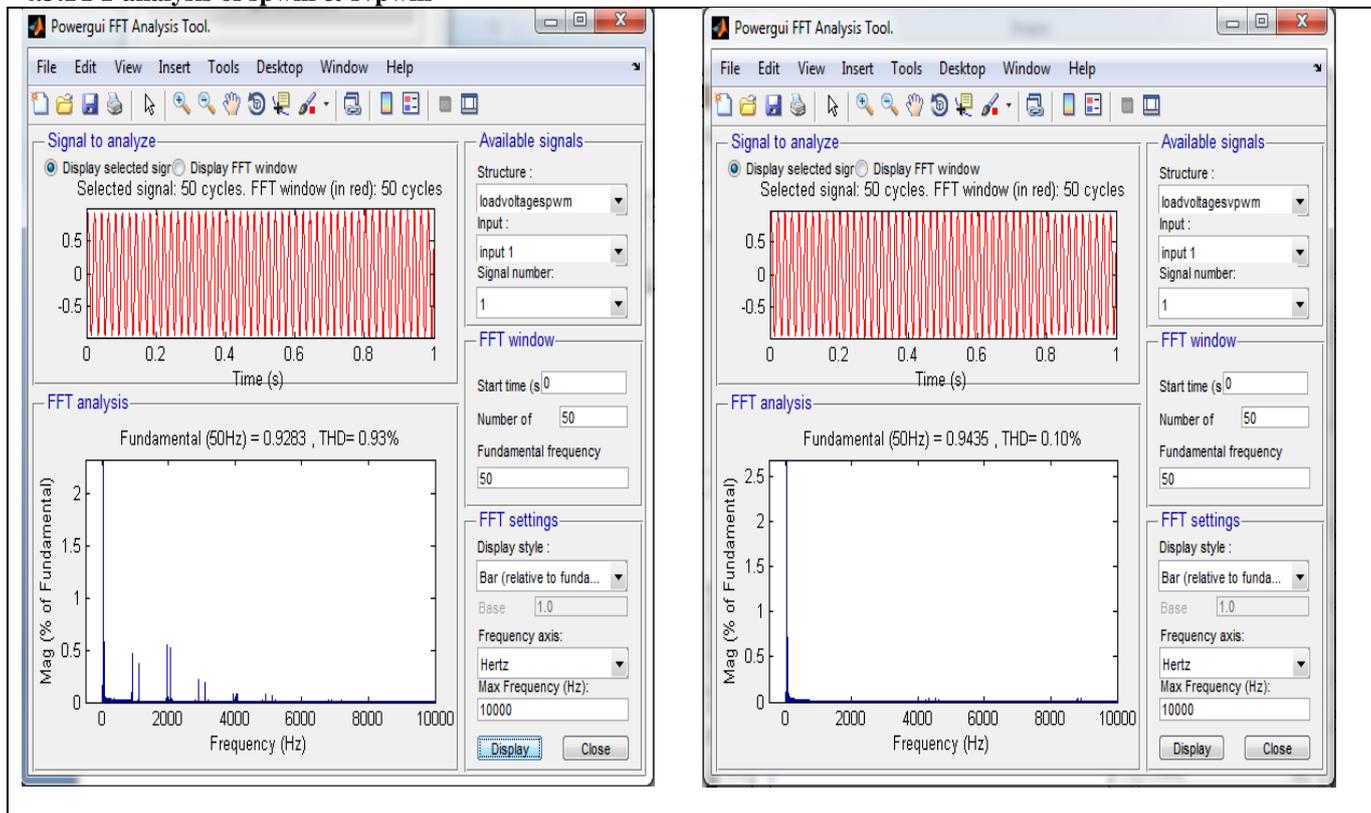


fig4.3.1: waveforms of showing the FFT analysis of load voltage of spwm & svpwm

Table 2: Comparison of THD values in SPWM & SVPWM

S.NO	Waveform	THD in SPWM(%)			THD in SVPWM(%)		
		Sag	Swell	Sag&Swell	Sag	Swell	Sag&Swell
1	inverter output voltage	163.74	163.56	223.96	89.56	89.54	125.76
2	filter output voltage	11.34	4.49	9.94	0.35	0.35	1.04
3	Source voltage	0.00	0.00	0.00	0.00	0.00	0.00
4	load voltage	1.10	1.08	0.93	0.09	0.09	0.1

From the FFT analysis it is clear that the harmonic presents in the inverter output voltage & filter output voltage are low in case of space vector pulse vector pulse width modulation (SVPWM) than the sinusoidal pulse width modulation

V. CONCLUSION

The modelling and simulation of DVR using MATLAB/SIMULINK has been presented. The performance of DVR is studied under voltage Sag & Swells by using SPWM and SVPWM Techniques. From the simulation results DVR compensates Sags & Swells quickly and provides better voltage regulation in both the cases. Space Vector PWM effectively restored the voltage of Sensitive load to normal and reduced the harmonic distortion in load voltage when compared with Sinusoidal PWM. The Simulation study reveals that SPWM requires 15% more dc voltage when compared to SVPWM for the same output. For the compensation of same amount of voltage Sags & voltage Swells SVPWM requires less amount of dc voltage when compared to SPWM. So by using SVPWM technique dc voltage required for inverter is less when compared to Sinusoidal PWM technique in order to generate same amount of output. The harmonics content in the output voltage is reduced by using Space Vector PWM technique as compared to SPWM technique.

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SIMULATION DIAGRAM:

