International Journal of Modern Engineering Research (IJMER)
www.ijmer.com Vol. 3, Issue. 6, Nov - Dec. 2013 pp-3544-3551 ISSN: 2249-6645

Performance Analysis of Z-Source Cascaded H-Bridge Multilevel Inverter Based on Multi Carrier PWM Techniques

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ABSTRACT : *Multilevel inverter is one of the attractive topology for dc to ac conversion. Multilevel inverter synthesizes desired voltage wave shape from several levels of DC voltages. But the main drawback of MLI is its output voltage amplitude is limited to DC sources voltage summation. To overcome this limitation, a five-level Z-source cascaded H-bridge multilevel inverter has been proposed in this paper. In the proposed topology output voltage amplitude can be boosted with Z network shoot-through state control. It employs Z network between the DC source and inverter circuitry to achieve boost operation. The output voltage of proposed inverter can be controlled using modulation index and shoot through state. Performance parameters of Z -Source MLI have been analyzed for unipolar modulation and space vector modulation. Simulation model of Z-source cascaded multilevel inverter with unipolar ISCPWM, unipolar CDPWM and SVM Modulation technique has been built in MATLAB/SIMULINK and its performance has been analyzed.*

Keywords: *Multi Level Inverter, Total Harmonic Distortion, Pulse Width Modulation, Shoot-Through, Buck-Boost.*

I. INTRODUCTION

Multilevel inverters are widely used in high power applications such as large induction motor drives, UPS systems and Flexible AC Transmission Systems (FACTS). Multilevel inverter obtains the desired output voltage from several levels of input DC voltage sources. By increasing the number of DC voltage sources, the inverter output voltage level increases. The multilevel inverters have advantages such as lower semiconductor voltage stress, better harmonic performance, low Electro Magnetic Interference (EMI) and lower switching losses. Despite these advantages, multilevel inverters output voltage amplitude is limited to the input DC sources voltage summation. It requires an intermediate DC to DC converter is for the buck or boost operation of MLI output voltage. Also occurring of short circuit can destroy multilevel inverters. In this paper multilevel inverter based Z-source is proposed which can solve above mentioned problems.The Z-source inverter utilizes Z impedance network between the DC source and the inverter circuit to achieve buck-boost operation. It utilizes shoot-through state control to boost the input dc voltage of inverter switches when both switches in the same phase leg are on. The Z-Source inverters have advantages such as lower costs, reliable, lower complexity and higher efficiency.
The ac output voltage can be of fixed or variable frequency. This can be achieved either by controlled turn-on and turn-off devices (e.g., BJTs, MOSFETs, IGBTs, and GTOs) or by forced commutated thyristors, depending on applications. The output voltage waveforms of an ideal inverter must be sinusoidal. The voltage waveforms of practical inverters are non-sinusoidal and contain certain harmonics. The output frequency of an inverter is determined by the rate at which the semiconductor devices are switched on and off by the control circuit and can provide ac output of adjustable frequency. The dc input to the inverter may be a battery, fuel cell, solar cells or other dc sources. But in case industrial applications, it is fed by a rectifier.

In this paper, a single phase cascaded H-bridge five levels Z-Source inverter is proposed for renewable energy systems and it employs Z network between the DC source and inverter circuitry to achieve boost operation. The output voltage inverter can be controlled using modulation index and shoot through state control. Cascaded Z-Source Multilevel inverter is analyzed with unipolar inverse sine carrier, unipolar carrier disposition PWM, SVM techniques. Performance parameters have been analyzed for cascaded Z-Source MLI. The performances of the three techniques are compared for single phase 5-level Z-Source cascaded multilevel inverter. Simulation of the circuit configurations have been performed in

II. MATLAB/SIMULINK.

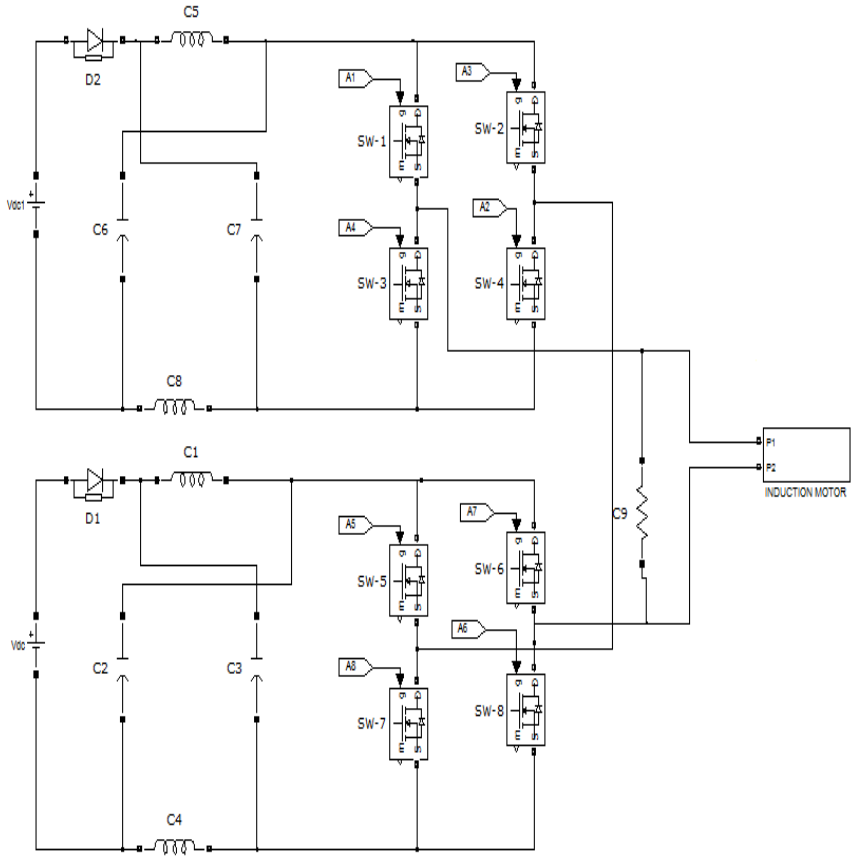

Fig.1Single phase 5-level z-source cascaded multilevel inverter

III. Z-SOURCE CONVERTER

To overcome the problems of the traditional Voltage and current source converters, this paper presents an impedance source (or impedance-fed) power converter (abbreviated as Z-source converter) and its control method for implementing dc-to-ac power conversion [4]. It employs a unique impedance network (or circuit) to couple the inverter main circuit to the power source for providing unique features that cannot be observed in the traditional Voltage and current source converters where a capacitor and inductor are used, respectively. The Z-source converter overcomes the above-mentioned limitations of the traditional Voltage and current source converter and provides a novel power conversion concept [2].In Fig. 2, a two-port network that consists of a split-inductor L1 and L2 and capacitors C1 and C2connected in X shape is employed to provide an impedance source (Z-source) coupling the converter (or inverter) to the dc source. The dc source/or load can be either a voltage or a current source/or load. Therefore, the dc source can be a battery, diode rectifier, thyristor converter, fuel cell, an inductor, a capacitor, or a combination of those [3]. Switches used in the converter can be a combination of switching devices and diodes such as the antiparallel combination, the series combination etc.

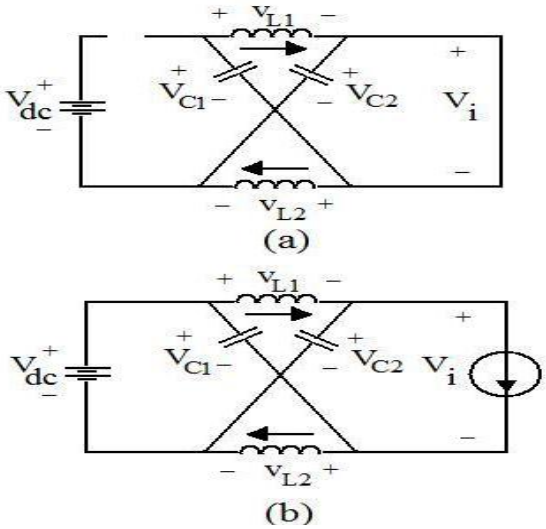

Fig.2 (a) Full shoot-through and (b) non-shoot-through equivalent circuits

The Z-source concept can be applied to all dc-to-ac, ac-to-dc, ac-to-ac, and dc-to-dc power conversion. To describe the operating principle and control, this paper focuses on an application example of the Z-source converter: a Z-source inverter for dc-ac power conversion needed for fuel-cell applications. The diode in series with the dc source is for preventing reverse current flow.

IV. CASCADED MULTILEVEL INVERTER TOPOLOGY

Cascaded multilevel inverters are made from series connected full bridge inverters, each with their own isolated dc bus. This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources. This type of converter does not need any transformer or clamping diodes or flying capacitors.Each level generates three different voltage outputs +Vdc, 0 and –Vdc by connecting the dc sources to the ac output side by different combinations of the four switches. The output voltage of multilevel inverter is the sum of all the individual inverter outputs. Each of the H-bridge's active devices switches only at the fundamental frequency, and generates a quasi-square waveform by phase-shifting its positive and negative phase legs switching timings. Further, each switching device always conducts for 180˚ (or half cycle) regardless of the pulse width of the quasi-square wave. This switching method results in equalizing the current stress in each active device.This topology of inverter is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency. Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work. A multilevel inverter has four main advantages firstly; the voltage stress on each switch is decreased due to series connection of the switches therefore, the rated voltage and consequently the total power of the inverter could be safely increased. Second, the rate of change of voltage (dV/dt) is decreased due to the lower voltage swing of each switching cycle. Third, harmonic distortion is reduced. Fourth, lower acoustic noise and electromagnetic interference (EMI) is obtained.

VOLTAGE LEVEL OUTPUT	VOLTAGE	ON SWITCHES
Level 2 (non shoot-through)	2Vin	S3,S4,S5,S6
Level 1 (non shoot-through)	Vin	S1,S3,S5,S6
Level 1(shoot-through)	Vin	S1,S2,S3,S4, S5,S6
Level 1 (non shoot-through)	Vin	S3,S4,S5,S7
Level 1(shoot-through)	Vin	S3,S4,S5,S6, S7,S8
Level 0 (zero state)	0V	S1,S3,S5,S7
Level 0 (shoot-through)	0V	S1,S2,S3,S4, S5,S7
Level 0 (shoot-through)	0V	S1,S3,S5,S6, S7,S8
Level -1 (non shoot-through)	-Vin	S1,S3,S7,S8
Level -1 (shoot-through)	-Vin	S1,S2,S3,S4, S7,S8
Level -1 (non shoot-through)	-Vin	S1,S2,S7,S8
Level -1 (shoot-through)	-Vin	S1,S2,S5,S6, S7,S8
Level -2 (non shoot-through)	-2Vin	S1,S2,S7,S8

Table 1Conduction Table

V. MODELLING OF CASCADED H-BRIDGE INVERTER

For each full bridge inverter the output voltage is given by

Voi=Vdi(S1i-S2i) (1)
and the input dc current is
Idci=Ia(S1i-S2i) (2)

where,
(a) i =1,2.. Number of full bridge inverters employed.
(b) I_a is the output current of the cascaded inverter.
(c) S1i and S2i is the upper switch of each full bridge inverter.

Now the output voltage of each phase of the multilevel cascaded inverter is given by:
Von=∑ Voi , i = 1, 2....n (3)

VI. CONTROL SCHEMES

The main aim of the modulation strategy of multilevel inverters is to synthesize the output voltage as close as possible to the sinusoidal waveform. Many modulation techniques have been developed for harmonic reduction and switching loss minimization. Multilevel inverter control techniques are based on fundamental and high switching frequency. Another widely used popular classification for the modulation methods developed to control the multilevel inverters is depend upon open loop and closed loop concepts.

A.UNIPOLAR-MCPWM technique

It is obtained by comparing the rectified sinusoidal reference or with two sine references (sine and 180 degree phase shifted sine), with multi carriers positioned above the zero level. This scheme has the advantage of effectively doubling the switching frequency as far as the output harmonics are concerned, where the lowest harmonics appears as side bands of twice switching frequency. Here only n carriers are required for obtaining 2n+1 level, unlike in above methods 2n+1 carriers are required.

1. UNIPOLAR-ISCPWM [inverted sine carrier PWM]:-

The control scheme uses an inverted (high frequency) sine carrier that helps to maximize the output voltage for a given modulation index. Enhanced fundamental component demands greater pulse area. The difference in pulse widths (hence area) resulting from triangle wave and inverted sine wave with the low (output) frequency reference sine wave can be easily understood.

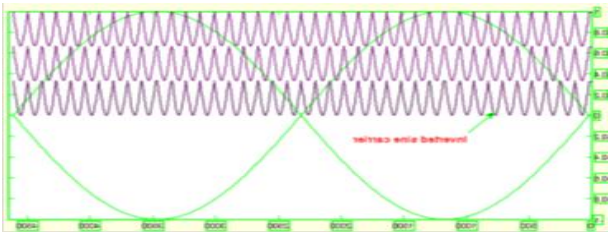

Fig.3 Unipolar-ISCPWM

2. UNIPOLAR-CDPWM: -

In this method four phase shifted carrier triangular signals are compared with the two modulating sinusoidal signals to produce switching PWM pulses. This method employs two straight lines that are greater than or less than the peak value of the reference sinusoidal signal to control the shoot-through duty ratio. Inverter operates in shoot-through whenever the triangular carrier signal is higher than the positive straight line or lower than the negative straight line. The frequency of the modulating signal is taken as 50Hz. The frequency of the triangular signal can be calculated by Frequency modulation index, mf which is given.

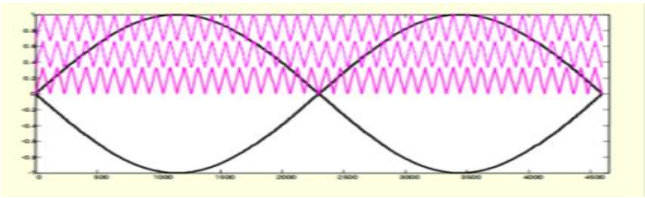

Fig.4 Unipolar CDPWM

For each full bridge inverter the output voltage is given by
"mf=" fc/fo (4)

where fc is the frequency of the carrier signal and fo is the frequency of sinusoidal and modulating signals. Output voltage depends on the boost factor

B=1/(1-(2(Vca-Vp))/Vca)=1/(1-2Tsh/T) (5)

where,

Vca - Peak value of the triangular waveform

V p - Amplitude of the constant

Tsh - Total shoot-through state period

T - Period of switching

3. SPACE VECTOR MODULATION:-

The SVM technique can be easily extended to all multilevel inverters [13]–[19]. Fig. 5 shows space vectors for the traditional two-, three-, and five-level inverters. These vector diagrams are universal regardless of the type of multilevel inverter. In other words, Fig.5(c) is valid for five-level diode-clamped, capacitor-clamped, or cascaded inverter. The adjacent three vectors can synthesize a desired voltage vector by computing the duty cycle (Tj,Tj+1,and Tj+2) for each vector

V*=((TjVj+Tj+1Vj+1+Tj+2Vj+2))/T (6)

Space-vector PWM methods generally have the following features: good utilization of dc-link voltage, low current ripple, and relatively easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high-voltage high-power applications. As the number of levels increases, redundant switching states and the complexity of selecting switching states increase dramatically. Some authors have used decomposition of the five level space-vector diagram into two three-level space-vector diagrams with a phase shift to minimize ripples and simplify control [16]. Additionally, a simple space-vector selection method was introduced without duty cycle computation of the adjacent three vectors.

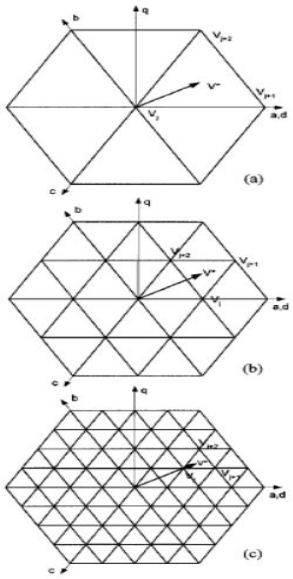

Fig.5. Space-vector diagram: (a) two-level, (b) three-level, and (c) five-level inverter.

VII. SIMULATION AND EXPERIMENTAL RESULTS

Fig.6 shows Matlab Simulink of Z-Source cascaded MLI using Unipolar PWM with Boost factor = 1.25, ma=0.8, RLoad where R=100Ω , Input voltage V dc=100V, Z impedances, L]=L2=L3=L4=L=1000mH and C]= C2= C3= C4= 10mF . Simulink circuit is shown with LC filter having. This LC filter can act as an electrical resonator, an electrical analogue of a tuning fork, storing electrical energy oscillating at the circuit's resonant frequency.

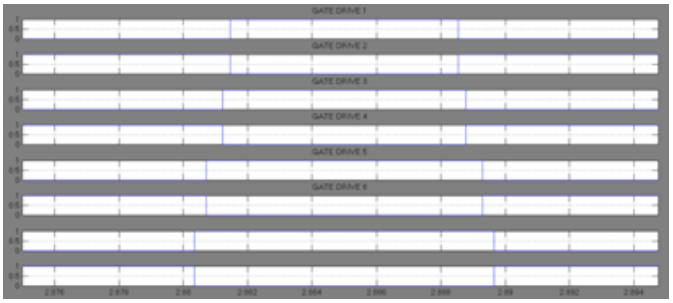

Fig.6 PWM pulse generation for unipolar PWM technique

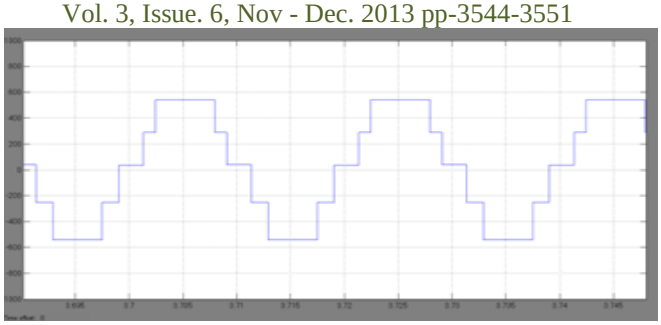

Fig.7 Output voltage of unipolar multicarrier techniques without filter

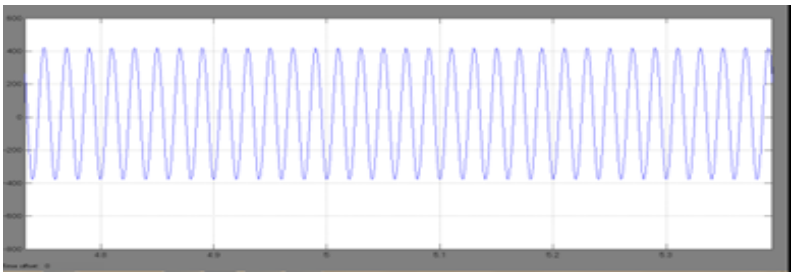

Fig.8 Output voltage with filter

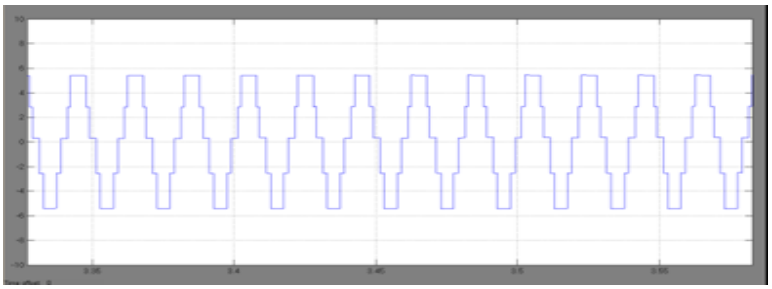

Fig.9 Output current without filter

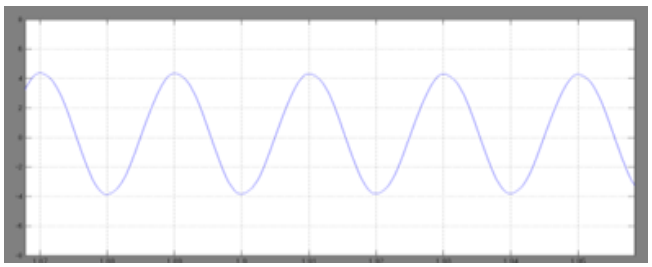

Fig.10 Output current with filter

Fig.7and Fig.8 shows the load voltage waveform without filter and its FFT spectrum. Figs.9 &10 show the load current waveform with filter and without filter.THD of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency. THD is calculated for various modulation index values and the comparison is shown in Fig 11.From the figure it is shown that THD is low for the chosen rna of 0.8.Output voltage and other parameters are compared between Z-Source MLI. Compared with the latest sinusoidal PWM technique for cascaded multilevel Z-Source inverter, the proposed unipolar PWM technique does not produce the harmonics of carrier frequencies. The proposed modulation technique reduces the amplitude of significant harmonics and its sidebands for all modulation indexes thus making filtering easier, and with its size being significantly smaller.

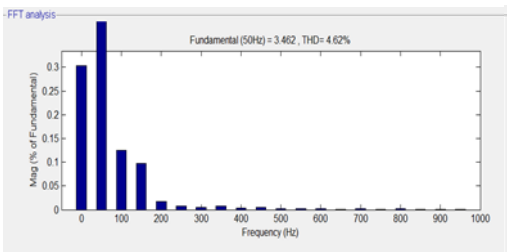

Fig.11THD value of unipolar ISPWM

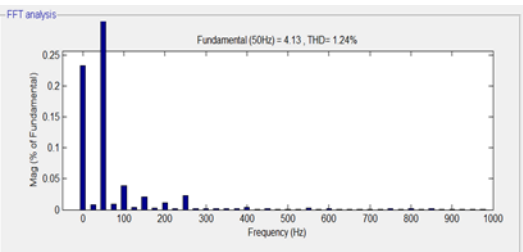

Fig.12 THD value of unipolar CDPWM

MEASURED QUANTITIES	UNIPOLAR ISCPWM	UNIPOLAR CDPWM	SVM
Input voltage	400V	400V	400V
Output voltage	450V	540 V	465V
THD	4.62%	1.24%	15.1%

TABLE 2COMPARISON

VIII. HARDWARE DETAILS

Power Circuit

230V, 50Hz ac supply is step down to 15V ac using a step down transformer. It is then converted to dc using a bridge rectifier. Capacitors placed immediately after the bridge rectifier filters the ripples in the rectified dc output and it linearly discharges during any power supply interruption. Output of the capacitor is fed to the L7805A voltage regulator that regulates the dc voltage value at 12V. This voltage is also fed to L7812A voltage regulator to obtain a 5V regulated dc. Hence two dc power supplies of 12V and 5V are obtained. The 5V dc output is fed to the control circuit and the 12V dc is fed to main circuit.

Control Circuit

As mentioned above, 5V dc is fed to PIC16F877 microcontroller and is programmed with space vector modulation technique to produce the PWM output. Crystal oscillator is provided in this circuit to give necessary clock input to the microcontroller. A reset switch and a potentiometer are also provided in this circuit.

Main Circuit

The main circuit consists of three parts

- Z-source circuit
- Isolation part
- Cascaded H-bridge

The 12V dc from the power circuit is fed to the z-source network and then the output of z-source network is connected to the cascaded H-Bridge inverter via optocoupler MCT2E.The PWM output of the control circuit is fed to the input terminal of the MCT2E optocoupler and the output is fed to the input of cascaded H-bridges which consist of eight IRF540 MOSFETs. The output of cascaded H-bridge is connected to a resistive load.

Fig 13 Hardware Unit

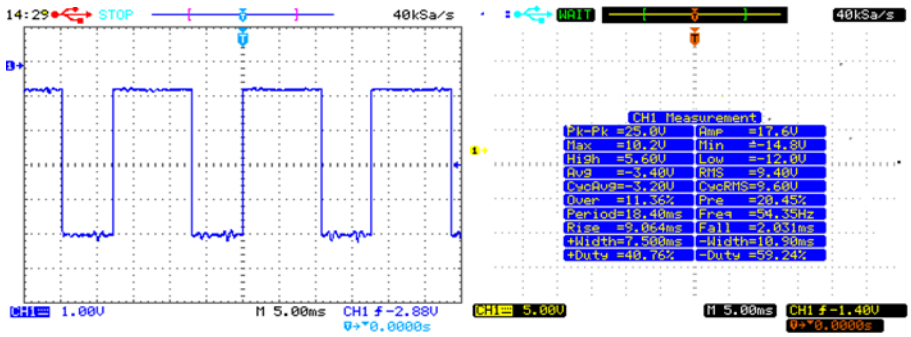

Fig 14 PWM output

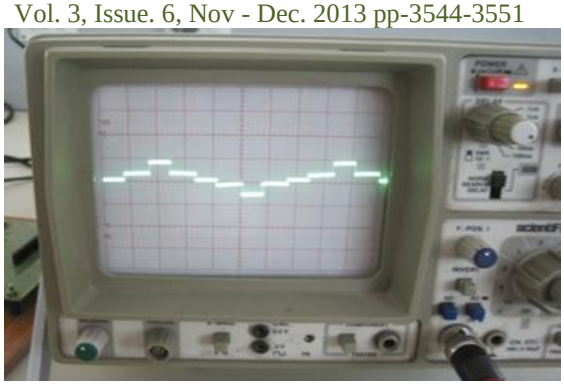

Fig 15 Fivel level output

IX. CONCLUSION

This paper has investigated a Z-source cascaded multilevel inverter. Z-Source cascaded multilevel inverter gives higher output voltage through its Z network. Unipolar PWM techniques have been employed for Z-MLI. The performance of the proposed Z-MLI has been compared. From the results, it is found that Z-MLI with unipolar PWM provides a higher RMS value of the output voltage, higher voltage gain, reduced voltage stress and avoids the intermediate boost DC-DC converter. Topology and modulation-method is selected based upon the application They are selected depending on their unique features and limitations like power or voltage level, dynamic performance, reliability, costs, and other technical specifications

ACKNOWLEDGEMENT

The author wish to thank the management of PSNA institution for providing the computational facilities to carry out this work.

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