International Journal of Modern Engineering Research (IJMER)
www.ijmer.com Vol. 3, Issue. 6, Nov - Dec. 2013 pp-3632-3640 ISSN: 2249-6645

Variable Threshold MOS Circuits

Dr. Ragini K.[1], Dr. Satyam M.[2], Dr. Jinaga B. C.[3]
[1]*G. Narayanamma Institute of Technology & Science,*
Department of Electronics and Communication Engineering, Hyderabad, India
[2]*International Institute of Information Technology, Hyderabad, India*
[3]*Jawaharlal Nehru Technology University, Hyderabad, India*

ABSTRACT: *Dynamic threshold MOS (DTMOS) circuits provide low leakage and high current drive , compared to CMOS circuits, operated at low voltages. This paper proposes a modified DTMOS approach, called Variable threshold MOS (VTMOS) approach. The VTMOS is based on operating the MOS devices with an appropriate substrate bias which varies with gate voltage, by connecting a positive bias voltage between gate and substrate for NMOS and negative bias voltage between gate and substrate for PMOS. With VTMOS, there is a considerable reduction in operating current and power dissipation, while the remaining characteristics are almost the same as those of DTMOS. Results of our investigations show that VTMOS circuits improves the power up to 50% when compared to CMOS and DTMOS circuits, in sub threshold-region. The performance characteristics of VTMOS circuits - The Power dissipation, Propagation delay and Power delay product with the substrate bias have been evaluated through simulation using H spice. The dependency of these parameters on frequency of operation has also been investigated.*

Keywords: *Sub- threshold, Dynamic threshold MOS Inverter, Propagation delay, Noise-margin, Variable threshold MOS Inverter, Power dissipation.*

I. INTRODUCTION

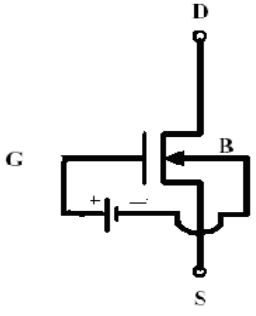
Over the past twenty years , semi conductor industry emerged considerably and demand for VLSI has grown all over the world. During the recent years . there is a great demand for portable devices like cellular phone , palm top computers, GPRS receivers, pocket calculator, and pacemakers, they all demand for low power. Hence low power design has emerged as a very attractive and fast development field. The limited battery life time demands for the reduction of power consumption of portable devices. High performance digital systems such as DSP, microprocessor's, and other applications insists for low power design. Besides this, the environment also demands for low power design. As the electronic equipment usage increases, the power consumption and the cost for excessive cooling system increases.

In view of this it is essential to minimize the power dissipation. The various techniques that are employed to reduce the power dissipation are recycling the energy that might be stored in nodal capacitances, reduction in transitions (0 to 1 or 1 to 0), reduction in voltages and currents , and so on. The techniques based on operation at very low currents usually below the normal conduction region, especially in FET based circuits is known as sub threshold operation. This has attracted several investigators, as it has flexibility to choose their own logic levels and power dissipation. This paper is only an attempt to modify the normal sub threshold operating condition to reduce the power dissipation without affecting the performance. The modified operation that is suggested is based on biasing the substrate of FET dynamically in tune with the gate voltage. This we termed as variable threshold MOS operation. It has been shown that VTMOS operation can result in power saving of up to 50% compared to CMOS operation and can be used in cascadable circuits like CMOS circuits.

1.1 Current voltage characteristics of NMOS and PMOS Transistors under VTMOS operating conditions in sub-threshold region:

To evaluate the behavior of NMOS and PMOS devices under VTMOS operating conditions, the current voltage characteristics are measured and plotted using H spice simulation tool. The transistor's are chosen from 65nm technology. The threshold voltage for NMOS and PMOS devices are 0.22v and -0.22v respectively. The width of NMOS (Wn) and PMOS (Wp) is chosen as 200nm and 400nm respectively. The supply voltage is taken as 0.2v which is below the threshold of both the devices.

1.1.1 Current voltage characteristics of NMOS devices under VTMOS operating conditions:



(a) n-MOSFET

Figure 1

As shown in Figure (1),the NMOS transistor is connected to gate through $V_{AN,}$ which bias the substrate negative with respect to gate. For different values of V_{AN} starting from 0 to 0.2v, the current voltage characteristics of NMOS, i.e Id verses Vgs are plotted and given in Figure(2).

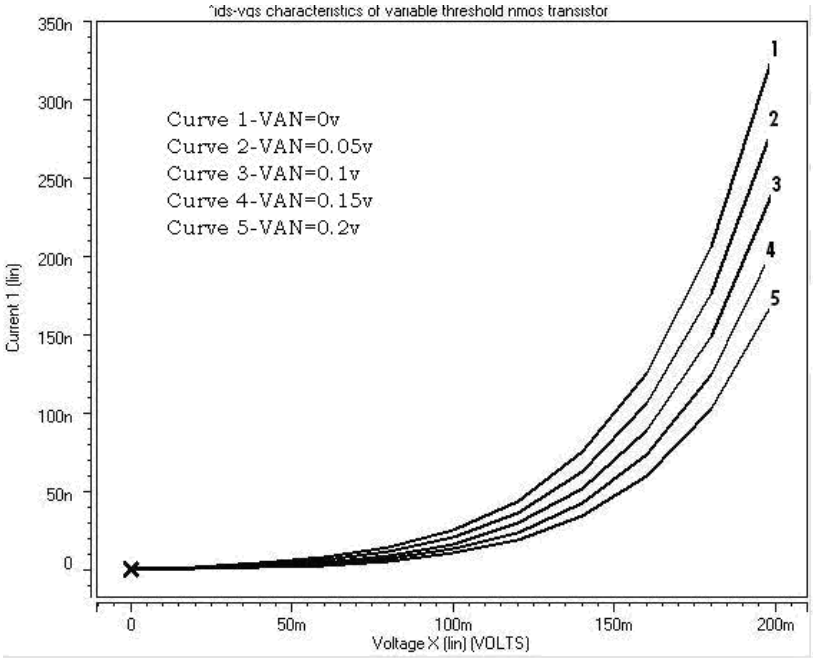


Figure: 2 Ids-Vgs curves of Variable Threshold NMOS Transistor (V_{AN} varying from 0(top)to 0.2v(bottom))

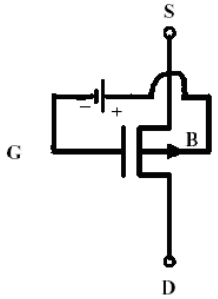
When V_{AN} is varied from 0 to 0.2v, the transistor substrate bias is dynamically adjusted, depending on the gate voltage, causing the threshold voltage of the device to adjust dynamically. The variation in threshold voltage causes variation in leakage currents and power dissipation.

The VTNMOS transistor is operated in two modes i.e ON mode and OFF mode .As the entire operation is limited to sub threshold region , for a given V_{AN} , the 'ON' condition is defined for NMOS transistor when Vgs=0.2v.Similarly for a given V_{AN} , ' OFF' condition is defined for NMOS transistor when Vgs = 0v. In the 'ON' mode, when V_{AN}=0.2v and Vgs=0.2v,then the substrate bias of NMOSFET transistor is switched to 0v. In this condition, the VTNMOS transistor is similar to NMOS ON transistor operation. Hence the drain current of VTNMOS is same as NMOS transistor under normal conditions and is found to be 171nA.

For the condition, that VAN=0v and Vgs=0.2v (DTNMOS condition),the source and substrate of MOSFET is forward biased, which implies that the effective threshold voltage of the device is reduced. hence one expects much higher current than the current that flows under normal NMOS operation (Vgs=0.2v).This current has been found to be 334nA from the Figure (2).

The OFF condition of the transistor in this article is defined as the condition in which Vgs = 0 and V_{AN} is varied from 0 to 0.2v.when Vgs=0v and V_{AN}=0V,the condition corresponds to normal NMOS transistor .when V_{AN}=0.2v,the substrate is biased negative w.r.t source by -0.2v and hence ,the threshold voltage increases and the current decreases further .From the Figure(2),the value of current for Vgs=V_{AN}=0 is measured as 1.4nA and for Vgs=0v and V_{AN}=0.2v it is 550pA, which is about one-third of the leakage current ,when the substrate is biased at 0v.

1.1.2 The current voltage characteristics of PMOS under VTMOS operating conditions:



(b) p-MOSFET

Figure 3

The PMOS device under VTMOS operating condition is shown in Figure (3).It may be seen that the substrate is positively biased w.r.t gate.

Figure 4(a) shows the Ids verses Vgs curves of PMOS device under VTMOS operating conditions, for different values of $V_{AP,}$ starting from 0 to -0.2v. The Vds is considered as -0.2v and Vgs is varied from 0 to -0.2v.

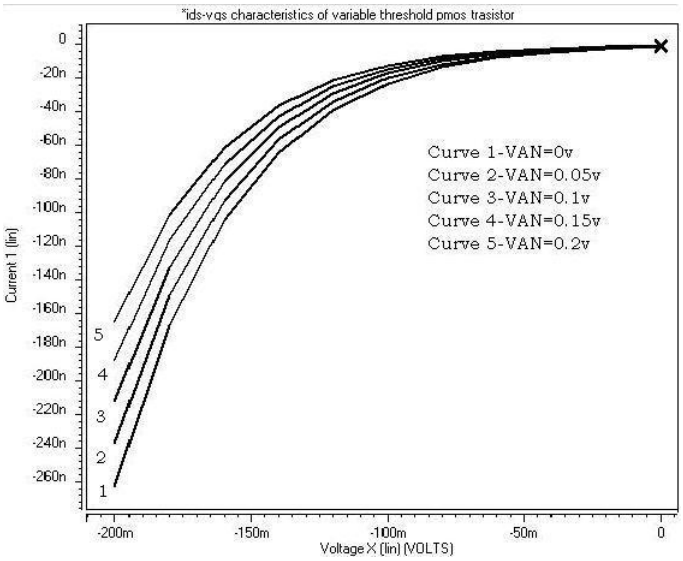


Figure: 4 (a) Ids-Vgs curves of Variable Threshold PMOS Transistor (V_{AP} varying from 0(bottom)to 0.2v(top))

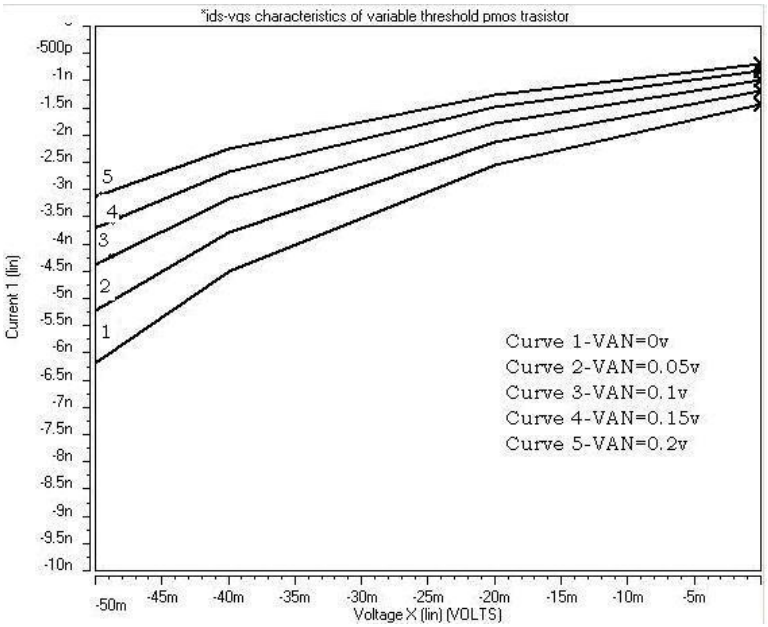


Figure: 4(b) Ids-Vgs curves of Variable Threshold PMOS Transistor (V_{AP} varying from 0(bottom)to 0.2v(top))-zoomed version to Measure Ioff current

For different values of V_{AP} starting from 0 to -0.2v, the current voltage characteristics of PMOS is plotted.

When V_{AP} is varied from 0 to -0.2v, the PMOS transistor's threshold voltage is varied dynamically as in the case of NMOS device .The ON and OFF conditions for PMOS device are similar to that of NMOS device. Considering the ON condition of VTPMOS transistor, for V_{AP}=0v and Vgs=-0.2v (DTPMOS condition) it is observed that there is highest drain current of Ion=-262nA .When V_{AP}=-0.2v and Vgs=-0.2v,lowest Ion drain current Ion=-164nA is recorded for VTPMOS and is observed from Figure 4(a).

Considering the PMOS off condition, it is observed from the Figure 4(b), that for V_{AP} = 0 v , the Ioff current is 1.4nA and for V_{AP} = 0.2v, the Ioff current is less and is measured as 695pA. thus the current levels (Ion & Ioff) get reduced with increase in bias voltage when VTPMOS substrate is positively biased with respect to gate.

II. VTMOS SEQUENTIAL CIRCUITS

Sequential circuits are those in which the output depends on the present inputs and previously applied inputs. As mentioned earlier this sequential circuits are generally realized by making use of combinational circuits with appropriate positive feedback. VTMOS based sequential circuits are realized using VTMOS combinational circuits. The transistor's for

sequential circuits are chosen from 65nm technology. The width of PMOSFETS and NMOSFETS are chosen as 400nm and 200nm respectively. The supply voltage is taken as 0.2v which is below the threshold of the devices.

For different values of V_{AN} starting from 0 to 0.2v and corresponding V_{AP} of same magnitude from 0 to -0.2v, the performance parameters of VTMOS sequential circuits– average power dissipation, propagation delays, rise and fall time delay, power-delay –product and frequency response have been obtained through simulation .The VTMOS JK master slave flip flop is designed and performance analysis is done in the following sections . The performance results of the VTMOS JK master slave flip flop are compared with the CMOS JK master slave flip flop circuits.

2.1 VTMOS JK master slave flip flop:

The VTMOS JK master slave can be constructed with a pair of JK flip flops using VTMOS NAND gates. The circuit diagram, Truth table and operation of the circuit is given in Figure 5 and Table (1)below. The first flip flop serves as master and second flip-flop serves as slave. There is a feedback connection from the output of second to the input of first. The master is enabled for clock=1 and slave is enable for clock = 0.

Circuit Diagram:

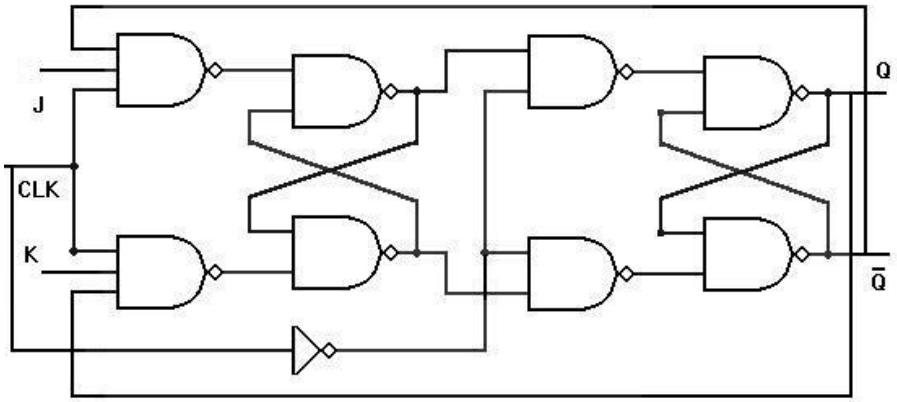


Figure 5

Truth table:

Inputs			Outputs	
Clock	**J**	**K**	**Q**	$\overline{Q}$
×	×	×	0	1
↑	0	0	No change	
↑	0	1	0	1
↑	1	0	1	0
↑	1	1	Toggle	

Table 1

When clock = 1, the master is enabled, and output of master responds to the input J and K according to the truth table. When clock = 0, the master is disabled and slave is enabled. The state of master output is now transferred to slave output. the master slave flip flop functions properly only when the clock width is larger than the propagation delay time through the master flip flop. The performance of this latch in terms of power dissipation , logic levels ,propagation delay ,rise and fall time delays ,frequency response have been analyzed and described below.

2.2 Input output wave forms for VTMOS JK master slave flip flop circuit:

Function of the VTMOS JK master slave flip flop circuit has been compared with conventional JK master slave flip flop circuit and verified with inputs taken in the form of pulses varying from 0 to 0.2v, with a rise and fall time of 25ns. As in the case of combinational circuits, the supply voltage is 0.2v and load capacitance is 10fF. The input pattern chosen for analysis of performance parameters is J=111001101 and K=010110010 and clock=0101010101 at a sample time of 10 microseconds (100kHz) frequency. The output wave forms are plotted for all Flip-flops where v (3),v(4) represents the output corresponding to Master flip-flop and v(8),v(9)represents Slave output.. From the figures 6(a), 6(b) and 6(c), it may be seen that the output logic levels are almost the same as input logic levels and the output is as for expected for the given input .Thus the VTMOS JK master slave flip flop circuit is found to be working properly as that of conventional CMOS JK master slave flip flop circuit.

Circuits (VTMOS JK master slave flip flop for $V_{AN}=V_{AP}=0v$, VTMOS JK master slave flip flop for $V_{AN}=V_{AP}=0.2v$, and CMOS JK master slave flip flop.) for a period of 200 microseconds is shown in Figure 6(a), Figure 6(b) and Figure 6(c).

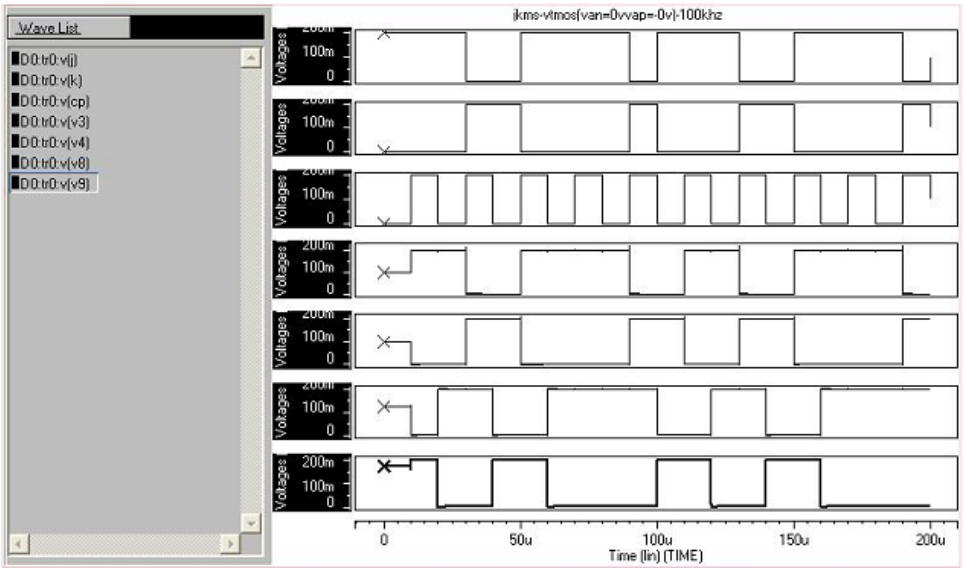


Figure 6(a): INPUT-OUTPUT WAVEFORMS OF VTMOS JKMS Flip flop(V_{AN}=0V,V_{AP}=0V) -100KHZ

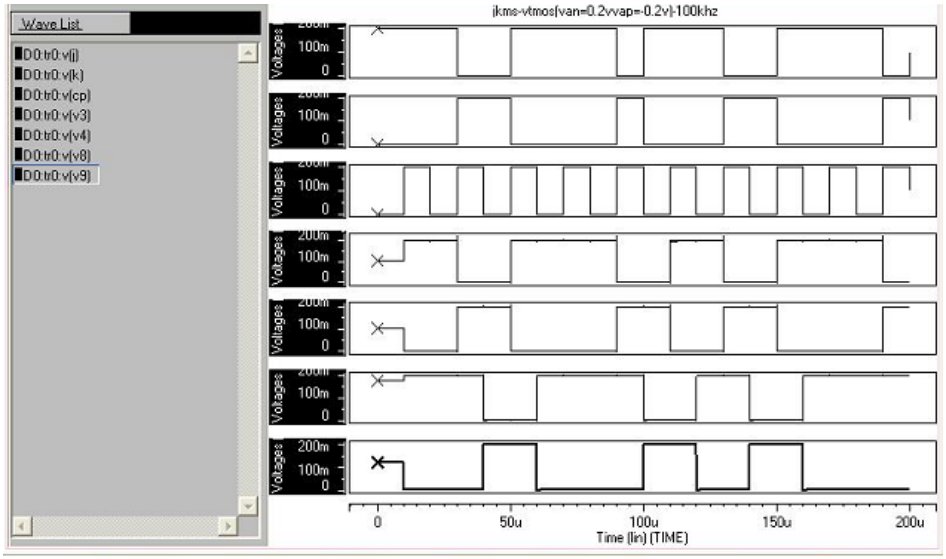


Figure 6(b): INPUT-OUTPUT WAVEFORMS OF VTMOS) JKMS Flip flop(V_{AN}=0.2V,V_{AP}=0.2V -100KHZ

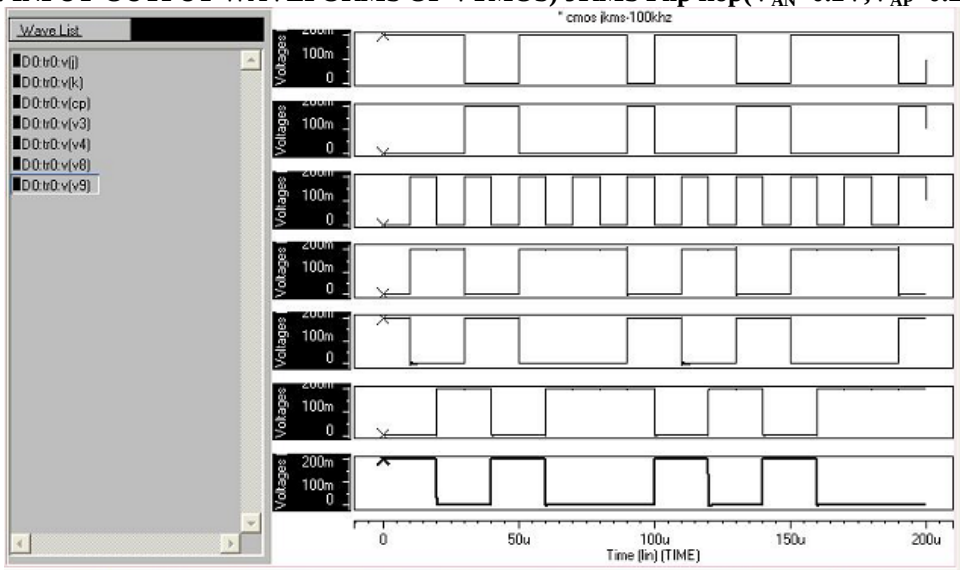


Figure 6(c): INPUT-OUTPUT WAVEFORMS OF CMOS JKMS Flip flop-100KHZ

From the figures 6(a), 6(b) and 6(c), it may be seen that the output logic levels are almost the same as input logic levels and the output is as for expected for the given input .Thus the VTMOS JK master slave flip flop circuit is found to be working properly as that of conventional CMOS clocked SR latch circuit.

The performance of VTMOS JK master slave flip flop circuit with $|V_{AN|}=|V_{AP}|$ varying from 0 to 0.2V is compared with CMOS JK master slave flip flop. The performance analysis is done in following section and result discussion is made in the next section. At last the frequency analysis is done.

III. PERFORMANCE ANALYSIS OF VTMOS JK MASTER SLAVE FLIP FLOP CIRCUIT

The propagation delay, the rise and fall time delay, average power dissipation and power delay product are measured for VTMOS JK master slave flip flop circuit (for $|V_{AN|}=|V_{AP}|$ varying from 0 to 0.2v) at a particular input signal frequency of 100 kHz for performance evaluation .The performance results of VTMOS JK master slave flip flop are also compared with the conventional CMOS JK master slave flip flop in this section.

The variation of performance parameters (propagation delay, average power dissipation and power delay product) for different JK master slave flip flop circuits (Sub threshold VTMOS JK master slave flip flop circuit with $|V_{AN|}=|V_{AP}|$ varying from 0 to 0.2v and CMOS JK master slave flip flop Circuit), are tabulated in Table 2(a) for a frequency of 100 khz, and at supply voltage of 0.2v. The input pattern is repeated for a period of 5000 microseconds . The variation of rise and fall time delays of all JK master slave flip flop circuits is shown in Table 2(b).Along with this, the variation of propagation delay, power dissipation and power delay product for $|V_{AN|}=|V_{AP}|$ varying from 0 to 0.2 v at 100 khz. is also shown in the Figure. 7(a), 7(b), 7(c)

The discussion on the performance analysis is done in the next following section.

S.no	Circuit	T_{PLH} (seconds)	T_{PHL} (seconds)	T_P (seconds)	Average power dissipation (watts)	Power delay product (joules)
1	VTOMS (0V)	4.058E-08	2.280E-08	3.169E-08	4.287E-10	1.358E-18
2	VTMOS(0.05V)	4.607E-08	2.533E-08	3.570E-08	2.566E-10	0.916E-18
3	VTMOS(0.1V)	5.062E-08	2.739E-08	3.901E-08	2.133E-10	0.832E-18
4	VTMOS(0.15V)	5.811E-08	3.238E-08	4.524E-08	1.729E-10	0.782E-18
5	VTMOS(0.2V)	6.724E-08	3.575E-08	5.149E-08	1.464E-10	0.754E-18
6	CMOS	5.177E-08	2.702E-08	3.940E-08	3.121E-10	1.229E-18

Table 2(a) – Variation of propagation delay, power dissipation and power delay product for different JKMS Flip flop circuits

S.no	Circuit	Rise time delay (seconds)	Fall time delay (seconds)
1	VTMOS(0V)	1.167E-08	9.287E-08
2	VTMOS(0.05V)	1.784E-08	2.993E-08
3	VTOMS(0.1V)	2.208E-08	3.105E-08
4	VTMOS(0.15V)	2.418E-08	3.453E-08
5	VTMOS(0.2V)	2.837E-08	5.451E-08
6	CMOS	2.529E-08	4.098E-08

Table 2(b) -Variation of rise and fall time delay for different JKMS Flip flop circuits

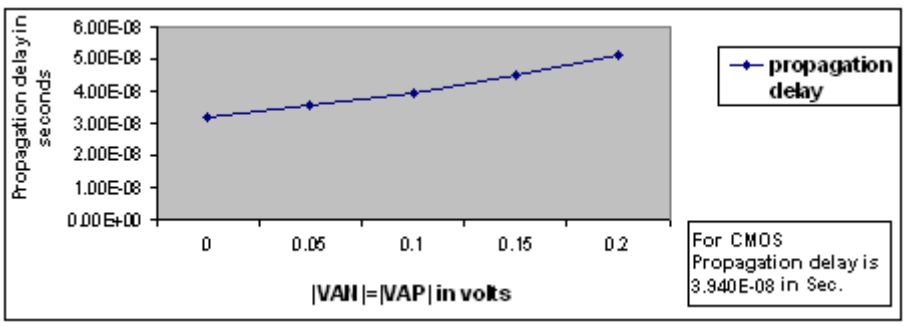


Figure 7(a): Variation of propagation delay for VTMOS JK master slave Flip flop ($|V_{AN|}=|V_{AP}|$ varying from 0 to 0.2v)

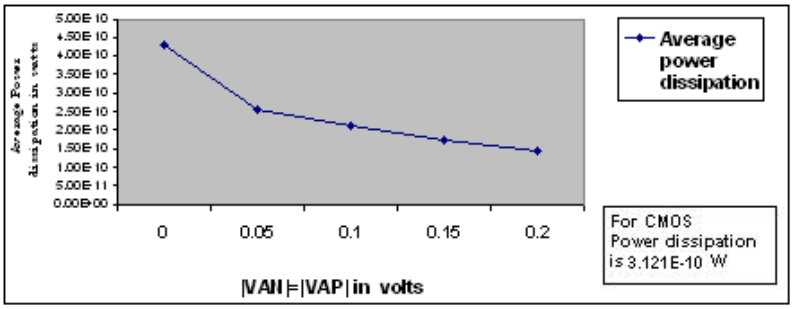


Figure 7(b): Variation of Power dissipation for VTMOS JK master slave Flip flop ($|V_{AN}|=|V_{AP}|$ v arying from 0 to 0.2v)

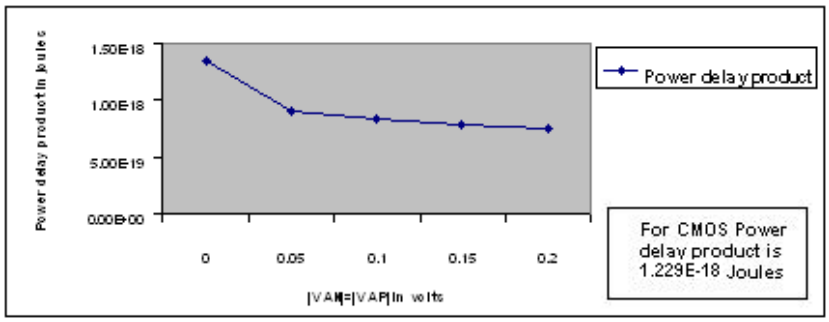


Figure 7(c) : Variation of Power delay product for VTMOS JK master slave Flip flop($|V_{AN}|=|V_{AP}|$ varying from 0 to 0.2v)

3.1 Result Discussion:

Results are obtained from HSPICE simulations using 65nm technology . The variation of propagation delay of VTMOS JKMS Flip flop with $|V_{AN}|=|V_{AP}|$ varying from 0 to 0.2v is plotted in figure 7(a). It is observed that propagation delay of VTMOS JKMS Flip flop, increases with increase in $|V_{AN}|=|V_{AP}|$. The propagation delay is lowest for VTMOS JKMS Flip flop with $|V_{AN}|=|V_{AP}|$=0v and the propagation delay of VTMOS JKMS Flip flop with $|V_{AN}|=|V_{AP}|$=0.2v, almost approaches the CMOS JKMS Flip flop circuit.

Figure 7(b) gives the variation of power dissipation of VTMOS JKMS Flip flop with $|V_{AN}|=|V_{AP}|$ varying from 0 to 0.2v. It is observed that power dissipation is highest for VTMOS JKMS Flip flop at $|V_{AN}|=|V_{AP}|$=0V. Over all 53% reduction in power dissipation is observed for VTMOS JKMS Flip flop at $|V_{AN}|=|V_{AP}|$=0.2v when compared to CMOS JK master slave flip flop.

The variation of power delay product of VTMOS JKMS Flip flop with increase in $|V_{AN}|=|V_{AP}|$ is observed in Figure 7(c). The power delay product also reduces with increase in $|V_{AN}|=|V_{AP}|$ which is invited feature of VTMOS JK master flip flop.

3.2 Effect of frequency:

The effect of frequency on performance characteristics is noted by varying the frequency from 100 khz to 8 Mhz. The input and output wave forms of VTMOS JK master slave flip flop at $|V_{AN}|=|V_{AP}|$=0v, VTMOS JK master slave flip flop at $|V_{AN}|=|V_{AP}|$0=0.2v and CMOS JK master slave flip flop are given in Figure 8(a), 8(b) and 8(c) for 2 MHZ(sample time of 500 microseconds) frequency for the same input pattern of J=111001101 and K=010110010 and clock=0101010101.

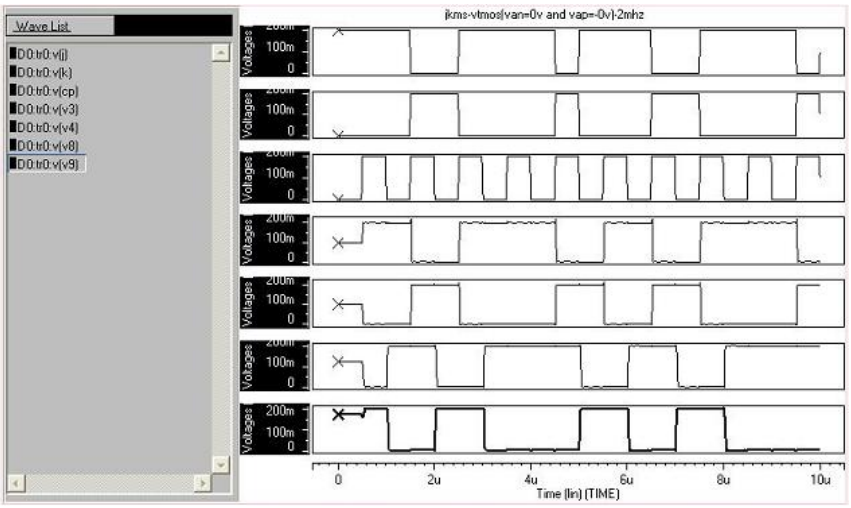


Figure 8(a): INPUT-OUTPUT WAVEFORMS OF VTMOS JKMS Flip flop($V_{AN}=V_{AP}$=0V) -2MHZ

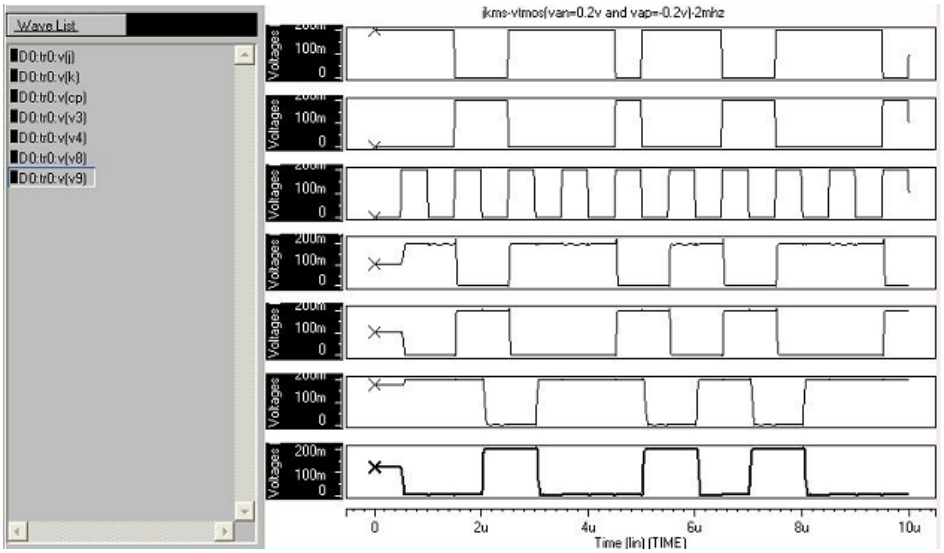


Figure 8(b): INPUT-OUTPUT WAVEFORMS OF VTMOS JKMS Flip flop(V_{AN}=V_{AP}=0.2V) -2MHZ

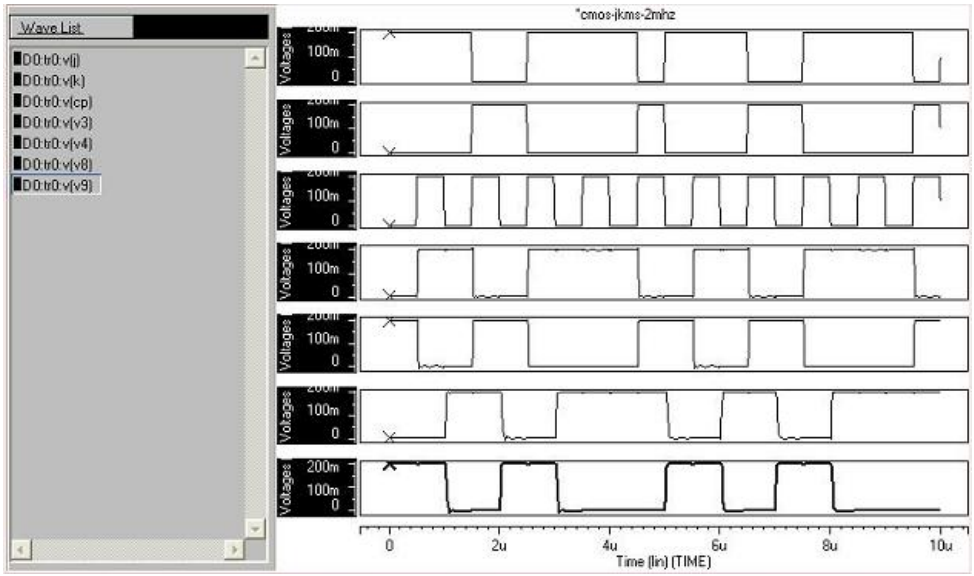


FIGURE 8(c): INPUT-OUTPUT WAVEFORMS OF CMOS JKMS -2MHZ

From the figures it may be seen that the output waveforms resembles the input waveforms at 2Mhz frequency .Hence it can be said that VTMOS JK Master slave circuit is working properly at higher frequencies. With increase in frequency the general trend of variation of power dissipation and propagation delay are maintained as those reported at 100Khz. The variation of power dissipation with frequency for sub threshold VTMOS JK Master slave circuit (0 TO 0.2V) and sub threshold CMOS JK Master slave circuit is shown in Figure 9.It is observed that average power dissipation increases with frequency, but propagation delay and power delay product remains almost constant with frequency. As in the case of VTMOS combinational circuits the power dissipation of VTMOS JK master slave flip flop increases much more faster than in the case of CMOS JK master slave flip flop as frequency is increased. The reasons for this rapid increase in power dissipation in the case of VTMOS JK master slave flip flop are similar to that explained for VTMOS inverter circuits.

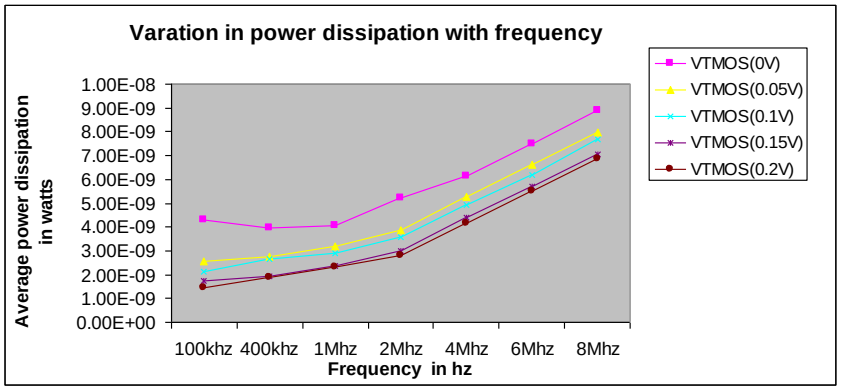


Figure 9: variation of average power dissipation with frequency for JK master slave

IV. CONCLUSIONS

This paper reports a modified DTMOS approach which is called VTMOS approach. In these circuits the substrate is operated with a fixed bias (V_{AN} /V_{AP}) which results in further reduction in the operating currents compared to DTMOS circuits. The Proposed scheme shows improved power efficiency compared to CMOS and DTMOS circuits , up to a frequency of 8 M h z (for the specific devices used in this Investigation).

Using these concepts one may be able to build low power digital circuits like [19, 20] which consume lower power than the conventional CMOS and DTMOS circuits.

REFERENCES

[1] H.Soeleman , K.Roy, and B.C.Paul. : "Robust Sub threshold Logic for Ultra Low Power Operation" ,IEEE trans VLSI system, Feb 2001,Vol. 9, PP. 90-99.

[2] Jabulani: Nyathi and Brent Bero: "Logic Circuits Operating in Sub Threshold Voltages" , ISLPED 06, October 4-6, 2006, Tegernsee, Germany.

[3] C.Hyung, - 11 Kim, H.Soeleman, and K.Roy: "Ultra-Low Power DLMS Adaptive Filter for Hearing Aid Applications" ,IEEE transactions on very large scale integration (VLS1) system, vol. 11, No.6, December, 2003. PP 1058-1067.

[4] H. Soeleman and K. Roy,"Ultra-low power digital subthreshold logiccircuits", in Int. Symp. Low Power Electron. Design, 1999, pp. 94–96.

[5] Fariborz Assaderaghi, Stephen Parke, Dennis Simitsky, Jeffrey Bokor, Ping K. KO. Chenming Hu:"A Dynamic Threshold Voltage MOSFET (DTMOS) for Very Low Voltage Opertaion" ,IEEE Electron device letters, vol. 13, No.12, December 1994.

[6] Tae-Hyoung Kim, Hanyang Eom, John. Keane and Chris Kim: "Utilizing Reverse Short Channel Effect for Optimal Sub Threshold Circuit Design" ,ISLPED 06, October 4-6, 2006. Tegern see, Germany.

[7] H. Soeleman, K. Roy, B. Paul :"Robust ultra-low power sub-threshold DTMOS logic", in Int. Symp. Low Power Electron. Design, 2000 ,pp.25 – 30.

[8] J. Gil, M. Je, J. Lee and H. Shin:"A High Speed and Low Power SOI Inverter using Active Body-Bias", in Int. Symp. Low Power Electron.Design , 1998 , pp.59-63.

[9] F. Assaderaghi, D. Sinitsky, S. Parke, J. Bokor, P. K. Ko, and C. Hu: "A dynamic threshold voltage MOSFET (DTMOS) for ultra-low voltage operation", in IEDM Tech. Dig., 1994, pp. 809–812.

[10] I.Chung, Y.Park, and H. Min: "A new SOI inverter for low power applications", in Proc. 1996 IEEE Int. SOI Conf., 1996, pp. 20–21.

[11] A.Drake, K. Nowka, R. Brown: " Evaluation of Dynamic-Threshold Logic for Low-Power VLSI Design in 0.13um PD-SOI" ,VLSI-SOC 2003,pp. 263-266.

[12] M.R. Casu, G**.** Masera, *G.* Piccinini, M. Ruo Roch, M. Zamboni:"Comparative Analysis of PD-SOI Active Body-Biasing Circuits," *Proc. IEEE International SOI Conference*, pp. 94-95, Oct. 2000.

[13] S.Soleimani,A.Sammak,B.Forouzandeh "A Novel Ultra-Low-Energy Bulk Dynamic Threshold Inverter Scheme",Proceedings of the International Multi Conference Of Engineers and Computer Scientists 2009 Vol 1 IMECS 2009,March 18-20,2009,Hong Kong

[14] Assaderaghi et al,F.: "Dynamic Threshold - Voltage Mosfet (DTMOS) for Ultra - Low Voltage VLSI" ,IEEE trans Electron Devices, Vol. 44, PP 414-422, Mar 1997.

[15] T.Kobayashi, and T.Sakurai : "Self-adjusting Threshold Voltage Scheme (SATS) for Low-Voltage High - Speed Operation", in Custom Integrated Circuits Conf., May 1994, pp.271-274.

[16] J.M Rabaey: "Digital Integrated circuits: A Design Perspective 1st ed Upper Saddle River" New Jersey: Prentice Hall, 1996.

[17] H.Soeleman., K.Roy.:"Digital CMOS Logic Operation in the Sub-threshold Region," in Tenth Great Lakes Symp.VLSI,Mar.2000,pp.107-112.

[18] Wet Jin and Philip Chan,CH.: "A Comparative Study of S01 Inverter Circuits for Low Voltage and Low Power Applications" , Proceedings 1997 IEEE International SOI conference, Oct. 1997.

[19] Jaydeep P.Kulkarni,Keejong Kim,and Kaushik Roy.:"A 160 mV Robust Schmitt Trigger Based Subthreshold SRAM",IEEE Journal Of Solid-State Circuits,VOL 42,NO.10,Oct 2007.

[20] V.Moalemi,Afjali A.Koosha:"Subthreshold 1-Bit Full Adder Cells in sub-100nm Technologies",Proc.of the IEEE Computer Society Annual Symposium on VLSI,pp.514-515,2007.

BIO-DATA OF AUTHORS

Dr.K.RAGINI-Received B.Tech degree from Sri Venkateswara University,Tirupathi in 1990 and M.Tech and Ph.D degree in Electronics and Communication Engineering from JNTU,Hyderabad in 2000 and 2013 respectively.Worked as Assistant Professor in ECE Department at Chaitanya Bharathi Institute of Technology and Science,Gandipet,Hyderabad from 2000-2005.Then joined as Associate Professor in ECE Department at G.Narayanamma Institute of Technology and Science and presently working in the same institute. She is guiding number of M.Tech students and recently guiding Ph.D Students. she has 10 publications to her credit.

DR.M.SATYAM-Received B.E.(Electronics) from Madras University in 1958.Obtained M.E. and Ph.D from Indian Institute of Sciences in 1960 and 1963 respectively.He worked in various capacities at IISc,Bangalore till his retirement.Presntly he is working as visiting professor,IIIT,Hyderabad.He guided 33 Ph.D students and 11 M.S. students.He has 139 publications in various National and International Journals.He has 10 patents to his credit.He is actively engaged in Research and Teaching.

DR.B.C.JINAGA- Born on June, 1950, graduation from Karnataka University, Dharwad, Post Graduation from Regional Engineering, Warangal and Ph.D. from Indian Institute of Technology, Delhi. He has been with JNT University since 21 years. Prof.B.C. Jinaga was occupied various key positions at JNT University and presently Rector at JNT University. He guided several students for Ph.D. He has published quit number of papers in reputed international and National journals. His research interest includes signal Processing and Coding Techniques. He received Best Teacher Award for the year 2002 - Awarded by Government of Andhra Pradesh.