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A Review on Thermal Aware Optimization of Three Dimensional Integrated Circuits (3D ICs)

Sakshi Raghuvanshi[1], Prince Nagar[2], G.K.Singh[3]

[1] *Student,*[2]*Lecturer,*[3]*Associate Professor, Electronics and Communication Engineering, Sharda University, Greater Noida, Uttar Pradesh, India.*

Abstract:*As the technology size has reached upto 14nm, further shrinking creates some major performance issues. Three dimensional integrated circuits (3D ICs) are gaining importance in the present arena on account of their advanced features. While stacking of die on die in 3D ICs also result in serious thermal problems. These thermal issues can be minimised at different physical design stages with the help of various techniques and algorithms. In this paper an overview of the various methods used for thermal optimization is presented including techniques at floorplanning, placement and routing. It also includes the techniques involving the use of TSVs (through-silicon-vias).*

Keywords:*Floorplanning, placement, routing, 3D-ICs, through-silicon-via (TSV).*

I. INTRODUCTION

With the growth of VLSI, continuous shrinking of technology feature size has been the demand of researchers to enhance the performance of the circuits. Also increasing the integration density leads to increased system complexity and more complex physical design. Interconnect delay is also an important issue for highly integrated circuits. Three dimensional integrated circuit (3D IC) in which multiple device layers are vertically stacked and interconnected, has emerged as a solution to alleviate these problems and enhance the performance beyond Moore's law. 3D ICs provide a means to decrease interconnect length thereby increasing speed, can also combine various technology and physical domain in a single product, therefore enhancing the capabilities. But, these benefits are achieved at cost of other factors like testing becomes difficult and complex, as the number of layers stacked increases yield also decreases. One of the major problem associated with 3D ICs is improper heat evacuation. Therefore introduction of TSVs in 3D IC designs provide a promising solution through many benefits like heterogeneous integration, reduction in wirelength and decrease in max temperature.

II. LITERATURE REVIEW

This paper follows the order of physical design stages and is organised as follows. Section 2.1 introduces with the thermal model required by 3D ICs. Section 2.2 discuss the floorplanning algorithm considering the temperature aspects too. Section 2.3 deals with the thermal aware placement in 3D ICs. Thereafter in section 2.4 TSV planning is described. And finally thermal dependent routing algorithm are discussed.

2.1 Heat Transfer Models

Several thermal analysis need to be performed for the successful application of 3D ICs in products. Development of analytical models for heat spread is required to accurately analyse thermal management of 3D ICs. **Jain Ankur**, **et.al [10]** developed finite-element and analytical models of heat transfer for stacked 3D ICs. Analytical model was developed for temperature distribution in multidie-stack with multiple heat source. This model was used to develop thermal resistance and thermal sensitivity matrices for 3D ICs which is the extension of the single-valued junction-to-air thermal resistance concept in an IC. Thermal performance of interdie bonding layer is obtained with the help of numerical simulations performed. Also due to the vertical integration of the dies has led to the reduction in die footprint area but at the cost of increased maximum temperature.

There is a great demand to perform thermal analysis involving the structure of BEOL and location of all power sources in the layout. Also the design loop to assess the thermal consequence of design iterations should include the thermal analysis and verify final design before sign-off. **Oprins H., et.al [18]** presented a method to perform a detailed fine grain thermal analysis of stacked die packages inclusive of complete back end of line structure (BEOL), interconnection between dies and complete electrical design layout of all stacked dies. By using 3D numerical techniques calculations are performed and the method allows to import the full electrical design of all dies in stack. Technique is demonstrated on a 2 stacked die structure, for which the effect of TSV on temperature distribution is studied. Experimental results indicated that the maximum error is less than 5% in the temperature peak and less than 10% in tails of temperature profile.

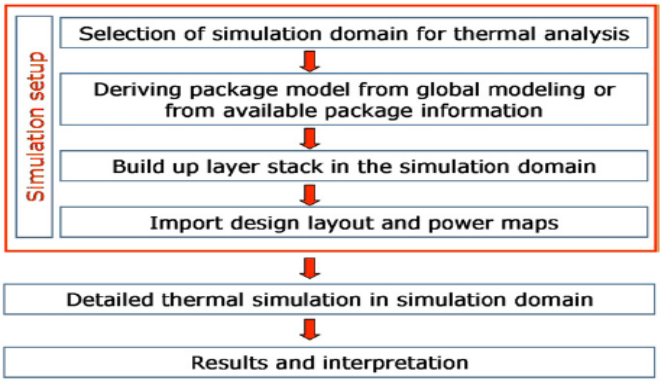

Figure 1. Flow chart for detailed thermal modeling of a stacked die structure [18]

Thermal models have usually assumed equal sized die whereas manufacturing and packaging considerations require different die size for yield and interconnection improvement. **Choobineh Leila, et.al [9]** for predicting the three dimensional temperature presented a heat transfer model for multi-die 3D IC having unequally-sized die. Three dimensional temperature fields for each die are obtained by solving the energy conservation equations with appropriate boundary conditions. Thermal performance of unequally-sized die stacks is compared with a uniformly-sized die stack with the help of this model only. It can be concluded from the experimental results that the rise in peak temperature is greater when the degree of non-uniformity is greater in the die stack.

2.2 Floor planning Algorithms For 3d Ic

Every stage of 3D IC design including the floorplanning process need to consider the thermal issues as a number of challenges are posed by thermal constraint to an efficient 3D floorplanning algorithm. For 2D circuits, floorplanning is a well-studied problem. Several works exist on thermal-driven 2D floorplanning but very few for 3D ICs. **Cong Jason, et.al[15]** proposed a thermal-driven 3D floorplanning algorithm which involved a combined-bucket-and-2D-array (CBA) an efficient 3D floorplan representation. A compact resistive thermal model (CBA-T) was integrated with the 3D floorplanning algorithm to obtain better temperature optimization. Also for faster solution generation a thermal-driven 3D floorplanning algorithm (CBA-T-Fast) based on simplified closed-form thermal model was proposed. And finally a hybrid (CBA-T-Hybrid) of resistive network and closed-form thermal model mentioned earlier was proposed to target a good trade-off between runtime and quality. For CBA-T the maximum on-chip temperature was reduced by 56% with 9X runtime when compared to non-thermal driven floorplan algorithm. Similarly, for CBA-T-Fast the maximum on-chip temperature was reduced by 40% with 2X runtime compared with the non-thermal driven 3D floorplanning algorithm. Lastly for CBA-T-Hybrid maximum on-chip temperature can be reduced by 50% with 3X runtime compared with CBA.

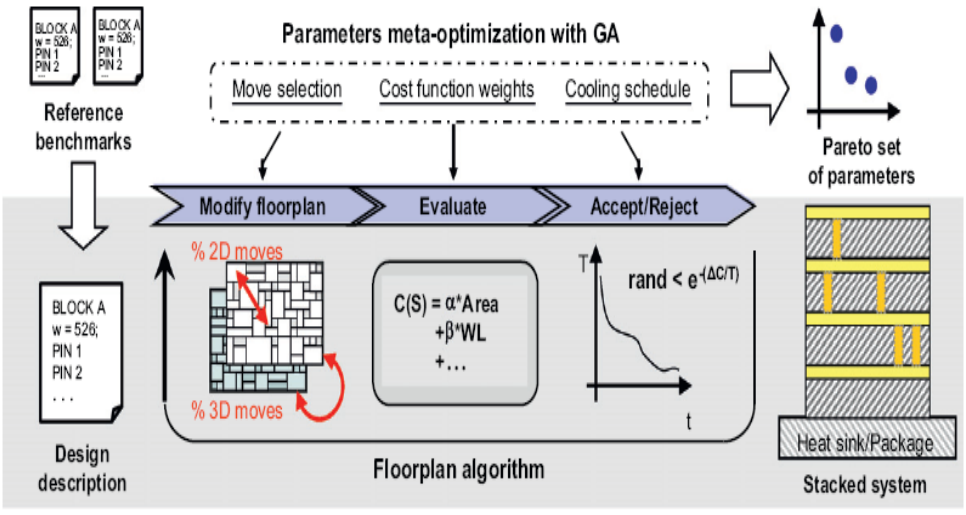

Figure 2. Workflow of floorplan algorithm and meta-optimization [11]

Multiple authors have presented thermal aware floorplanners all of them mainly focusing on minimising weighted sum of area, wirelength and peak temperature. **Frantz Felipe, et.al[11]** discuss the implementation of 3D floorplan algorithm and recognizes 17 parameters that effect its performance. Then they also proposed the use of Genetic algorithm to identify the sets of parameters which provide good floorplan. Two method for reduction of peak temperature and thermal gradients in 3D ICs used are first involving the use of smart heuristic that moves the high power density close to heat sink and other includes the use of a two-phase simulated annealing process involving two different cost function. Results help in concluding that average peak temperature and gradient was reduced by -37% and -56% respectively with an increase of 11% in area and 14% in wirelength when smart heuristic was combined with cost function.

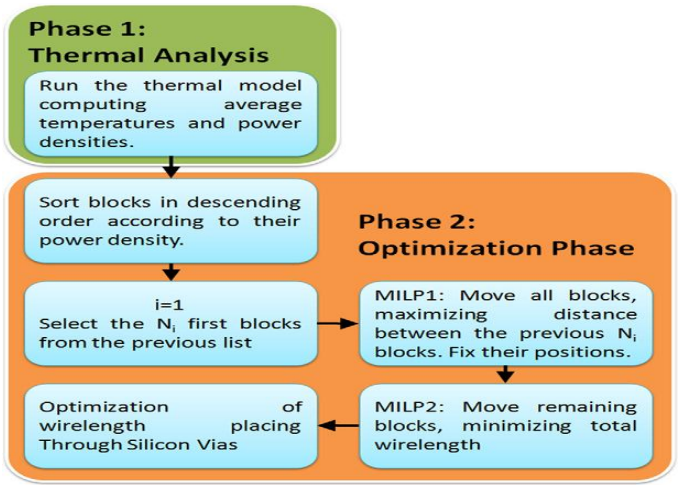

Figure 3. Iterative flow of the approach [12]

As power densities are already an issue in 2D architecture, it increases the thermal problem when moved to 3D architecture. Therefore it is necessary to devise efficient 3D floorplanning which optimize thermal profile of 3D multiprocessor architectures. **Cuesta David, et.al[12]** proposed a set of design rules for the generation of 3D thermal-aware floorplanner for Niagara architecture. The main areas of their work include (1) multi-objective formulation of the floorplanning problem in 3D multi-processor architecture with thermal constraints. (2) By using Mixed Integer Linear Programming (MILP) it performs an efficient resolution of the optimization problem by optimizing the location of functional blocks and through silicon vias. (3) Integration of this MILP model with an accurate thermal model of architecture. Based on the Niagara system experimental results showed an extensive improvement in main thermal and reliability-related metrics (peak and mean temperature, thermal gradients) along with low performance overhead.

The (linear) thermal model must be added to the topological relations when MILP [12] is used for thermal aware floorplanning thereby making the resultant algorithm becomes too complex especially when the problem size increases. **Cuesta David, et.al[13]** proposed thermal-aware floorplanner for 3D many-core single chip a more advanced than the previous one. Through the use of Multi-Objective Evolutionary Algorithm (MOEA) they thermally optimize the 3D layout. They studied the thermal aware problem and formulated the total wire length problem with two different genetic algorithms. Furthermore, this helped in eliminating hotspot, reduce peak and mean temperature and reliability issues associated with temperature. It can be concluded from the experimental results that the maximum-on-chip temperature can be reduced in 80^o in the best case, for two realistic homogeneous and heterogeneous many-core single-chip architecture.

2.3 Thermal Aware Placement Algorithms

Pavlidis Vasilis F., et.al [25] examined the dependence of interconnect delay on the inter-plane via location in 3D-ICs. By optimally placing the inter-plane vias delay of interconnects can be reduced. Via locations which reduce the propagation delay are determined and the inter-plane vias locations are obtained through near-optimal heuristics and geometric programming. For implementing efficient algorithms having lower computational time along with negligible loss of optimality, proposed heuristics are used. Results indicated an improvement in delay for short point-to-point interconnects of 32% with optimally placed inter-plane vias. Also the maximum improvement in delay for optimally placed inter-plane vias is 19% for interconnect trees.

3D placement is an important stage in physical design of 3D ICs which provide the arrangement of a set of functional cells in the multi-stacked layers and offer a way to routing. Many 2D placement algorithms are extended for solving 3D placement problem but as thermal issues are critical therefore need to be solved during

physical design process. **Yan Haixia, et.al [2]** proposed a thermal aware 3D placement algorithm using a quadratic uniformity model which integrates thermal problem with placement process to reduce hotspot temperature and obtained a thermally balanced 3D placement. This algorithm include thermal aware global placement, thermal aware layer assignment and finally a detailed placement. Thermal dissipation and cell distribution are unified through DCT and integrated with wirelength optimization into a quadratic function with the help of quadratic uniformity modelling during global placement stage. This work also proposes two fast methods to estimate the temperature of each grid to update the coefficient instead of precise thermal analysis. Thereafter the distribution of cells through thermal aware layer assignment finishes assignment of cells among the stacked layers with optimum temperature. And finally detailed placement removes the overlaps and optimises the wirelength. Experimental results concluded that this algorithm helped in achieving reduced temperature with little increase in wirelength.

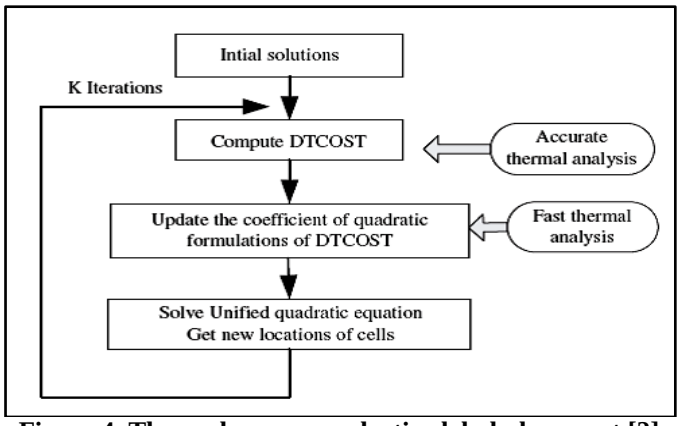

Figure 4. Thermal aware quadratic global placement [2]

In Yan Haixia, et.al [2] the proposed a thermal aware 3D placement algorithm based on quadratic uniformity model but it did not included the through-silicon-vias (TSVs), which are very common in 3D ICs. **Athikulwongse Krit, et.al [1]** have proposed two methods to exploit the die-to-die thermal coupling used force directed temperature aware placement in 3D ICs. First method involves the TSV spread and alignment in which TSVs are arranged only on the basis of TSV density & not on the placement density obtained from both TSV and cell area. Second method is the thermal coupling-aware placement. As based on force directed temperature aware placement, this method introduced two new forces, one that moves cells and other that moves TSVs. The movement is such that higher power cells are placed closed to TSV to heat sink path. These forces balance the power density and thermal conductivity as the area with higher difference has stronger force and weaker force for area with smaller difference.

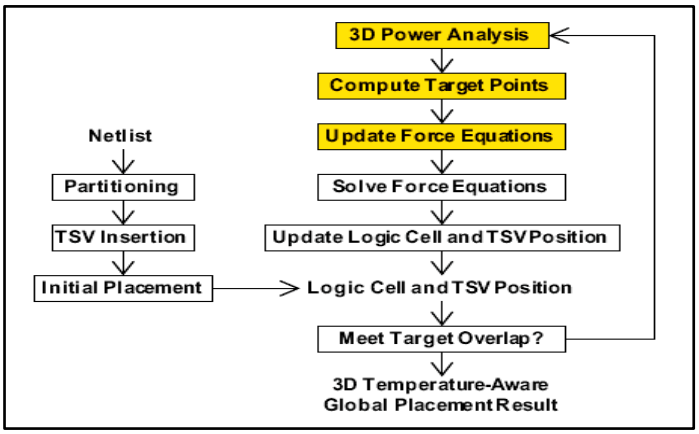

Figure 5. Design flow for 3D IC global placement [1]

For bus planning in 2D layout representations, concept of block alignment is successfully used but neglected for 3D layout. Also blocks are not aligned such that their position fulfil upperand lower distance limits i.e., alignment ranges are not considered. By employing different alignment methods help in structural planning of interconnects of 3D ICs as illustrated in Figure.4. **Knechtel Johann, et.al[6]** demonstrated the effective use of 2D and 3D block alignment of different interconnects for structural planning. They also introduced a 3D

layout representation Corblivar, which is based on the extended corner block list. Extension include encoding of both fixed alignment and alignment ranges along with handling inter and intra-die alignment in a unified manner. Also developed techniques for block alignment and placement. Based on CBL extension and simulated annealing (SA) an open source 3D floorplanning tool was developed. Results concluded Corblivar's applicability for structural planning of interconnects, which is block alignment along with performance competitive with classical 3D floorplanning.

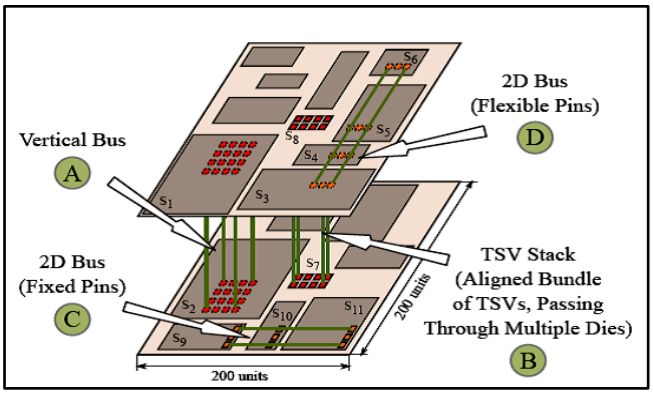

Figure 6. **Interconnect structures in a 3D IC and related block-alignment configurations [6]**

STS-via should be assigned to area which required TS-via for reducing temperature. As TS-via are only inserted into whitespaces, total wirelength of 3D ICs is affected by the STS-via position. Since placing STS-via into hot region result in wire detour leading to increased wirelength, therefore necessitates the STS-via to be integrated with pin assignment. **He Xu, et.al[4]** proposed an approach integrating STS (signal through-the-silicon) via planning with pin assignment. Authors considered STS via planning and pin assignment for two-pin nets connecting one source block to all its sink blocks. This is solved using a min-cost maximum flow based algorithm which provided an optimized solution. Their experimental results made a conclusion that temperature was reduced by 19.3% through their approach when compared to initial temperature and 1.7% when compared to algorithm not considering thermal optimization. Wirelength was also reduced by a factor of 18.9% using their algorithm.

2.4 Algorithms For TSV Planning In 3d IC

Most of the thermal via planning methods have not considered the leakage power but the via number required in the design will be under-estimated if the impact of leakage power on temperature is not taken into account. Higher temperature results to larger delay and leakage power thereby degrading the performance. Similarly increase in leakage power raises temperature resulting in more thermal vias requirement. Leakage-delay-temperature are dependent on each other therefore need to be considered together otherwise may lead to over-estimation or under-estimation for thermal-vias planning. **Wang Kan, et.al[3]** integrated the temperature-leakage-timing dependence into thermal via planning of 3D ICs. They achieved it with the help of three process: (1) Iterative TSV planning considering leakage power-delay-temperature dependence. (2) Performance aware TSV planning with resource constraints. (3) Weighted via planning with power-temperature-timing evaluation. Thus a weighted via insertion approach considers both performance and heat dissipation with resource constraint to obtain best balance among temperature-via number and delay.

Till now majority of work have concentrated on optimization of single performance criterion like power dissipation, delay and signal integrity. Based on multiple performance criterion an inclusive TSV placement and routing methods is needed to make the interconnect timing, performance and system reliability better. **Qian Libo**, **et.al[5]** first of all derived first order expressions for TSV resistance, capacitance and inductance as a function of physical dimension and material characteristics on the basis of parasitic parameter extraction model. They proposed an optimization algorithm concentrating on TSV insertion in 3D ICs with the main aim to minimize the propagation delay considering signal reflection too. Thus, their experimental results showed a 49.96% improvement in average delay and a 62.8% decrease in reflection coefficient when compared to conventional insertion algorithm. Also the effectiveness of optimization for delay increases for higher non-uniform inter-plan interconnect.

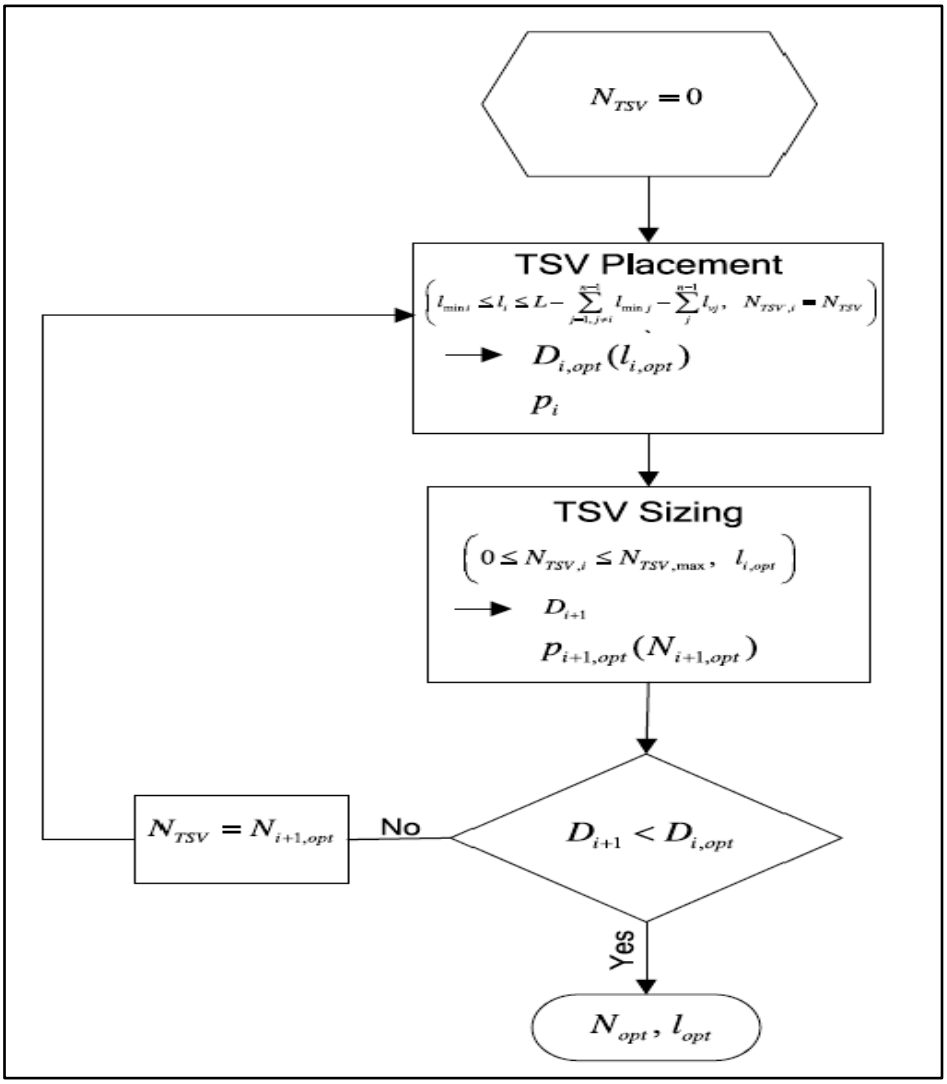

Figure 8. Design flow of interconnect iteration algorithm [5]

Only few works have examined the 3D P/G network design. Few focuses on power supply noise reduction while others concentrated on IR drop in 3D ICs during early stages. Distribution of P/G TSVs is affected by not only the power distribution but also the whitespace distribution around circuit modules as TSVs go through the silicon layer. **Li Zuowei**, **et.al[8]** based on a sensitivity model considering temperature-dependent leakage current this paper presented an efficient thermal aware P/G (power/ground) TSV planning algorithm with topology optimization of P/G grids. More specifically, for supporting P/G TSV planning thermal aware IR drop analysis and a sensitive model for P/G TSV insertion among layers is proposed. Also to optimize P/G network in non-uniform P/G grid topology, shorter wires are used to connect the P/G TSVs to P/G grids. Results helped in concluding that the IR drop is underestimated by 11% when thermal impacts on power delivery are neglected. Also 51.8% of additional P/G TSVs are required to overcome the severe IR drop violation than the cases without considering thermal impacts. And maximum IR drop can be reduced by 42.3% & number of violated nodes reduced by 82.4% using the P/G TSV planning based on sensitivity model.

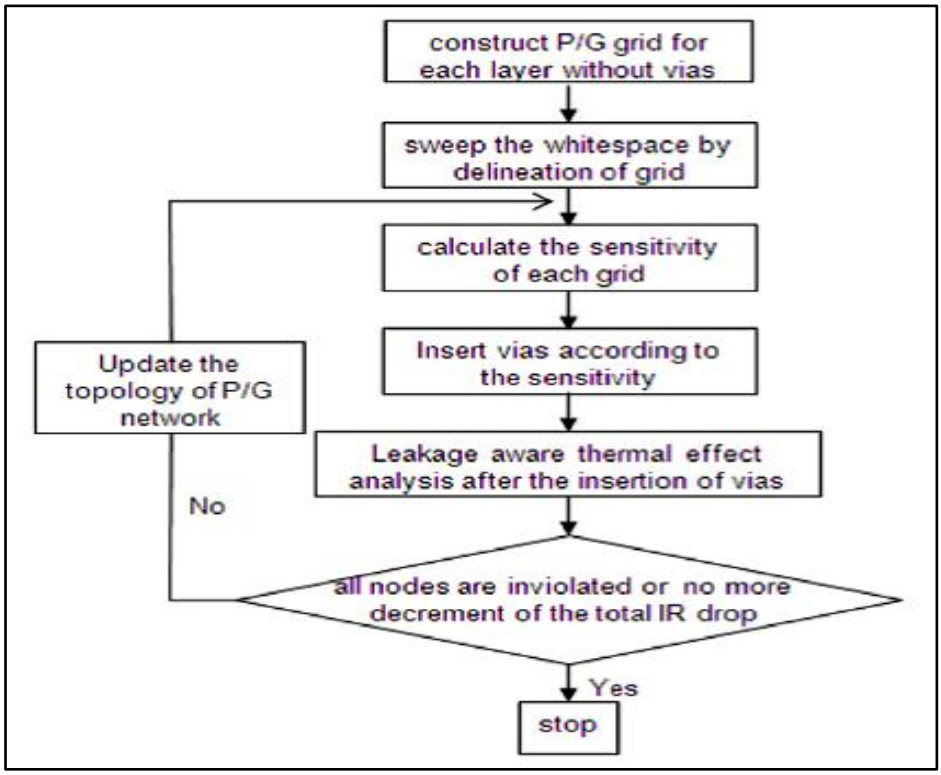

Figure 9. Overall flow of co-optimization of P/G grid topology [8]

The physical design of 3D partitioning, floorplanning and partitioning helps in determining the number of (signal) TSVs to be used. Many previous works have optimized the TSV count, wirelength and on chip temperature but have never considered the exploitation of high-level data transfer information obtained from high-level synthesis(HLS) on minimizing TSVs. **Byunghyun Lee**, **et.al[7]** proposed a set of algorithms two for TSV resource sharing and one for TSV refinement for TSV allocation optimization. Based on sharing granularity and design complexity two sharing algorithms are: (1) word-level TSV sharing and (2) bit-level TSV sharing. TSV sharing problem was resolved into a graph partitioning which employed two types of edges and solved by repetitive iterations. Whereas by using the greedy TSV splitting technique and register replication they also solved the TSV refinement. Along with this they also proposed a new TSV-aware 3D floorplanner to evaluate the wirelength more accurately. Their results showed a decrease in TSV number by 26.0% in word-level TSV with an increase in wirelength by 12.4% and a decrease in TSV count by 31.4% in bit level TSV with an increase of 18.1% in wirelength.

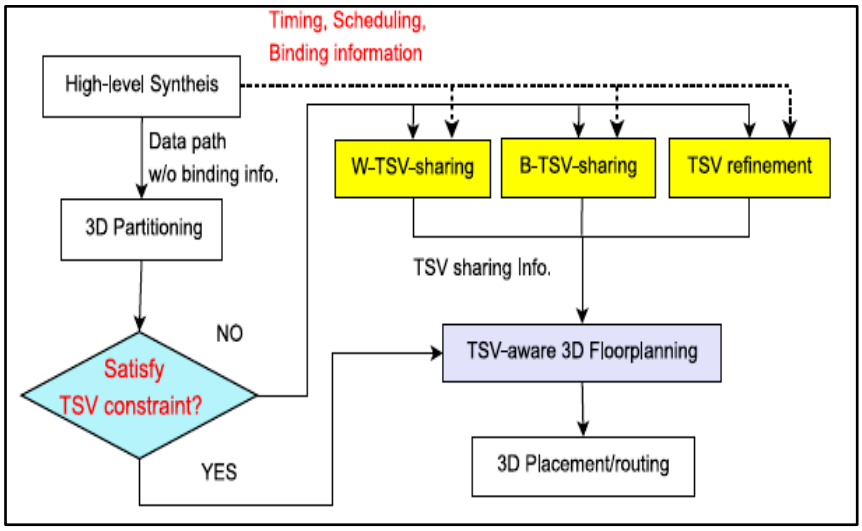

Figure 10. The algorithmic flow of the proposed word-levelTSV sharing for two layered data paths [7]

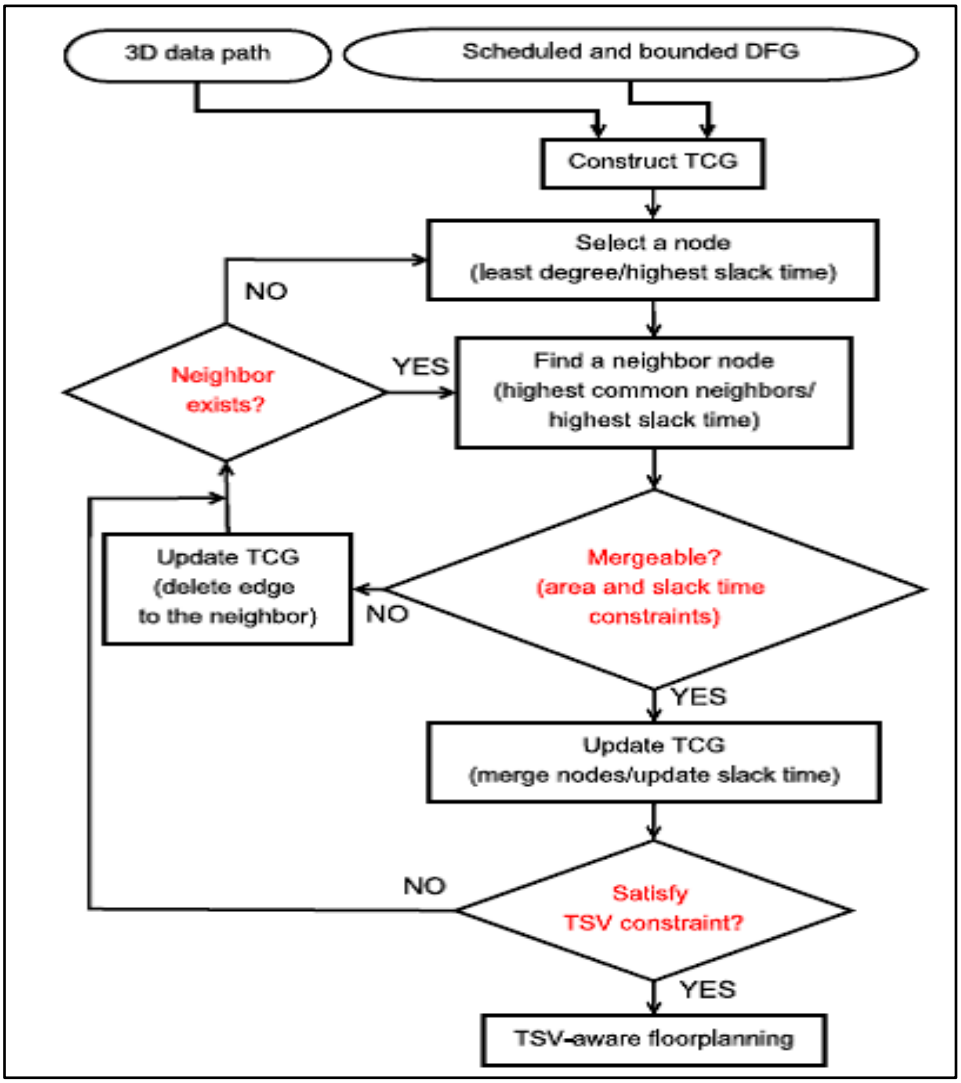

Figure 11. Algorithm flow of proposed word-level TSV sharing for two layer data paths [7]

2.5 Temperature Aware Routing Algorithms

Several 3D routing algorithms have dealt with the problems of 3D channel routing, maze routing but majority of them have not considered the thermal problem associated with 3D ICs in the routing phase. **Zhang Tianpei, et.al [17],** to lower the effective thermal resistance of material for reducing temperature of the chip, proposed a temperature-aware 3D global routing algorithm with appropriate insertion of thermal vias and thermal wires. Thermal vias and thermal wires have similar function where thermal vias are added as vertical interlayer thermal conduit having no electrical function and thermal wires conduct heat laterally within same layer. Thermal vias help spread heat paths over multiple thermal vias while vias perform conduction to heat sink. Routing scheme starts with routing congestion estimation and signal interlayer via assignment, finally followed by thermally-driven maze. Sensitivity analysis is utilized along with linear programming (LP) based thermal via/wire insertion to reduced temperature. And is repeated iteratively till temperature and routing capacity violations are resolved. Experimental result help in concluding that this routing algorithm reduces the peak temperature and remove routing congestion effectively.

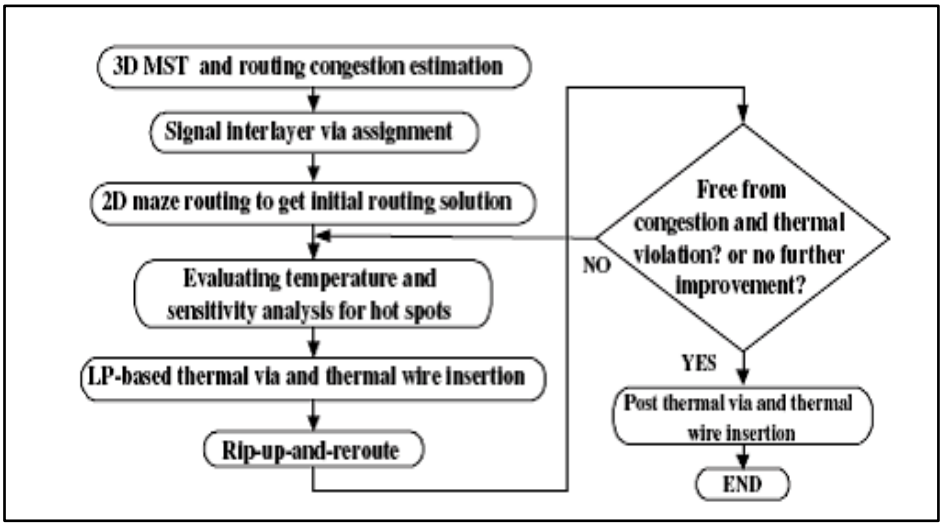

Figure 12. Flow for the temperature-aware 3D global routing algorithm

Different device layers stacked along with low thermal conductivity of bonding material leads to excessively high temperature. In a Steiner tree the location of TSVs have great impact on the overall topology as well as dealy at sink nodes of tree. In lowering temperature of chip TSVs play a vital role. **Pathak Mohit, et.al [14]** presented a thermal aware Steiner routing algorithm for 3D stacked ICs. It consisted of two main parts: tree construction and tree refinement. A delay-oriented Steiner-tree was made through the tree construction algorithm which included the minimization of Elmore delay function. Repositioning of through-silicon-vias (TSVs) used in existing Steiner tree while preserving original routing topology was done through the tree refinement algorithm for further thermal optimization. It was concluded that an improvement of 52% in performance at the cost of 15% wirelength and 6% TSV count increase for four-die stacked was reported which outperforms the 3-D maze routing.

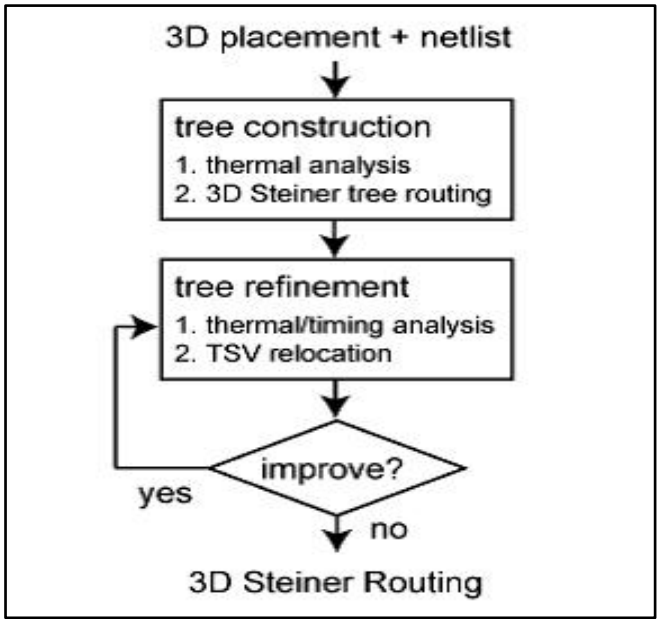

Figure 13. Overview of thermal-driven 3-D Steiner routing [14]

In the above approach [14] signal TSVs have been grouped into movable and non-movable TSVs by 3-D Elmore delay model. Movable signal TSVs don't deteriorate the performance and are placed near to hotspot region. Yet, this method does not exploit the outstanding thermal conductance of TSVs in thermal dissipation. **Hsu Po-Yang, et.al [16]** with the aim to minimize temperature with small wiring overhead, they proposed a three stage TSV locating algorithm in global routing for 3D IC. This work helps in constructing stacked signal TSV and utilize the thermal conductance of stacked TSVs to improve the thermal dissipation of the circuit. First algorithm was developed to stack signal TSVs by utilizing the thermal dissipation capabilities of stacked TSVs.

Second constructed aligned signal TSVs for the purpose of dissipating heat vertically without adding extra thermal TSVs thereby resulting in no additional area overhead for TSVs. Finally a gain function was proposed to concurrently consider interconnect wirelength and temperature profile. This gain function was utilized by the algorithm to optimize chip temperature with very small wiring overhead. Along with this, their algorithm moves TSVs on non-critical path resulting in no performance loss. Results demonstrated that a 17% temperature reduction with 3% wiring overhead and no performance loss was achieved with the help of 3-D Elmore delay model. Also in comparison to the work of Pathak and Lim [14] in which movable signal TSVs are relocated to reduce temperature, results has 8% more temperature reduction with same number of signal TSVs.

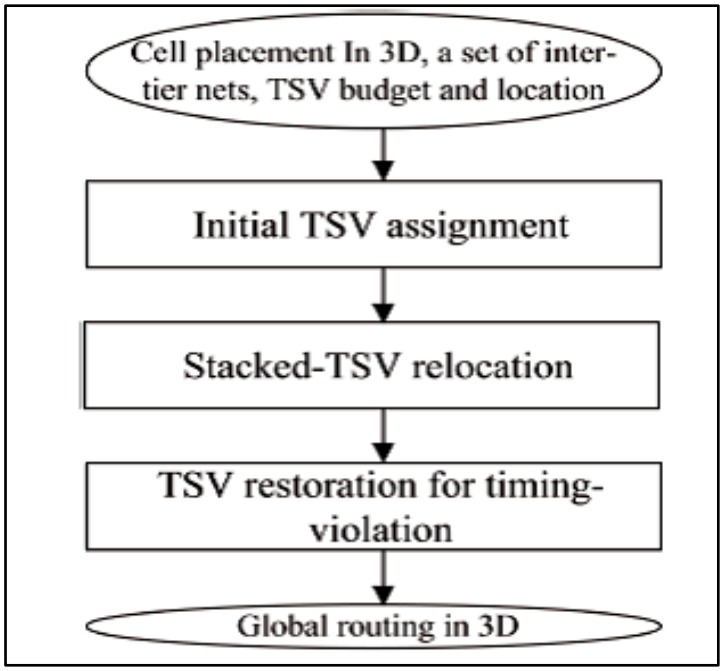

Figure 14. Overall flow of placing signal TSVs in global routing [16]

III. Summary

Experiments have indicated that the major issues faced by three dimensional integrated circuits, specially the thermal problems can be reduced with the help of various algorithms implemented at different design stages. Shrinking the size of ICs through vertical stacking of dies reduces the wirelength and delays but also results in increased power density along with higher on-chip temperature. Higher temperature leads to increased leakage power degrading the performance. To reduce the increased temperature TSVs are added to the 3D ICs which help in proper distribution of heat, released by various processing units and forming hotspot in the different layers. Thermal-driven floorplanning algorithm helps in reducing the on-chip temperature by 50% with low overhead. Also, the use MILP and MOEA helped in eliminating hotspot, reduce peak and mean temperature and reliability issues associated with temperature. Thermal aware 3D placement algorithm integrates thermal problem with placement process and reduce hotspot temperature to obtain a thermally balanced 3D placement. As well as a weighted via insertion approach considering both performance and heat dissipation along with resource constraint provide the best balance among temperature-via number and delay. Finally a thermal aware routing algorithm using Steiner routing for 3D stacked ICs resulted in an improvement of 52% in performance at the cost of 15% wirelength and 6% TSV count increase for four-die stacked which outperforms the 3-D maze routing.

IV. Future Scope

There are several areas in the field of thermal optimization of 3D ICs which have not been taken into consideration till yet. The impact of large interlayer vias on thermal resistance for every tile stack has not been considered. Also to speed up the thermal-driven 3D floorplanning algorithm without going through simulated annealing closed-form temperature formula need to be implemented [15]. Along with the above mentioned work, these thermal driven algorithms for different design stages can be implemented on a single 3D IC at various design stages. Implementation of the above algorithms at every design stage will enhance and improve the chip performance completely in various aspect, thereby making them more suitable for use in future.

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