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FPGA Based Power Efficient Chanalizer For Software Defined Radio

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ABSTRACT: *Multiple communication channel support in RF transmission, such as that in a Software Defined Radio (SDR) warrants the use of channelizers to extract required channels from the received RF frequency band and to perform follow-on baseband processing. This paper describes the process of channelization as it applies to low power and high-efficiency applications in wireless and Satellite Communications (SATCOM) domains. Smaller bandwidths and changing requirements of bandwidth calls for a programmable channel selection mechanism whereby channels and the resulting bandwidth can be selected based on target application, which is the primary principle in the Software Defined Radio based systems.*

Keywords: *Software defined radio, Channelization, Digital filter banks, Reconfigurability . Low complexity*

I. INTRODUCTION

A software-defined radio (SDR) system is a radio communication system which can tune to any frequency band and receive any modulation across a large frequency spectrum by means of a programmable hardware which is controlled by software. A Software radio is an enabling technology for future radio transceivers, allowing the realisation of multi-mode, multi-band, and reconfigurable base stations and terminals. However, considerable research efforts and breakthroughs in technology are required before the ideal software radio can be realised. The basic idea of SDR is to replace the conventional analog signal processing in radio transceivers by digital signal processing by placing the analog to digital converter (ADC) in receivers as close to the antenna as possible. Thus SDR should be able to support multiple communication standards by dynamically reconfiguring the same hardware platform. Also, SDR should be able to use the same architecture for any number of channels by simply reconfiguring the digital front-end as compared to a conventional radio transceiver whose complexity grows linearly with the number of received channels.

In this paper, we review some of the existing digital filter banks and investigates the potential of these filter banks for channelization in multi-standard SDR receivers. We also present two of our low complexity, reconfigurable filter bank architectures for SDR channelizers.

II. OBJECTIVES OF THE PROPOSED TOPIC

The overall objective of this work has been to develop a low-power Channelizer design that can be implemented on FPGA device. The design consists of schematic entry and RTL descriptions in Verilog. Specific tasks include:

1. Improvements of Polyphase Channelizer.
2. Efficient M-Path Polyphase channelization architecture is designed for highly efficient and low-cost (power and area) designs.
3. For providing a complete solution to the problem on hand, we need to address two aspects: 1)Programmability and 2) Low-Power and efficient design techniques. In a channelizer design, we need to perform basic channelization and secondary signal processing operations.

2.1. FILTER BANKS FOR SDR CHANNELIZERS

In this section, we review existing digital filter banks and discuss their suitability for channelization in SDR receivers.

1. Per-Channel (PC) Approach

The PC approach is based on a parallel arrangement of many one-channel channelizers. Each one-channel channelizer performs the channelization process.

The PC approach is a straight forward approach and hence relatively simple. But the main drawback is that, the number of branches of filtering-DDC-SRC is directly proportional to the number of received channels. Hence the PC approach is not efficient when the number of received channels is large. Furthermore, if the channels are of uniform bandwidth, a filter bank approach would be a cost-effective solution than the PC approach. Its hardware cost is very high, which has led to the development of DFT filter banks.

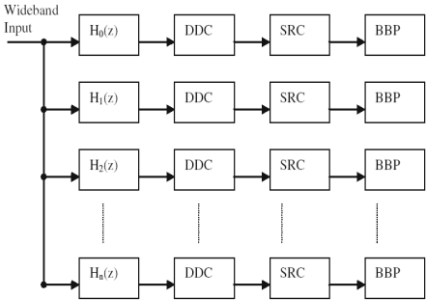

Figure 3 Per-Channel approach based channelization.

2. DFT Filter Banks

DFT filter bank is a uniformly modulated filter bank,which has been developed as an efficient substitute for PC approach when the number of channels need to be extracted is more, and the channels are of uniform bandwidth (for example many single-standard communication channels need to be extracted). The main advantage of DFT filter bank is that, it can efficiently utilize the polyphase decomposition of filters.

However, DFTFBs have following limitations for multi-standard receiver applications:

2.1. DFTFBs cannot extract channels with different bandwidths. This is because DFTFBs are modulated filter banks with equal bandwidth of all bandpass filters.

Therefore, for multi-standard receivers, distinct DFTFBs are required for each standard. Hence the complexity of a DFTFB increases linearly with the number of received standards.

2.2. Due to fixed channel stacking, the channels must be properly located for selecting them with the DFTFB.The channel stacking of a particular standard depends on the sample rate and the DFT size. To use the same DFTFB for another standard, the sample rate at the input of the DFTFB must be adapted accordingly. This requires additional sample rate converters (SRCs),which would increase the complexity and cost of DFTFBs.

2.3. If the channel bandwidth is very small compared to wideband input signal the prototype filter must be highly selective resulting in very high-order filter. As the order of the filter increases, the complexity increases linearly. Ideally, the reconfigurability of the filter bank must be accomplished by reconfiguring the same prototype filter in the filter bank to process the signals of the new communication standard with the least possible overhead, instead of employing separate filter banks for each standard. However reconfiguration of DFTFB suffers from following overheads:

1. The prototype filter needs to be reconfigured. Generally DFTFB employs the polyphase decomposition. Hence

reconfiguration can involve changing the number of polyphase branches which is a tedious and expensive task.

2. Downsampling factor needs to be changed. If down sampling is to be done after filtering, then we need separate digital down converters. This will add more cost.

3. The DFT needs to be reformulated accordingly which is also expensive.

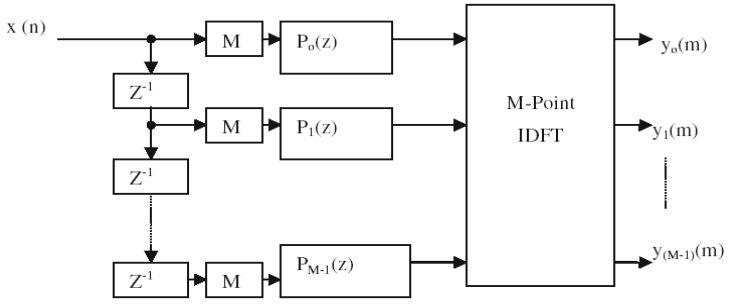

Figure 7 DFT filter bank.

In the case of multiple channel extraction of single standard signal i. e., extraction of many channels of identical bandwidth, the complexity of PC approach is given by N.L.fs, where N is the number of channels extracted, L is the total length of filters employed in all
the branches for PC approach and fs is the sampling frequency. The complexity of DFTFB is only L.fs which is N times lower than PC approach. But in the case of SDR, multiple channels of multiple standards need to be extracted.
In that case, the complexity of PC approach and DFTFB are NCSs and NSs respectively, where NC and NS are the number of channels and number of standards respectively.Thus the complexity of these channelizers can be reduced further if (1) the length of filter, L, can be reduced and (2) the same filter bank can be reconfigured to the new standard. Thus there is a need for developing new filter bank architectures for SDR receivers

3. ALTERNATIVE FILTER BANKS

A Goertzel filter bank (GFB) based on modified Goertzel algorithm was proposed in as a substitute to DFTFB. In GFB, the DFT is replaced by a modified Goertzel algorithm which performs the modulation of the prototype low-pass frequency response to any centre frequency which is not possible using DFT. This will eliminate the limitation of fixed channel stacking associated with DFTFBs.

This paper is an attempt towards design of FBs with reduced area complexity and improved reconfigurability when compared with conventional resampling-based FBs The frequency response masking (FRM) technique was originally proposed for designing low complexity sharp transition-band finite impulse response (FIR) filters. A reconfigurable low complexity channel filter for SDR receivers based on the FRM technique The objective of the work in was to realize a channel filter to extract a single channel (frequency band) from the wideband input signal.

New low complexity reconfigurable architecture for the modal filter whichcan simultaneously extract multiple channels is also presented in this paper. The proposed modal filter architecture can generate simultaneous frequency responses employing different delay line adders.Coefficient multiplication, which is the most power consuming operation, is done only once for obtaining different frequency responses simultaneously in the proposed modal filter architecture. Consequently the proposed FB offers low multiplier complexity when compared with other FBs in the literature. The proposed FB has been compared with the conventional PC approach, DFTFB, GFB.

III. FREQUENCY RESPONSE MASKING BASED FILTER BANKS

Ideally, the reconfigurability of the receiver must be accomplished in such a way that the filter bank architecture serving the current communications standard must be reconfigured with least possible overhead to support a new communication standard while maintaining the parallel operation (simultaneous reception/transmission of multistandard channels). To realize a filter bank which can be reconfigured to accommodate multiple standards with reduced hardware overhead, we have proposed a frequency response masking (FRM) based reconfigurable filter bank (FRMFB) in The FRM technique was originally proposed for designing application-specific low complexity sharp transition-band finite impulse response (FIR) filters.
Table 1 Comparison of channelization approaches,

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Parameter		PC Approach	DFTFB	PFT
Computational complexity	For multiple uniform bandwidth channels	Poor	Excellent	Good
	For multiple non-uniform bandwidth channels	Poor	Poor	Poor
Silicon cost		Poor	Excellent	Good
Initial design flexibility	Independent channels	Yes	No	No
	Number of channels	Selectable	2^N	2^N
Reconfigurability		Poor	Very poor	Poor

IV. REVIEW OF FREQUENCY RESPONSE MASKING APPROACH

In this section, a brief review of the FRM approach is presented. An SDR channelizer consists of a bank of filters known as channel filters for extracting individual channels from the digitized wideband input signal. FIR filters are employed as channel filters because of their linear phase property and guaranteed stability. Sharp transition-band FIR filters are required in the channelizer to meet the stringent wireless communication specifications. In conventional FIR filter designs, higher order filters are required to obtain sharp transition-band.

The complexity of FIR filters increases with the filter order. Several approaches have been proposed for reducing the complexity of FIR filters. In an FRM technique was employed for the synthesis of sharp transition-band FIR filters with low complexity. The advantage of the FRM technique is that the bandwidths of the filters are not altered and the resulting filter will have many sparse coefficients (because the subfilters have wide transition-band) resulting in less complexity.

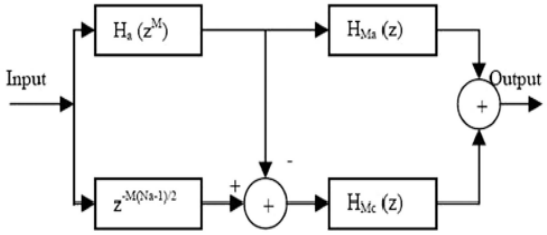

Fig. 1. FIR filter architecture based on FRM technique.

Fig. 1. FIR filter architecture based on FRM technique filters. The basic idea behind the FRM technique is to compose the overall sharp transition-band filter using several wide transition-band subfilters.In this paper, the sharp transition-band filter designed using FRM with necessary modifications has been employed as channel filter in an SDR channelizer.

The FRM approach can be more clearly explained with the help of Fig. 2. Fig. 2(a) represents the frequency response of an LPF Ha(z). The passband and stopband edges of the modal filter are fap and fas, respectively. The complementary filter of the modal filter Hc(z) is shown in Fig. 2(b). Replacing each delay of Ha(z) and Hc(z) by M delays, two filters Ha(zM) and Hc(zM) are obtained, and their frequency responses are shown in Fig. 2(c). Two masking filters HMA(z) and HMC(z) as shown in Fig. 2(d), are used to mask Ha(zM) and Hc(zM), respectively. If the outputs of HMA(z) and HMC(z), are added, as shown in Fig. 1, the frequency response of the resulting filter H(z) is shown in Fig. 2(e). Thus a sharp transition-band FIR filter is obtained using four subfilters. Since these subfilters are having wide transition-band specifications, the overall complexity will be much less than direct or conventional design of sharp transition-band FIR filters.

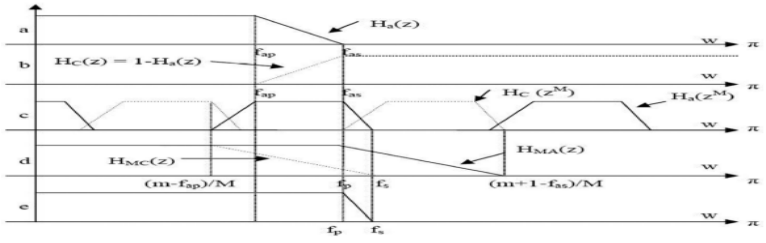

Fig. 2. Frequency response illustration of FRM approach.

In an SDR receiver, the specifications of the channelizer changes as the mode of communication changes. In conventional multi-mode channelizers a separate channelizer is needed for each mode, and reconfigurability is achieved by switching among distinct channelizers. This is not an efficient approach due to its increased hardware complexity and poor resource utilization. In this section, a reconfigurable filter bank is presented for SDR channelizers, which uses two blocks: a common hardware block at the front-end (modal filter) for multiple communication standards and a reconfigurable masking filter at the back-end. The complexity of the FB is dominated by the block at the front-end (as the order of the modal filter is substantially higher than that of the masking filter). Since the front-end hardware in the proposed scheme is the same (common) for all the communication standards, its complexity can be significantly reduced by using fixed-coefficient optimization techniques as in [12], which will ensure low complexity of the overall FB. However, in this paper, the idea discussed in has been extended by including the complete design details, generalized expressions for the modal and masking filters, practical design example, and actual implementation results on FPGA.The conventional FRM technique employs the direct form filter structure and therefore the critical path delay is proportional to filter length. But if transposed direct is employed, the critical path delay can be made independent of the filter length. Hence the transposed direct form is employed in the proposed FB. The proposed channelizer offers reconfigurability at two levels, named

1) architectural level, and 2) filter level.

A.Architectural Reconfigurability

The architectural reconfigurability of the FRM-based FB can be illustrated using the expressions (3). Though the proposed architecture is capable of handling multiple modes of communication, for ease of explanation, a dual-mode channelizer is used to illustrate reconfigurability. Let fp1 and fp2 be the passband frequencies and fs

and fs2 be the stopband frequencies of the channels corresponding to two modes (communication standards) of operation, m1 and m2 respectively. Reconfigurability can be achieved by using the same subfilters in Fig. 1 for both the modes. The parameters fap and fas remain unchanged for both the modes and therefore, the same modal filter is employed for both modes. The masking filters can be reconfigured by modifying the look up table (LUT) values which are explained in detail later. Thus,

fp1M1 ¡bfp1M1c = fp2M2 ¡bfp2M2c (4)

fs1M1 ¡bfs1M1c = fs2M2 ¡bfs2M2c (5)

where M1 and M2 denote the upsampling factors for the two modes m1 and m2 respectively, which can be obtained by solving (4) and (5). Thus by changing the number of delay elements, the same modal filter can be employed to work for both the modes. It is assumed that the two channels are at baseband or need to be down converted to baseband before filtering. However, the expressions (4) and (5) can be extended to bandpass channels also. The dual-mode channelizer can be extended to incorporate additional communication modes by choosing an appropriate nuIn addition to the architectural reconfigurability explained above, each of the subfilters of the proposed FB has been implemented such that they can be reconfigured. This enables the same FB architecture to operate for an entirely new communication standard.

The filter level reconfigurability is explained in the next section.

B. Filter Level Reconfigurability

Filter reconfigurability means changing the coefficients of each filter in Fig. 1 according to the specifications of the new standard. It is well known that one of the efficient ways to reduce the complexity of multiplication operation is to realize

it using shift and add operations. In contrast to conventional shift and add units used in previously proposed reconfigurable filter architectures, a binary common subexpressions (BCSs) based shift and add

unit has been employed in the filter architectures.

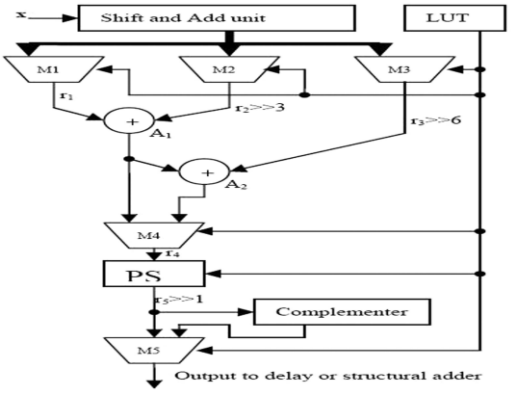

Fig. 3. Proposed reconfigurable filter architecture.

In two new reconfigurable FIR filter architectures based on a binary subexpression elimination (BSE) algorithm has been proposed. The architecture in consisted of a shift and add unit which will generate all the 3-bit BCSs using 3 adders. In this paper, the architecture in is modified for reducing its complexity. In the filter coefficients are stored in a LUT without any coding. As a result of this, if the first few bits are zeros, the adders employed in the architecture are unnecessarily used. The proposed architecture of the filter for an 8-bit

coefficient is shown in Fig. 3. M1 and M2 are 8 : 1 multiplexers; M3 is a 4 : 1 multiplexer and M4 and M5 are 2 : 1 multiplexers. The input is given to the shift and add unit whose output is shared among the multiplexers.

V. COMPLEXITY COMPARISON

In this section, we present a quantitative comparison of different filter banks reviewed in this paper. Table 2 showsthe comparison of the multiplication rate of the PC approach, DFTFB, GFB [5], MPRB our FRMFB and CDFB Multiplication complexity of a channelizer is defined as the total number of multiplications for extracting NI number of channels (of same communication standard) simultaneously. The multiplications involved in a channelizer can be grouped into three categories: Multiplications associated with (1) Channel filtering; (2) Digital down conversion and (3) Modulation of filters (this is not applicable for PC approach, FRMFB and CDFB).In Table 1, L represents the number of non-zero coefficients of the prototype filter for the PC approach, DFTFB and GFB, l represents the additional number of non-zero coefficients of the modal filter (because of over design) and masking filters in the proposed CDFB, lm represents the total number of non-zero coefficients for the modal filter and masking filters in the FRMFB (We have considered only non-zero coefficients as they will only result in multiplication complexity), and Fs represents the sampling frequency.

The multiplication complexities for PC approach, DFTFB and GFB are taken directly from. From Table 2, it is clear that the complexity of PC approach is directly proportional to the number of channels, NI.

Thus higher the number of channels, the PC approach is not hardware efficient. It can be seen that, the complexity of filtering (multiplication) operation is same for the proposed DFTFB and GFB and slightly higher for CDFB (because of overdesigning and masking filters). The MPRB consists of an analysis DFTFB and a synthesis DFTFB and hence the complexity is exactly twice that of DFTFB.As the FRMFB and CDFB do not require any DFT, there are no modulation complexity associated with FRMFB and CDFB. However separate (NI−1) digital down converters are required in the FRMFB and CDFB for converting all the channels except the low-pass channel to baseband. We have not considered FFT for the implementation of IDFT in DFTFB and MPRB, as FFT is appropriate only if the number of channels to be extracted is a power-of-two. From

Table 2, it can be seen that the over-all complexity of the proposed CDFB is lower than that of the PC approach, MPRB and GFB. Also, the proposed CDFB is less complex compared to DFTFB, when the number of channels, NI,increases. The FRMFB has the least filter length because ofthe wide transition-band subfilters compared to other filterbanks and hence has the least over-all complexity

Table 2 Multiplication rate of channelizers.

	PCApproach	DFTFB	GFB [5]	MPRB [10]	FRMFB [16]	CDFB [19]
Filter	$N_I \cdot L$	L	L	$2L$	lm	$L+l$
DDC	N_I-1	–	–	–	N_I-1	N_I-1
Modulation of filters	–	N_I^2	$N_I \cdot L$	$2N_I^2$	–	–
Sum	$N_I \cdot (L+1)-1$	$L+N_I^2$	$L \cdot (1+N_I)$	$2(L+N_I^2)$	$lm+N_I-1$	$L+l+N_I-1$

However, the design of FRMFB is a tedious task as it follows separate design procedure for each bandpass channel. For the extraction of channels of different standards (non-uniform bandwidth channels), only PC approach and FRMFB can be employed efficiently. Hence for non-uniform bandwidth channel extraction, FRMFB is a very good substitute for PC approach because of former's inherent low complexity and easy reconfigurability. Similarly for the extraction of channels of uniform bandwidth, CDFB is an excellent substitute for DFTFB, GFB and MPRB.

VI. CONCLUSIONS

In this paper,Low complexity and reconfigurability are the two key requirements of filter banks in SDR receivers.

The proposed architecture is inherently less complex and offers two level of reconfigurability: 1) at architectural level and 2) at filter level. The FRM technique is modified to improve the speed and reduce the complexity.

The filter bank based on frequency response masking can be used as an efficient substitute for the per-channel approach and the filter bank .

In future, to increase the flexibility of the proposed reconfigurable FB multistage FRM techniques will be investigated .

REFERENCES

[1]. Hentschel, T. and Fettweis, G."Software Radio Receivers," CDMA Techniques for Third Generation Mobile Systems. Norwell, MA: Kluwer Academic Publishers, 1999.

[2]. Mitola, J. Software Radio Architecture. Hoboken, NJ: Wiley, 2000.

[3]. Hentschel, T. Channelization for software defined base-stations. Annales des Telecommunications, 5—6 (May—June2002).

[4]. Pucker, L.Channelization techniques for software defined radio. Spectrum Signal Processing Inc., Burnaby, B.C., Canada, Nov. 17—19, 2003.

[5]. Kim, C., Shin, Y., Im, S., and Lee,W.SDR-based digital channelizer/de-channelizer for multiple CDMA signals. In Proceedings of IEEE Vehicular Technology Conference, vol. 6, Sept. 2000, 2862—2869.

[6]. Fung, C. Y. and Chan, S. C. A multistage filter bank-based channelizer and its multiplier less realization. In Proceedings of IEEE International Symposium on Circuits and Systems, vol. 3, Phoenix, AZ, May2002,

[7]. Abu-Al-Saud, W. A. and Stuber, G. L.Efficient wideband channelizer for software radio systems using modulated PR filter banks. IEEE Transactions on Signal Processing, **52**, 10 (Oct. 2004), 2807—2820.

[8]. Lim, Y. C. Frequency-response masking approach for the synthesis of sharp linear phase digital filters.IEEE Transactions on Circuits and Systems, **33** (Apr.2986), 357—364.

[9]. Hartley, R. I. Subexpression sharing in filters using canonic signed digit multipliers. IEEE Transactions on Circuits and Systems-II, **43** (Oct. 1996), 677—688.

[10]. Peiro, M. M., Boemo, E. I., and Wanhammar, L. Design of high-speed multiplierless filters using a nonrecursive signed common subexpression algorithm.IEEE Transactions on Computer Aided Design of

[11]. Integrated Circuits and Systems, **49**, 3 (Mar. 2002), [11] Xu, F., Chang, C. H., and Jong, C. C. Contention resolution algorithm for common sub

[12]. expression elimination in digital filter design. IEEE Transactions on Circuits and Systems-II, (Oct.2005)