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Simulation of Bridgeless SEPIC Converter with Modified Switching Pulse

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ABSTRACT: *In this paper, a new bridgeless single-ended primary inductance converter(SEPIC) power-factor-correction(PFC) rectifier is introduced. The proposed circuit provides lower conduction losses with reduced components simultaneously. In conventional PFC converters(continuous-conduction-mode boost converter), a voltage loop and a current loop are required for PFC.Simulation is done on bridgeless SEPIC and full bridge SEPIC and found that by working both in DCM conduction losses is less for bridgeless. In the proposed converter, the control circuit is simplified, and no current loop is required while the converter operates in discontinuous conduction mode.*

Keywords: *Continuous Conduction Mode (CCM), Discontinuous Conduction Mode (DCM), Duty cycle (D), IPower factor correction (PFC), Single ended primary inductance converter(SEPIC).*

I. Introduction

Today's commercial, industrial, retail and even domestic premises are increasingly populated by electronic devices such as PCs, monitors, servers and photocopiers which are usually powered by switched mode power supplies (SMPS). If not properly designed, these can present non-linear loads which impose harmonic currents. Harmonics can damage cabling and equipment within this network, as well as other equipment connected to it. Problems include overheating and fire risk, high voltages and circulating currents, equipment malfunctions and component failures, and other possible consequences. A non-linear load is liable to generate these harmonics if it has a poor power factor. Today's standards like International Electro technical Commission (IEC) 61000-3-2 limit the harmonics produced by these devices. Therefore, to satisfy the standards, power-factor-correction (PFC) converters are used for ac–dc conversion. The conventional PFC converter is a boost converter, and thus, the output voltage must be greater than the input voltage. In spite of this problem, this converter is widely used because of its simplicity.

In large number of applications, like offline low-voltage power supplies, where it is preferred to have the PFC output voltage lower than the input ac voltage, a buck-type converter is required. However, the input current of buck converter is discontinuous, and to filter this current, another passive filter must be used at the buck converter input. This is the characteristic of all converters in which a buck converter is at its input, such as buck–boost, non-inverting buck–boost, fly back, etc.. To resolve this problem, boost–buck converters like single-ended primary-inductor converter (SEPIC) and C´uk converters must be used. SEPIC is a DC to DC converter and is capable of operating in either step up or step down mode and widely used in battery operated equipment by varying duty cycle of gate signal of MOSFET. We can step up or step down voltage .For duty cycle above 0.5 it will step up and below 0.5, it will step down the voltage to required value. Various conversion topologies like buck, boost, buck-boost are used to step up or step down voltage. Some limitation like pulsating input and output current, inverted output voltage, in case of buck converter floating switch make it unreliable for different application. So it is not easy for conventional power converter design to maintain high efficiency especially when it step or step down voltage. All these characteristics are obtained in SEPIC DC to DC power conversion . Consequently, the input current would be continuous and also the output voltage can be lower than the input voltage. All these converters can be used in either discontinuous conduction mode (DCM) or continuous conduction mode (CCM). In CCM, a control circuit is required, but in DCM, the converter can operate at a fixed duty cycle to correct the input power factor (PF). DCM operation of boost converter causes the input current to become discontinuous.

Therefore, extra passive filter is needed to shape the input current toward sinusoidal waveform. In case of SEPIC and C´uk converters, due to the existence of two inductors in each converter, the input current is continuous even when the converter is operating in DCM.

II. Review of Literature and Statement of Problem

Conventional PFC converter is a rectifier followed by a boost converter as shown in Fig. 2.1. There are several disadvantages in this combination. At any given instant, three semiconductor devices exist in the power flow path. Also, special design of the dc-side inductor is necessary to carry the dc current as well as high-frequency ripple current. To overcome these problems, the bridgeless ac to dc rectifier is proposed as shown in Fig. 2.2.

Fig. 2.3 shows a conventional SEPIC PFC converter. In the literature, an interesting and novel bridgeless SEPIC PFC is introduced to minimize the conduction losses . This topology is similar to the bridgeless boost PFC rectifier .Despite the mentioned advantage, in comparison to the conventional SEPIC rectifier, this converter has three extra passive elements which contribute to the volume and weight of the converter. Another major problem with this converter is that it doubles the output voltage which considerably increases the size of output filter. To overcome these limitations, a new bridgeless SEPIC PFC is introduced in this paper. This converter has no extra (passive or active) elements in comparison to conventional SEPIC PFC. Also, in this converter, the conduction losses (number of active elements in the current path) are reduced in comparison to the conventional SEPIC PFC.

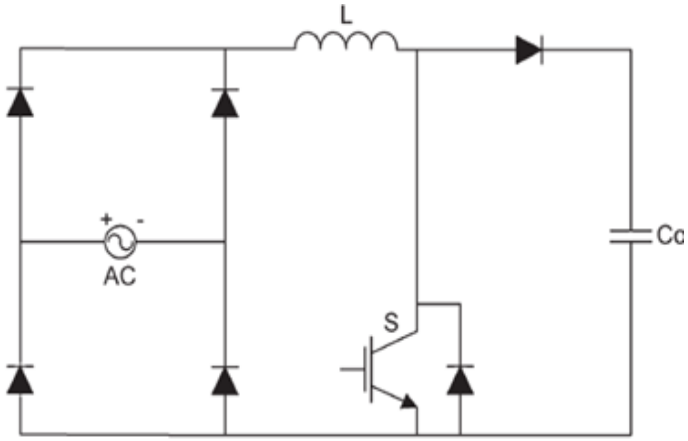

Figure. 2.1: Conventional PFC converter

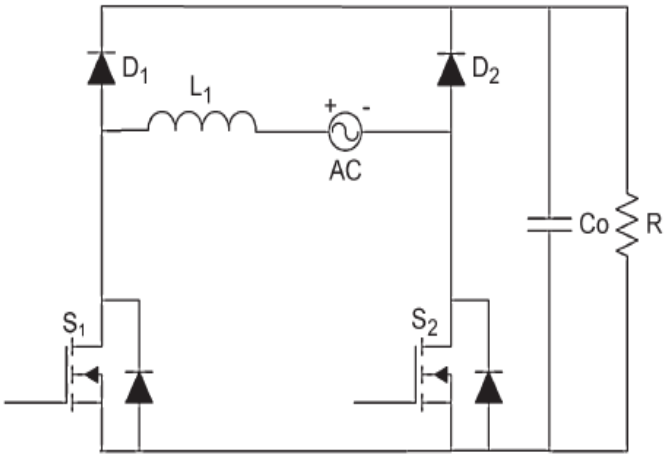

Figure 2.2: Conventional bridgeless boost PFC.

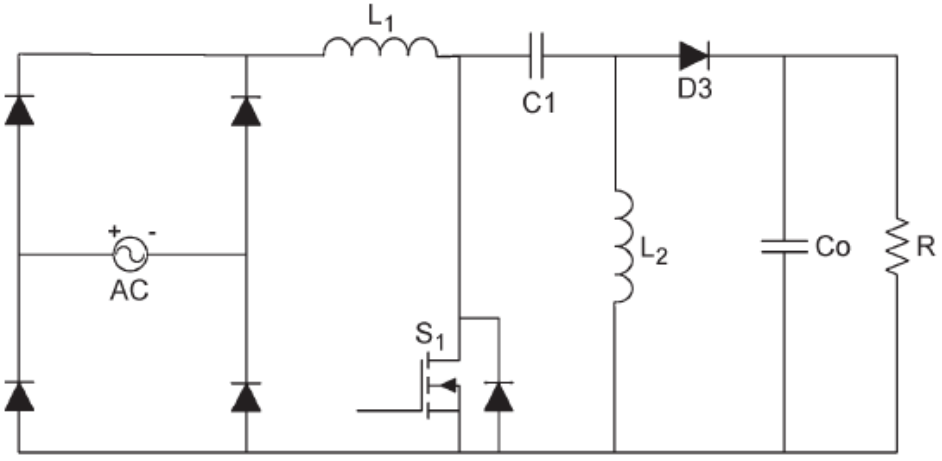

Figure 2.3 Conventional SEPIC PFC rectifier

III. Modified Bridgeless PFC Circuit Operation

Fig. 3.1 shows the power stage of a bridgeless SEPIC PFC rectifier. In this circuit, the SEPIC converter is combined with the input rectifier and operates like a conventional SEPIC PFC converter. The operation of this converter is symmetrical in two half-line cycles of input voltage. Therefore, the converter operation is explained during one switching period in the positive half-line cycle of the input voltage. It is assumed that the converter operates in DCM. It means that the output diode turns off before the main switch is turned on. In order to simplify the analysis, it is supposed that the converter is operating at a steady state, and all circuit elements are ideal. In addition, the output capacitance is assumed sufficiently large to be considered as an ideal dc voltage source (V_0) as shown in Fig. 3.2. Also, the input voltage is assumed constant and equal to $V_{ac}(t_0)$in a switching cycle.

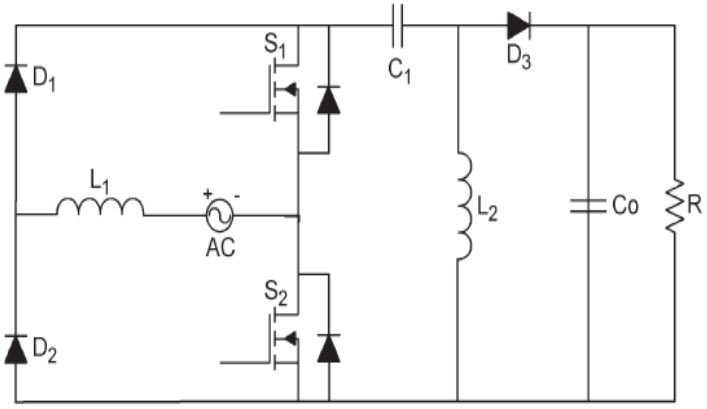

Figure 3.1: Proposed bridgeless SEPIC PFC

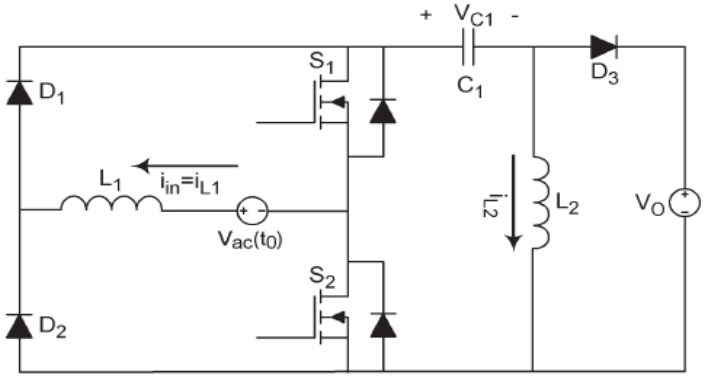

Figure 3.2: Equivalent circuit of the proposed bridgeless SEPIC PFC in a switching cycle.

Based on the aforementioned assumptions, the circuit operation in a switching cycle can be divided into three modes as shown by the equivalent circuits in Fig. 3.3. The theoretical waveforms are shown in Fig. 4.1. Before the first mode, it is assumed that the converter is in freewheeling mode. Therefore, D_1 and the body diode of S_2 are conducting, and all other semiconductor devices are off. Note that the voltage of C_1 follows the input voltage in DCM.

Mode 1: $[t_0 - t_1]$

This mode starts by turning S_1 and S_2 on. Input inductor current (L_1 current) starts to rise linearly by a slope of $V_{ac}(t_0)/L_1$. The voltage across L_2 is equal to the voltage of C_1 which follows the input voltage. Thus, i_{L_2} decreases linearly by a slope of $-V_{ac}(t_0)/L_2$. This mode ends by turning off *S*1. Based on the aforementioned operation, the following equations can be obtained:

$$i_{in}(t)=i_{L1}(t)=i_{fw} + \frac{V_{ac}(t_0)}{L_1}(t-t_0) \quad (1)$$

$$i_{L2}(t)=i_{fw} - \frac{V_{ac}(t_0)}{L_2}(t-t_0) \quad (2)$$

$$i_{sw1}(t)=i_{L1} - i_{L2} = (\frac{V_{ac}(t_0)}{L_1} + \frac{V_{ac}(t_0)}{L_2})t \quad (3)$$

where*i*fw is the freewheeling current which is equal to the input current. From (3), it can be concluded that *S*1 turns on under zero-current (ZC) switching condition.

Mode 2: $[t_1 - t_2]$

By turning S_1 and S_2 off, D_3 begins to conduct. Input inductor current decreases linearly by a slope of $-V_0/L_1$, and i_{L_2} increases linearly by a slope of V_0/L_2 until it reaches to i_{fw}. By substituting $t = t_1$ in (2), i_{L_2} is obtained as the following:

$$i_{L2}(t)=i_{L2}(t_1) + \frac{V_0}{L_2}(t-t_1) \quad (4)$$

Thus, the duration of this mode is

$$t_2-t_1=\frac{V_{ac}(t_0)}{V_0}(t_1 - t_0) \quad (5)$$

Mode 3: $[t_2 - t_3]$

This mode begins when D_3 turns off and the freewheeling mode starts. This mode ends by starting the next switching cycle at t_3. The current through inductors L_1 and L_2 are equal.
The duration of this mode is

$$t_3 - t_2 = T_s - (t_2 - t_0) \quad (6)$$

where*Ts* is the switching period.

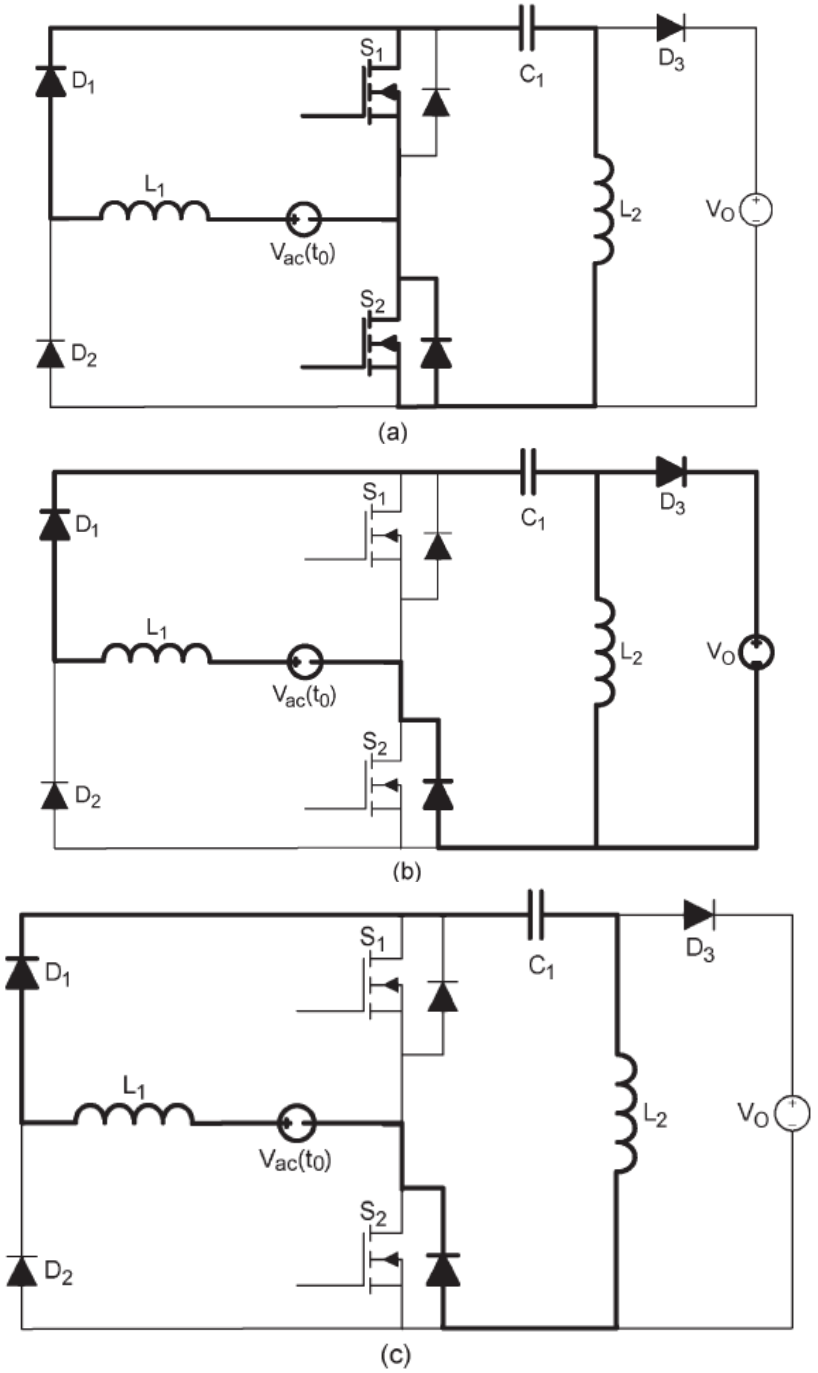

Figure 3.3: Equivalent waveforms of different modes of operation

The above equivalent circuit holds if the switching pulse is as in Fig 3.6 .If the switching pulse is as in Fig 3.7 then instead of body diode the switch path is taken in Fig 3.3 (b) and (c) i.ethe current via an intrinsic body diode is forced to flow through the channel of the switch. It can reduce the conduction loss on the switch further and the efficiency can be improved.

3.1 Comparison of Full Bridge and Bridgeless SEPIC Converter

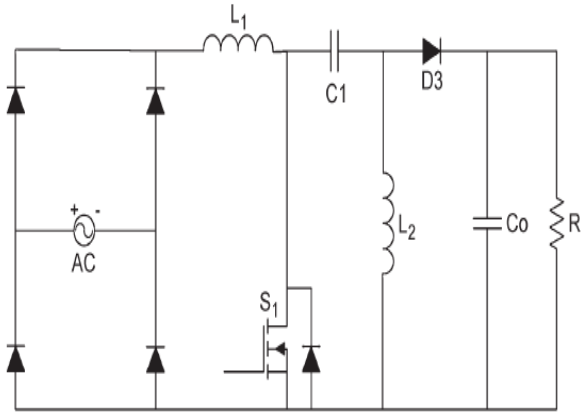

Figure 3.4: Full bridge SEPIC converter

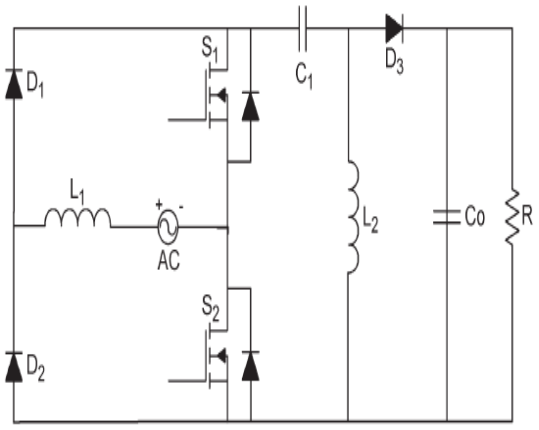

Figure 3.5: Bridgeless SEPIC converter

Conventional full bridge SEPIC converter is given PWM pulses and operated in switch on mode, switch off mode and freewheeling mode. Bridgeless SEPIC converter is given switching pulses such that one switch is continuously turned on during on half cycle with other switch is given PWM pulses, in the next half the switches are reversed. So in effect both switches off condition don't exist, so the conduction through the body diode can be omitted and thus reduce conduction losses and efficiency can be improved.

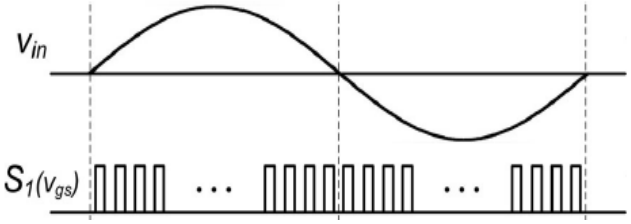

Figure 3.6: Switching pulses for full bridge SEPIC converter

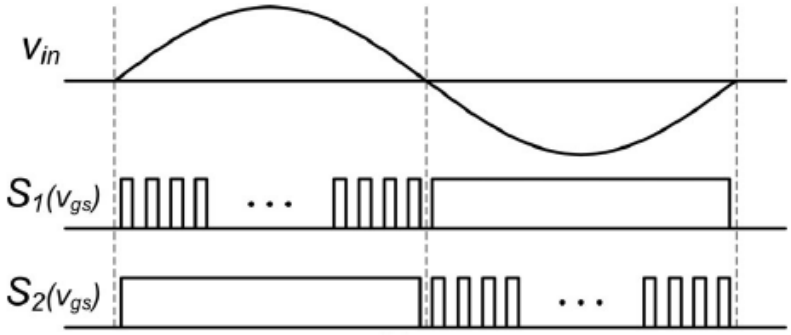

Figure 3.7:Switching pulses for Bridgeless SEPIC converter

IV. Design Procedure and Efficiency Improvement

Design procedure of this converter is similar to the conventional SEPIC PFC converter. Therefore, in this section, the design procedure is explained by an example. A converter with the following specifications is designed:

V_{ac} =$V_1 \sin(\omega t)$ = $180\sqrt{2}\sin(2\pi 50t)$

V_0=150 ± 5 Vdc

P_0=150 W

f_s=100 kHz

ΔI_L=20% I_1

where V_{ac} is the input sinusoidal voltage, V_0 is the output dc voltage, P_0 is the output power, f_s is the switching frequency, ΔI_L is the input current ripple, and I_1 is the input current peak.

Step 1: Input Current
From the output power and converter efficiency, the following equation can be obtained:

$$I_{in} = I_1 \sin(\omega t) = \frac{2P_0}{V_1 \eta} \sin(\omega t) \quad (7)$$

if efficiency, (η) is set equal to 90%, then

$$I_{in} = 1.32 \sin(2\pi 50t), \quad \Delta I_L = 0.26\text{A} \quad (8)$$

Fig. 4 shows that input current ripple is

$$\Delta I_L = \frac{V_{ac}(t_0) d}{L_1 f_s} \quad (9)$$

Step 2: Output Current
The output current is the average current of *D*3. Therefore, the output average current in a switching cycle can be obtained from the following equation:

$$i_{0,avg} = \frac{i_{op} d_1}{2} \quad (10)$$

where d_1 is the duty ratio of diode D_3 and is the peak current of D_3 which can be obtained from the following relation:

$$i_{op} = i_{L1}(t_1) + i_{L2}(t_1) = \left(\frac{1}{L_1} + \frac{1}{L_2}\right) V_{ac}(t_0) d T_s \quad (11)$$

Assuming $1/L_e = (1/L_1) + (1/L_2)$, then, from (5), (10), and (11), the following can be deduced:

$$i_{0,avg} = \frac{Vac^2(t_0) d^2}{2 L_e V_0} T_s \quad (12)$$

The average output current in one half of the line cycle becomes

$$I_{0,avg} = \frac{1}{\pi} \int_0^{\pi} i_{0,avg} \, d\omega t = \frac{V1^2 d^2}{4 L_e V_0} T_s \quad (13)$$

Step 3: Ensuring DCM Operation
To operate at DCM, the following inequality must hold:

$$d_1 < 1\text{-}d \quad (14)$$

By substituting (5) in the previous equation, the following inequality is obtained. This ensures that the converter operates at DCM.

$$d \leq \frac{V_0}{V_{ac}(t_0) + V_0} 0.392 \quad (15)$$

Using (4.8) and selecting d = 0.3, thus

$$L_e = \frac{V1^2 d^2}{4 V_0 f_s I_{o,avg}} = 147\mu\text{H} \quad (16)$$

From (9), L can be calculated as

$$L_1 = \frac{V_{ac}(t_0) d}{f_s I_{rip}} = 3.4\text{mH} \quad (17)$$

Therefore, L_2 can be calculated from the following equation:

$$\frac{1}{L_2} = \frac{1}{L_e} - \frac{1}{L_1} \tag{18}$$

Step 4: Output Capacitor (C_0)

Output ripple frequency is two times the input frequency, and at the worst case, the output current during the half period of ripple frequency must be provided by the output capacitor. Therefore, *CO* can be obtained from the following equation:

$$C_0 = \frac{P_0}{4 f_1 V_0 \Delta V_0} = 1000\mu H \tag{19}$$

where f_1 is the input frequency and ΔV_0 is the output ripple.

Step 5: Maximum Ratings of Semiconductor Elements

The maximum switch voltage and current can be obtained from the following equations:

$$V_{D,max} = V_{SW,max} = V_1 + V_0 = 400V \tag{20}$$

$$I_{D,max} = I_{SW,max} \approx I_1 + \Delta I_L - I_{L2,min} = 7.68\ A \tag{21}$$

where V_1 and I_1 are the input voltage and current peaks, respectively.

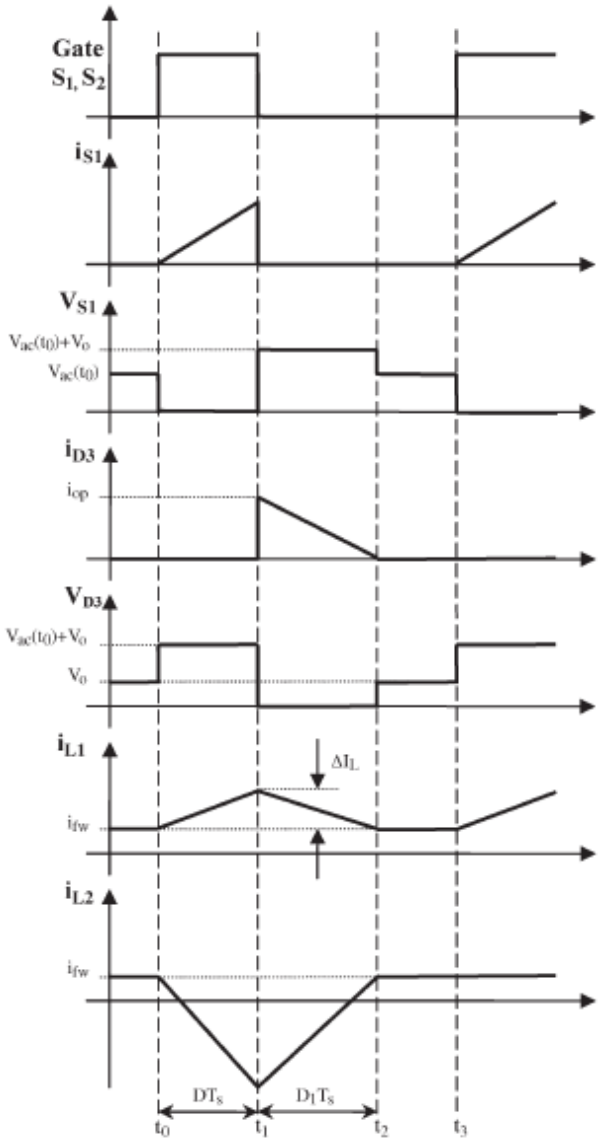

Figure 4.1: Theoretical waveform of proposed PFC converter

Step 6: Control Circuit

Based on the aforementioned operation of the proposed PFC circuit in DCM and the model given in for SEPIC PFC rectifier, the control circuit does not require a current loop to shape the input current. Therefore, any pulse width modulation IC can be used to control this PFC converter. The block diagram of the controller is shown in Fig. 4.1. It must be noted that, similar to conventional PFC, the voltage loop cannot compensate the 2*f*in output voltage ripple (*f*in is the input voltage frequency). Thus, the voltage loop must be designed so that the control circuit would neglect the 2*f*in ripple.

4.1 Efficiency Improvement

Based on circuit operation, it can be observed that one diode of rectifier is omitted in the current flow path and another diode is replaced by a switch. The voltage drop of a MOSFET is usually lower than a diode at low currents (In this application, the current is not so high). Therefore, it can be assumed that the losses of rectifier diodes are reduced from the total losses. By the following equations, the losses of these two diodes can be calculated

$$P_{D,avg} = \frac{1}{T}\int_0^T V_D I_D\, dt = \frac{1}{\pi}\int_0^\pi 1 * 1.3\sin(\omega)\, d\omega \qquad (22)$$

$$P_{D,avg} = 0.83W$$

where$P_{D,avg}$ is the average power loss in one diode of the input rectifier. Thus, the efficiency improvement of 150-W converter can be calculated from the following equation:

ηimprovement = $\frac{2P_{D,avg}}{150}$= 1.11%

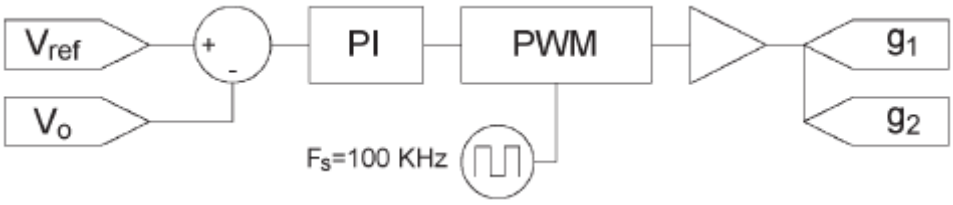

Figure 4.2: Control circuit

V. Simulation Results

The proposed bridgeless SEPIC PFC is simulated by MATLAB when V_{ac} = 180 Vrms, V_0= 150 ± 5 Vdc, ΔI_L= 20% I1, f_{sw} = 100 kHz and 150Woutput power. According to the aforementioned design considerations, the circuit elements are obtained as C_1 =1 μF, L_1 = 3.4 mH, L_2 = 100 μH, and C_0= 1000 μF.Fig. 5.2,5.3 shows the input current and voltage at full load .Fig 5.1Output waveform without controller. It can be observed from this figure that input current is in phase with input voltage and is practically sinusoidal with low total harmonic distortion and high Power Factor. Current waveforms of *L*1 and *L*2 are shown in Fig. 5.4. The voltage of *C*1 is shown in Fig.5.3.Simulation was done on full bridge SEPIC converter also in discontinuous conduction mode and could see that the conduction losses is more for this than full bridge SEPIC.

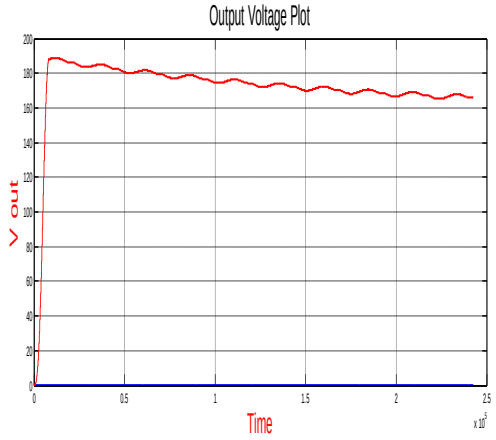

Figure. 5.1: Output

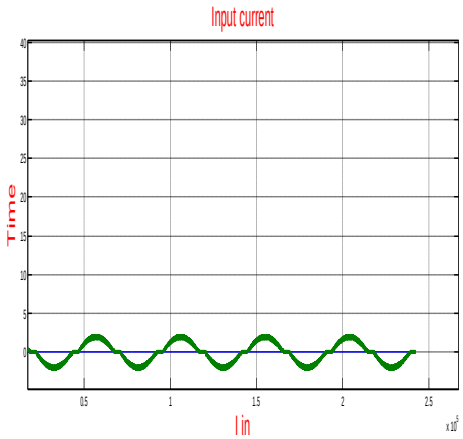

Figure 5.2: Input current

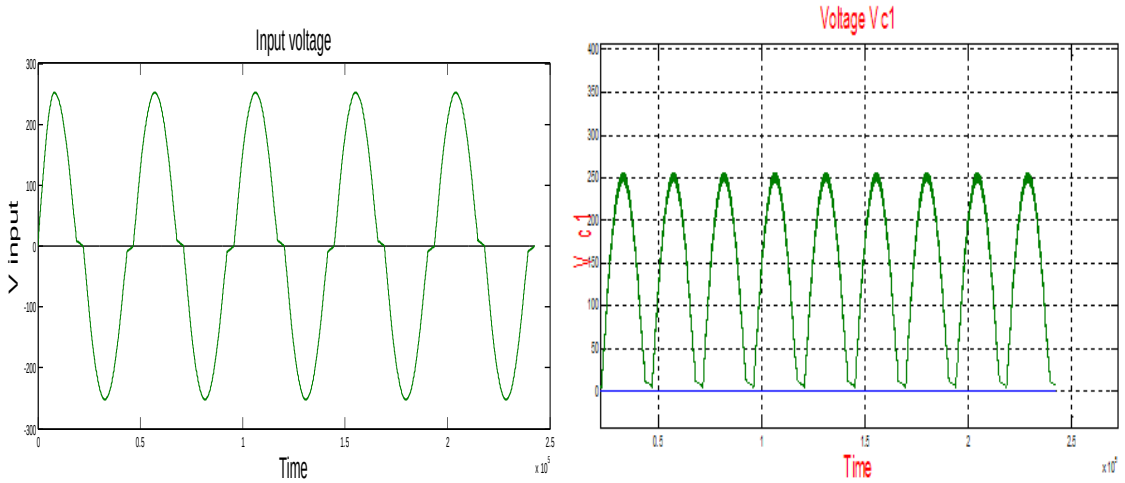

Figure 5.3: Input voltage Figure 5.4: capacitor

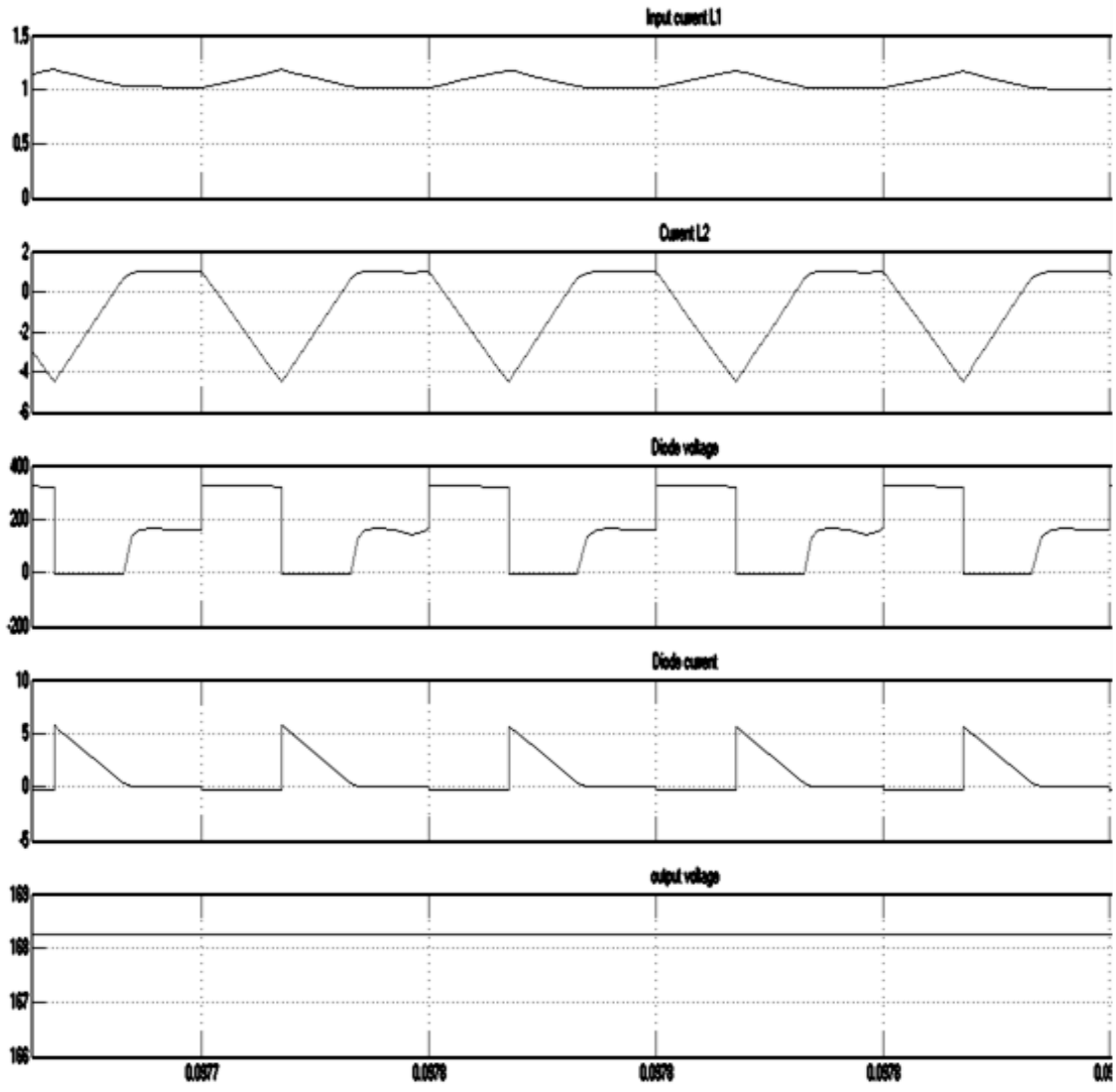

Figure 5.5: waveforms of open loop fullbridge SEPIC

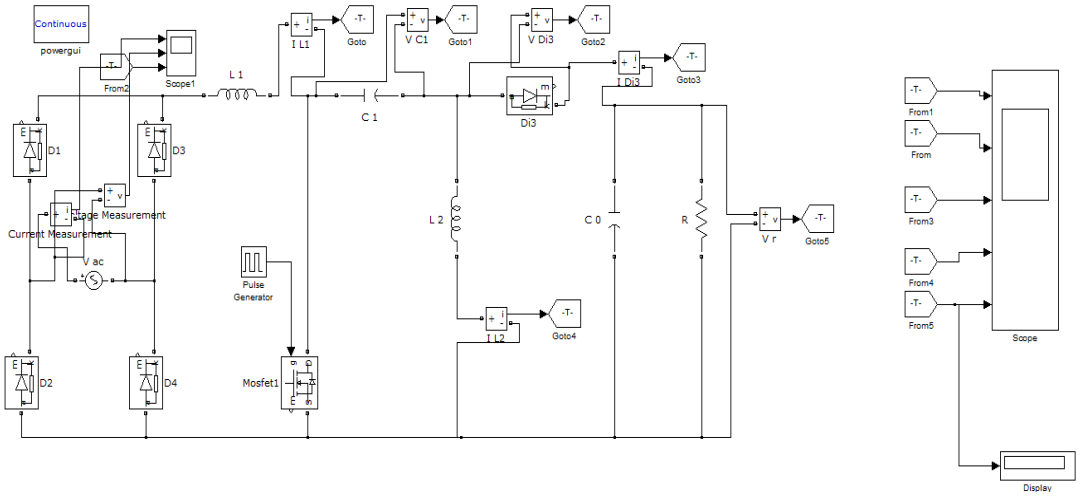

Figure 5.6: Simulink diagram of fullbridge SEPIC

Figures 5.1 ,5.2,5.3,5.4,5.5,5.6 shows the different waveforms of full bridge SEPIC converter.

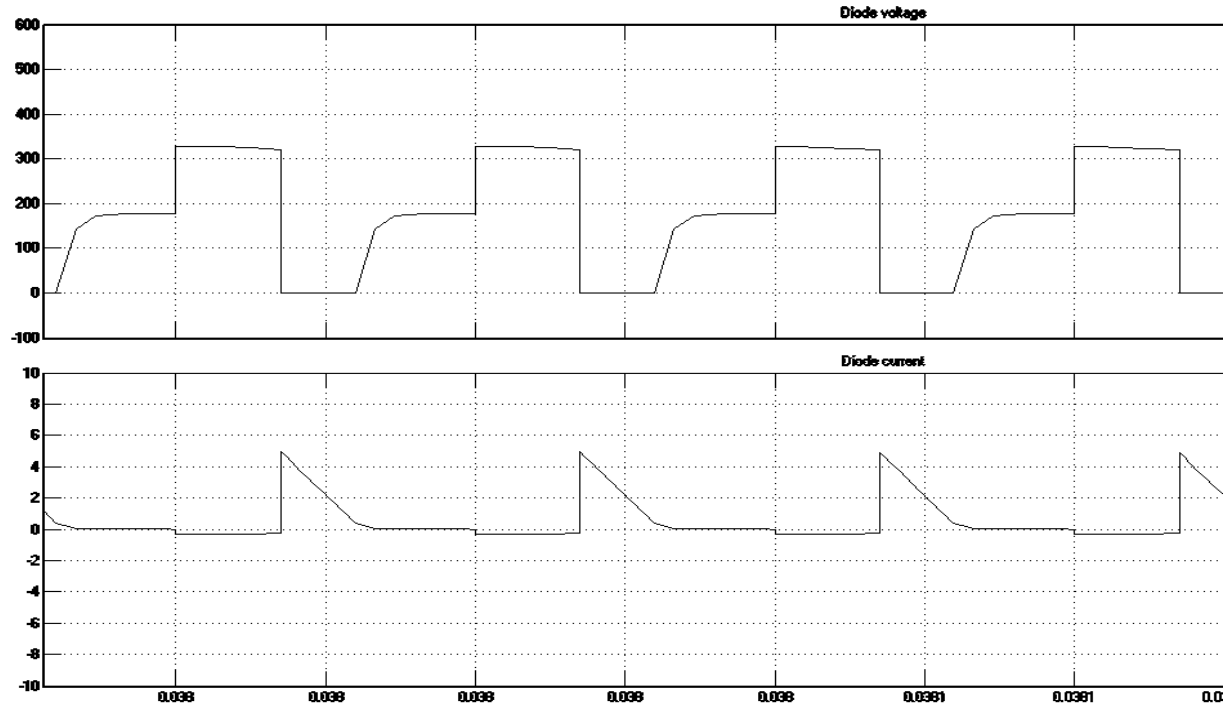

Figure 5.7: Diode voltage and current of bridgeless SEPIC

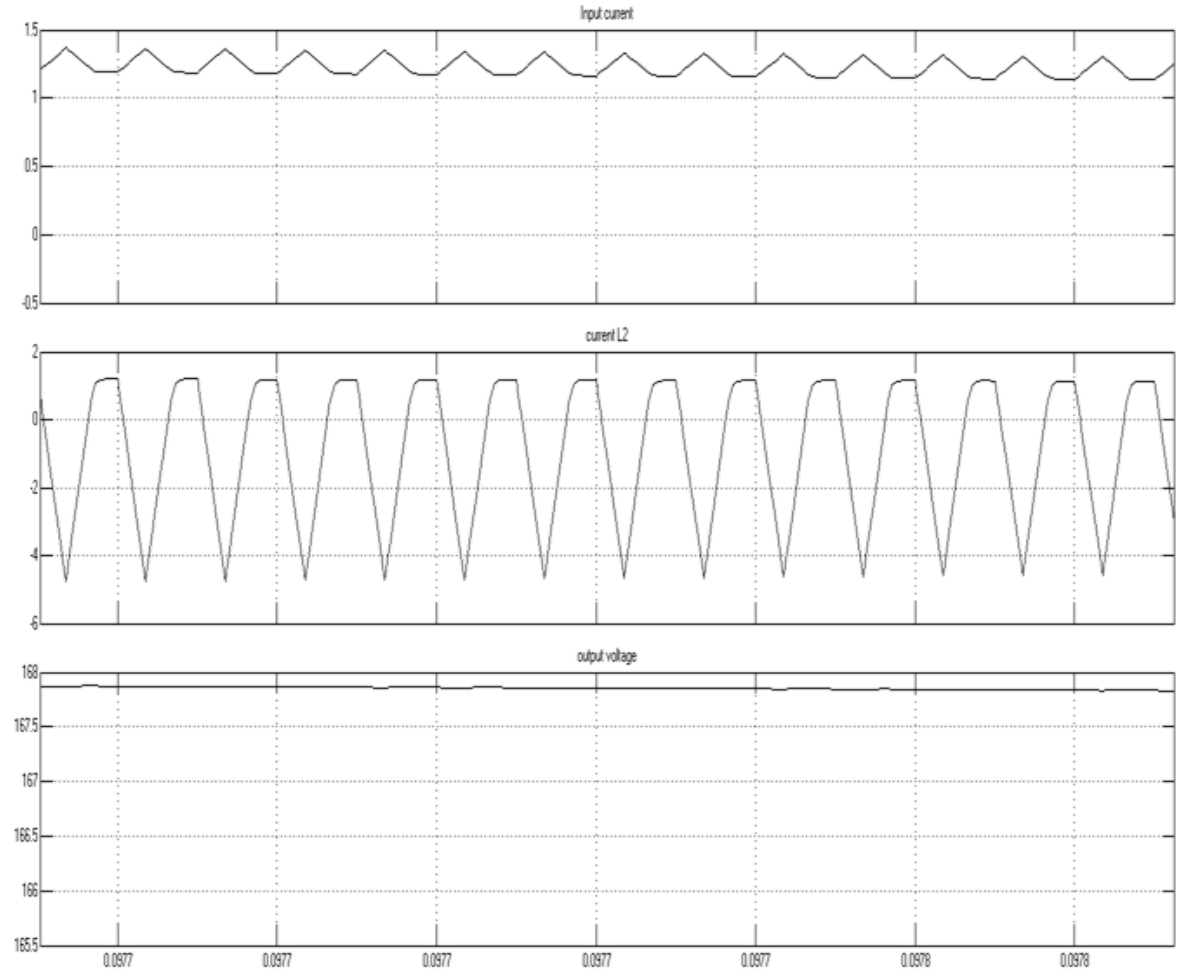

Figure 5.8: waveforms of bridgeless SEPIC converter

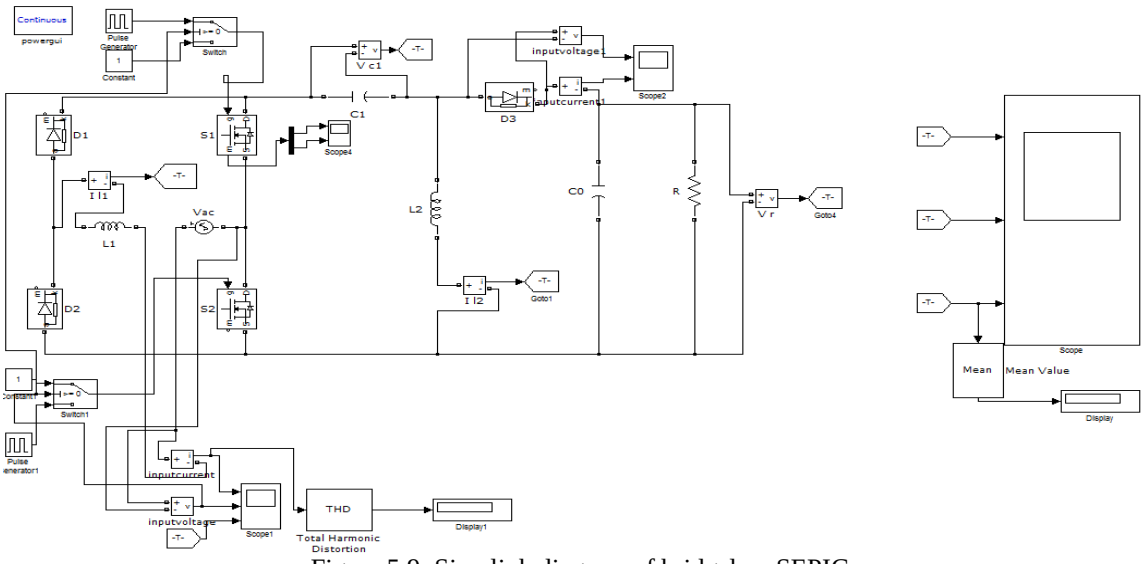

Figure 5.9: Simulink diagram of bridgeless SEPIC

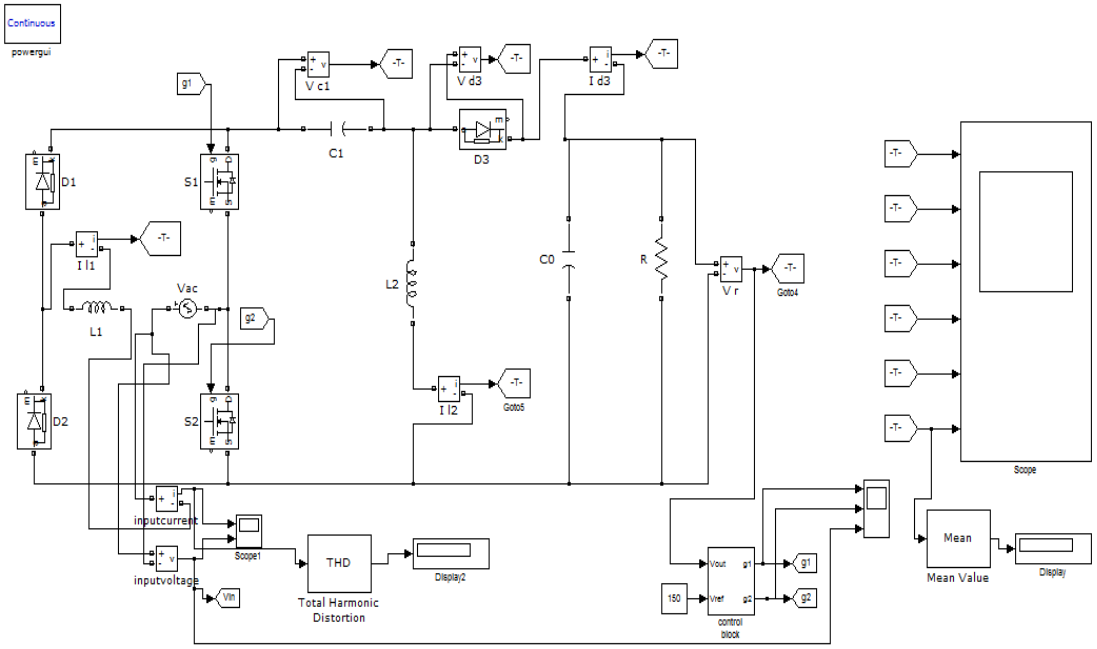

Figure 5.10: Closed loop SEPIC converter

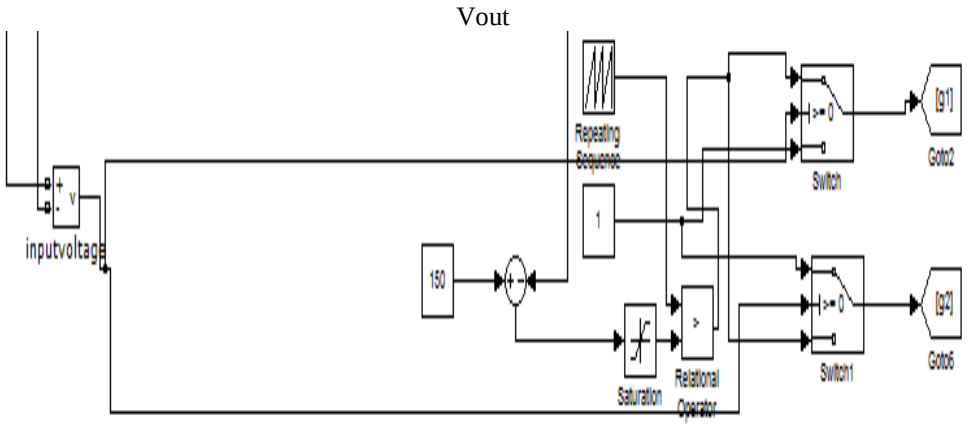

Figure 5.11: Controller circuit

VIII. Conclusion

In this paper, a new bridgeless SEPIC PFC rectifier has been introduced. The proposed circuit provides lower conduction losses with reduced components simultaneously. Two diodes of input rectifier are substituted with two switches in order to use one switch for SEPIC converter. In conventional PFC converters (CCM boost converter), a voltage loop and a current loop are needed for PFC.Here conventional is operated in DCM and compared with the bridgeless SEPIC. By using DCM operation in the proposed converter, the control circuit is simplified, and the current loop is omitted. The main features of the proposed converters include high efficiency, low voltage stress on the semiconductor devices, and simplicity of design. These advantages are desirable features for low-voltage power-supply applications.

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