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Low Power Design of Standard Digital Gate Design Using Novel Sleep Transistor Technique

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Abstract: *In the nanometer range design technologies static power consumption is very important issue in present peripheral devices. In the CMOS based VLSI circuits technology is scaling towards down in respect of size and achieving higher operating speeds. We have also considered these parameters such that we can control the leakage power. As process model design are getting smaller the density of device increases and threshold voltage as well as oxide thickness decrease to maintain the device performance. In this article two novel circuit techniques for reduction leakage current in NAND and NOR inverters using novel sleepy and sleepy property are investigated. We have proposed a design model that has significant reduction in power dissipation during inactive (standby) mode of operation compared to classical power gating methods for these circuit techniques. The proposed circuit techniques are applied to NAND and NOR inverters and the results are compared with earlier inverter leakage minimization techniques. All low leakage models of inverters are designed and simulated in Tanner Tool environment using 65 nm CMOS Technology (1volt) technologies. Average power, Leakage power, sleep transistor*

Keywords: *Average power, Leakage power, sleep transistor.*

I. Introduction

In modern electronics the peripheral circuits based on SRAM like input drivers, word line drivers, and output drivers etc. occupy major portion of on chip caches in processors. Due to this tremendous attention is given towards savings of leakage power in peripheral circuits for improving the device performance. The on chip memory utilization involves long inactive states during cache misses. Thus a large time is spent in sleep modes in various functions. It indicates that static power reduction is getting a important issue of concern for memory utilization based peripheral device.

For a CMOS circuit the power dissipation occurs during the active mode of operation due to dynamic and static components but in the standby mode, the power dissipation is due to the standby leakage current [2] [3]. In the hand held devices based on nanometer technologies static power consumption is a prime concern. Due to down scaling in the size down along with the improvement in operating speeds of CMOS VLSI circuits; the leakage power is increased with the growth of technology. We have found in various literatures that as the geometries are getting smaller threshold voltage as well as oxide thickness decrease to maintain the device performance.

Hence with the successive growth of technology reduction in channel length has decreased the requirement of levels of threshold voltage and gate oxide thickness. Due to reduction in threshold voltage the consequences are observed in the form of exponential increase in leakage current. For fulfilling the purpose of successive down scaling of transistors leakage current is going to be a limiting factor [1].In nanometer range based technology feature sizes are very small due to this smaller length of channels causes increase in sub threshold current because the transistors are not kept completely switched off.

In the growing technology the number of transistors is rising, transistors leakage occurs even they are not activated this causes significant dissipation of power during the inactive state of circuits for a given area. Hence with the successive growth of the technology leakage power in an integrated circuit is also increasing.

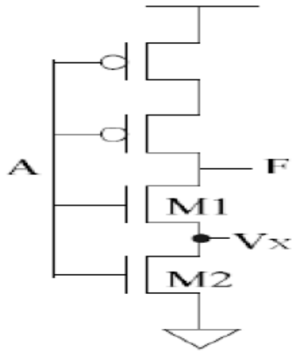


Fig 1: Transistor stack Connection for Forced Inverter

II. Related Work

From above discussion it can be observed that it is very necessary to reduce the idle mode operation static power in the peripheral circuits that utilizes SRAM for cache memory based functions. In all the processors SRAMS are integral and very important components. In addition to this in Embedded Systems SRAMS occupies a larger area on chips. So it is required to apply various leakage power reduction methods to SRAMs to increase valuable battery usage time in hand held mobile devices. We have analyzed many VLSI techniques that can help for leakage power reduction. Some of the techniques are such that they can provide a very perfect approach to reduce leakage power; but every technique has some disadvantages that implements limitations in the application of each technique. We have sorted out two new approaches that can be proposed to apply to reduce total power consumption, thus this can help in getting a new choice for low-leakage power VLSI design techniques. We have also studied previous techniques and compared with the two new methods presented in this report.

The method that has already proved its advantages in reducing leakage power in inverters is the making use of transistor stacking [4].With more than one transistor in the stack is kept in turned off state it has been found that sub threshold leakage current flow reduces in a stack of series connected transistors as shown in figure 1. This phenomenon is called as stacking effect. In the article [5] it has been proposed that the use of sleep transistors helps in leakage reduction, it is also known as gated-VDD and gated-GND techniques. This technique is used to cut off pull-up or pull-down or both networks from supply voltage or ground using sleep transistors. In this technique either i) an additional NMOS sleep transistor is used between pull-down network and ground or/and an additional PMOS sleep transistor is used between pull-up network and VDD.

2.1. Proposed Method

The sleep transistor is turned on during active mode of operation and turned off during idle or standby mode of operation. When the sleep transistor is off the virtual ground terminal VG will be at a nonzero potential. The gate to source voltage of off transistor M2 becomes negative and its threshold voltage increases. This has an effect of reducing sub threshold current flowing between drain and source of the transistor. The substrate to source voltage and drain to source voltage also reduce and give rise to higher threshold voltage. All these effects cumulatively add up to lowered sub threshold current that flows in the off transistors.

In this work we have proposed two novel techniques for reduction of leakage current in inverters with and without application of state retention property. We have used these techniques for the reduction of power dissipation during inactive (standby) mode of operation. The reduced power is compared to traditional power gating methods for circuit techniques.

As we have discussed before that in CMOS circuit power dissipation occurs due to dynamic and static components during the active mode of operation and standby condition the power dissipation is by the standby leakage current.

The dynamic switching power (PD) and leakage power (PLEAK) can be evaluated by following equations:

$$P_D = \alpha f c V^2_{DD} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$
$$P_{LEAK} = I_{LEAK} V_{DD} \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (2)$$

In the above equations the various terms are described below:

α : switching activity

f : operation frequency

C : the load capacitance

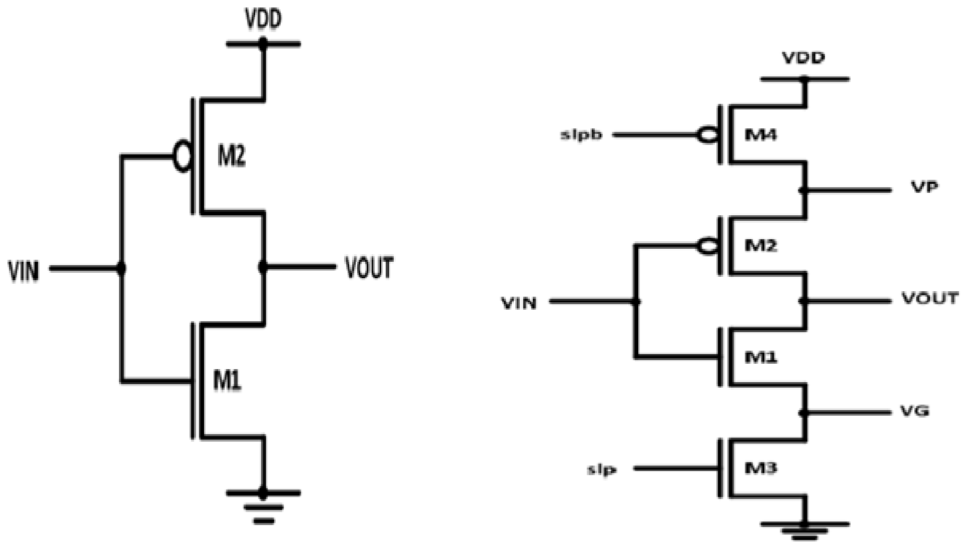
VDD : supply voltage and

I_{LEAK}: the cumulative leakage current due to all the components of the leakage current.

For CMOS Inverters current flows from Source to Drain in ideal conditions when $V_{GS} > V_T$. But in the case of real transistors current instead of cut-off abruptly below a given threshold it drops exponentially. This type of exponential drop off conduction is called as leakage conduction and it causes an undesired conduction in a state when transistor is considered as nominally off. This leakage current is also taken as sub threshold or weak inversion current that flows from drain to source when the transistor is off during the state when gate voltage is kept below the threshold voltage. The leakage current depends on various process parameters in the MOSFETs, like the transistor size, the quiescent state of the circuit [3] etc.
In this work we have considered various methods to reduce the sub threshold leakage current by increasing threshold voltage V_{TO}, increasing V_{SB} and reduction of V_{GS}, V_{DS} and lowering the temperature.

We have observe that the reduction in leakage current can be achieved using both process- and circuit-level techniques. In the process level the reduction in leakage current can be obtained by governing the dimensions like length, oxide thickness, junction depth and doping profile of the CMOS transistors and in the circuit level, threshold voltage and leakage current of transistors can be effectively controlled by controlling the voltages of different device terminals named as drain, source, gate and substrate body.
In this paper we have applied novel static power reduction method in inverters and SRAM memory peripheral circuits. This proposed method has tremendous scope in extending it for. Application related to peripheral devices like write data drivers, decoders etc.

The proposed design of novel low leak inverter uses new power gating technique in which PMOS transistor is used in the pull down path and NMOS transistor in the pull up path as sleep transistors. Both the sleep transistors are kept on during the active mode of operation. The PMOS
pull down transistor holds the virtual ground (VG) node at a higher potential than ground and the NMOS pull-up transistor maintains the virtual power (VP) node at a lower potential.



(a) Normal Inverter (b) Sleepy Inverter

Fig 2: Connection Diagram for a normal inverter and sleep inverter using transistor stack connection.

This helps the current flowing in the circuit to reduce and causes lower power dissipation during active mode. During the idle mode the sleep transistors are off. This provides a very large impedance path establishment across the nodes VP and VG in comparison to the traditional power gating method.

This method provides maximum reduction in static power during periods of inactivity or sleep state. However the output states during active mode of operation will not be at good logic1 and logic 0 values. To obtain good logic output levels during active mode of operation and to achieve the retention of previous output state, state retention transistors are introduced across the sleep control transistors. This state retention technique has resulted in state retention at lower total power dissipation as compared to previous best known techniques. This work also addresses leakage power reduction in buffer chains. Word line drivers have been designed with novel low leak inverters.

2.1.1. Low leakage Novel sleepy NAND, NOR inverter modeling

The novel technique based sleepy inverter for low leakage applications is shown in figure 2b.This novel sleepy inverter gives very good reduction in leakage power but if we consider the output voltage levels they are not at good logic1 and logic 0 values. The large amount of reduction in leakage power has uses in inverter chains provided in the peripheral circuits of SRAM related memory devices and systems like data/ address I/O driver, row pre decoder, word line driver, etc. if reduced voltage level is not as a constrain for limiting factor.

The novel sleepy inverter consist of PMOS transistor for giving pull down sleep transistor actions and NMOS transistor for pull up operations of sleep transistor. During active mode the sleep signal slp is logic 0 and sleep bar signal slpb is logic 1. In the active period duration the sleep transistors M3 and M4 are on. The node VG at higher potential with respect to ground and VP is at a lower potential with respect to VDD. In this manner the inverter circuit has lower potential difference for node VP and VG. In this way current though the circuit is reduced and power dissipation also get reduced. During operations in standby mode the slp signal is at logic 1 and signal slpb is logic 0. In this case M3 and M4 transistor are off and gives very high impedance between the path of VDD and ground and in this way leakage current is lowered consequently. It has been found that the power dissipation in standby mode duration operation is lowest. In this article we have described a design based on novel sleepy transistor based NAND and NOR inverter. The SLEEPY NAND GATE technique for low leakage operation of an inverter is shown in below figure 3. This inverter provides significantly leakage power reduction as compared to design of the conventional NAND using CMOS for leakage power reduction using 65nm technology with power supply V_{dd} (Vpwr) 1v and also considering the speed of the devices.

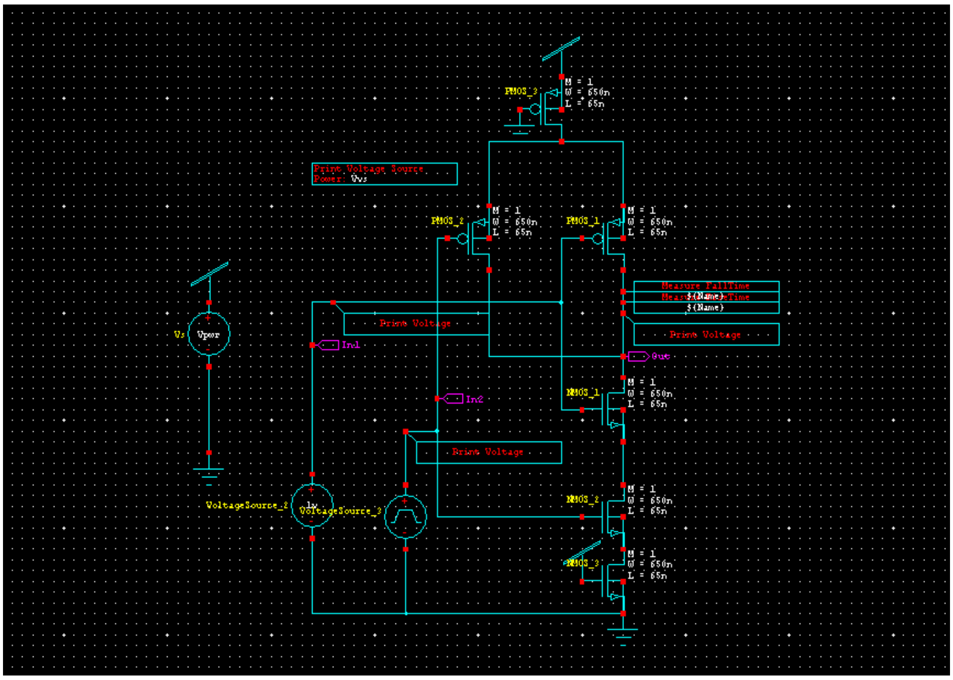


Figure 3: Sleepy NAND inverter for active MODE (slp=1, slpb=0).

The SLEEPY NOR gate for low leakage operation of an inverter is shown in below figure 4.
Figure 4 shows Sleepy NOR for active mode. During normal operation the sleep signal slp is held at logic 1 voltage level and complementary sleep signal slpb is held at logic 0 voltage levels. When inverter has to function in stand-by or sleep mode the signal slp is held at logic 0 and signal slpb is held at logic 1.

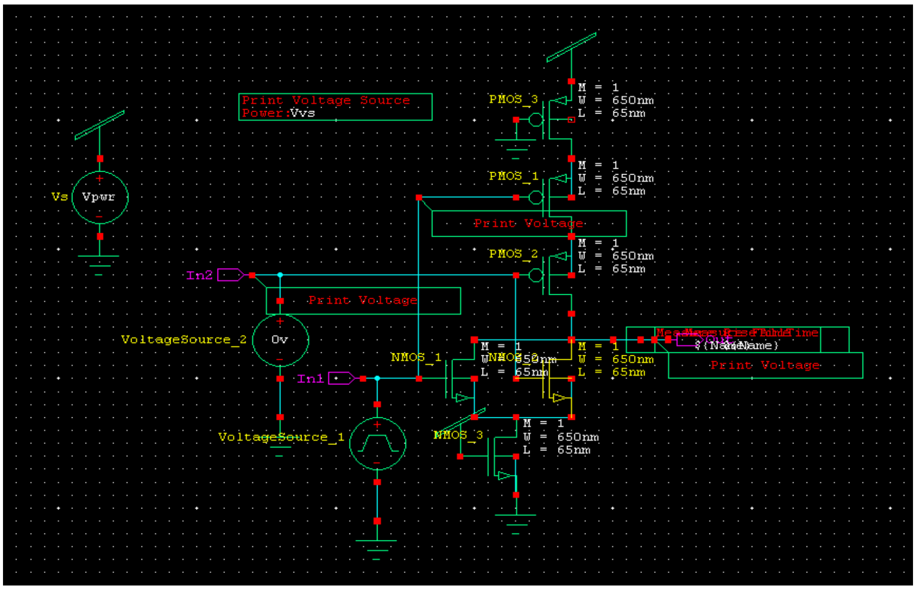


Fig 4: Sleepy NOR For Normal mode (slp=1, slpb=0)

The Novel SLEEPY NAND Inverter technique for low leakage operation of an inverter is depicted in below figure. This inverter though provides significantly leakage power reduction.

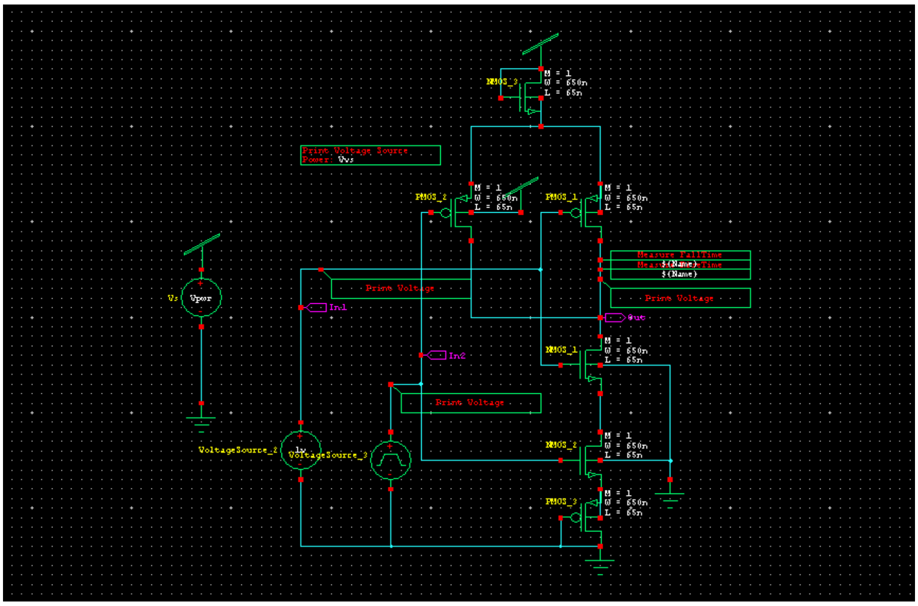


Fig 5: Novel Sleepy NAND Inverter for Normal Mode (slp=0, slpb=1)

Above figure 5 shows Novel Sleepy NAND gate for active mode. During normal operation the sleep signal slp is held at logic 0 voltage levels and complementary sleep signal slpb is held at logic 1 voltage level. When inverter has to function in stand-by or sleep mode the signal slp is held at logic 1 and signal slpb is held at logic 0. Similarly NOVEL SLEEPY NOR gate for low leakage operation of an inverter is shown in below figure 6. This inverter also provides significant leakage power reduction.

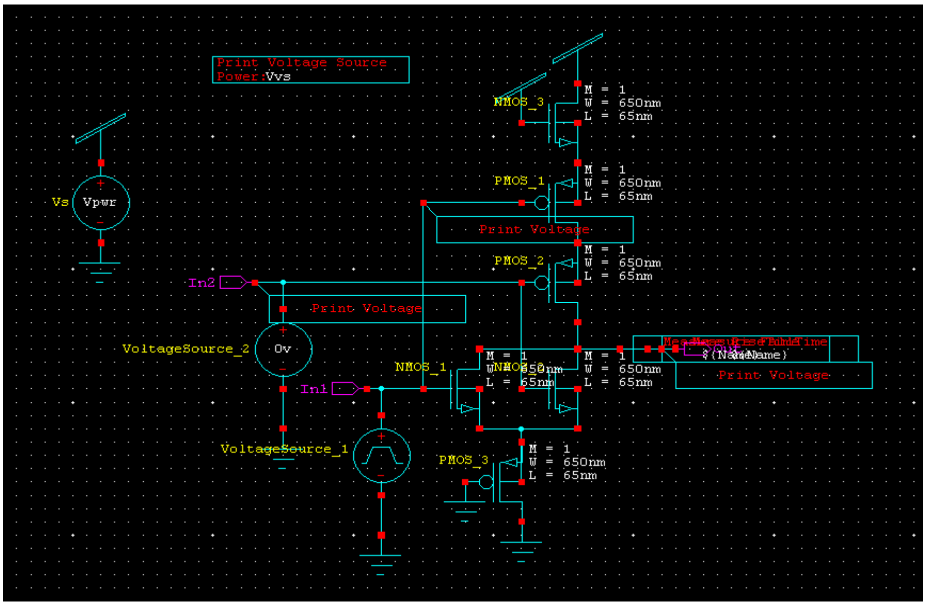


Fig 6: Novel Sleepy NOR Inverter for normal mode(Slp=0,slpb=1)

III. Results And Discussion

The circuit design is carried out using 65 nm CMOS NAND and NOR Gate technology files. All the designs are done and simulation is performed in Tanner design environment. The total (average) power dissipation is measured using Tanner tools. The power dissipation is measured both during active mode and standby mode of operations, for all the GATE and drivers and also considers the speed of all Gates in terms of rise time and fall time.

The simulation of Gate and driver circuits is performed by applying slp and slpb signals with 12nanosecond period and variable pulse widths. Active mode operation is observed by keeping these signals in the logic states. Long sleep (standby) period is also introduced to observe the performance during inactive period. The CMOS NAND and NOR Gate using sleepy, novel technique has exhibited lower leakage current and lower power. However during active mode lower output voltage is observed at correct functionality.

The average power dissipation during all operating modes is measured by using Tanner result browser and calculator. Table 1 and 2 compares the total power dissipation of all the NAND and NOR Gate during active mode i.e. when sleep control signals slp and slpb hold the respective sleep transistors in the on state and the logic inverter behaves as a normal NAND and NOR Gate.

TABLE 1.CMOS NAND Gate Total (Average) Power Dissipation (ACTIVE MODE):

S.No.	Inverter	Power (Watt.) O/P=0V(in:0,1)	Rise Time(s)	Fall Time(s)
1.	NAND Gate	3.214 E-6	1.859 E-10	1.584 E-10
2.	Sleepy NAND Gate (slp=1,slpb=0)	2.44 E-6	1.95 E-10	1.74 E-10
3.	Novel Sleepy NAND Gate (slp=0,slpb=1)	8.58 E-7	6.58 E-9	4.29 E-9

TABLE 2. CMOS NOR Gate Total (Average) Power Dissipation (Active Region):

S.No.	Inverter	Power (Watt.) O/P=0V(in:0,1)	Rise Time(s)	Fall Time(s)
1.	NOR Gate	3.15 E-6	1.92 E-10	1.92 E-10
2.	Sleepy NOR Gate (slp=1,slpb=0)	2.59 E-6	2.32 E-10	2.05 E-10
3.	Novel Sleepy NOR Gate (slp=0,slpb=1)	9.21 E-7	6.47 E-9	4.75 E-9

TABLE 3. CMOS NAND Gate Total (Average) Power Dissipation (SLEEP MODE):

S.No	GATE	Power (Watt.) O/P		Rise Time(s)	Fall Time(s)
		0V(in:1,1)	1V(in:1,0)		
1.	NAND Gate	4.78 E-8	3.60 E-8	N.A	N.A
2.	Sleepy NAND Gate (slp=0,slpb=1)	4.21 E-9	2.50 E-8	N.A	N.A
3.	Novel Sleepy NAND Gate (slp=1,slpb=0)	1.83 E-8	1.84 E-8	N.A	N.A

TABLE 4.CMOS NOR Gate Total (Average) Power Dissipation (SLEEP MODE):

S.No.	GATE	Power (Watt.) O/P		Rise Time(s)	Fall Time(s)
		0V(in:0,1)	1V(in:0,0)		
1.	NAND Gate	2.184 E-8	1.66 E-7	N.A	N.A
2.	Sleepy NAND Gate (slp=0,slpb=1)	4.00 E-9	1.546 E-8	N.A	N.A
3.	Novel Sleepy NAND Gate (slp=1,slpb=0)	1.844 E-8	1.88 E-8	N.A	N.A

Table 3 and 4 provides the total power dissipation during sleep mode of operation for all the NAND and NOR Gate.

The sleep signal slp is in the pull down path and sleep signal slpb is used in the pull up path. Depending upon whether PMOS or NMOS sleep transistor is driven, slp and slpb assume logic states to make them on or off. The logic values of these sleep signals for different modes of operation in case of different inverters are provided in the tables of observation.

IV. Conclusion

In this article we have simulated the circuit design using 65 nm CMOS NAND and NOR Gate technology files. All the designs are developed in Tanner design environment with the total (average) power dissipation measurement. The novel sleepy transistor based design provides very good reduction of leakage power but it shows low levels of output. This proposed method can be utilized in situations which do not have requirements of good voltage levels and the circuit remains standby (inactive) mode for most of its operation time. The leakage power during active and standby mode is found to be better for novel method compared to sleepy and sleepy inverts using NAND and NOR.

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