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International
Journal
Of Modern Engineering Research (IJMER)

High Performance Germanium Double Gate N-MOSFET

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ABSTRACT- *The current MOSFET technology supports scaling down to nanometer. To achieve enhanced transistor switching, it is difficult to keep the equivalent driver current at the same level since it changes by the certain restrictions like effective masses, density of states, uniaxial- and biaxial- strain; band structure, channel orientation, channel mobility, off-state leakage, switching delay in nano-scale and parasitic latch up. Current strained-Si is the ruling technology for intensifying the performance of MOSFET and development of strain can provide a better solution to the scaling. The future of nano-scale MOSFETs relies on exploration of novel higher mobility channel materials such as stained-Ge and strained III-V groups that might perform even better than very highly strained-Si. In addition, parameters such as injection velocity, short channel length effect and Band-to-Band Tunneling (BTBT) result in reduction of inversion charge, increase in leakage current, resulting in decrease in the drive current. While developing accurate model of MOSFETs all these complex effects should be captured. It is proposed to*

1. Design high performance double gate n-MOSFET with channel material Ge.

2. Benchmarked & stimulate high performance double gate n-MOSFET by using the simulation techniques.

Keywords- *Uniaxial strain, Strained Si, Strained Ge, Double-gate MOSFETs, Band To Band Tunneling.*

I. INTRODUCTION

The Si-based MOSFETs have been the most important building blocks of the Integrated Circuits (ICs), since they were first presented in 1960 *[1]*. Today's Integrated Circuits (ICs) use these MOSFETs as the basic switching element for digital logic applications and as an amplifier for analog applications. Even though the basic structure of the device has remained the same, the physical size has been continuously reduced by factor of two every 2-3 years using Moore's Law (fig.1) *[2]* which results in faster and highly complex chips with lowered cost per transistor *[2]*.

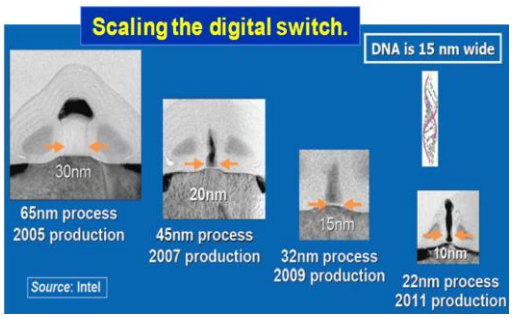

Fig.1: Scaling of bulk MOSFET using Moore's Law *[2]*.

This trend has been the main driving force for electronics industry for putting large energy and budget into scaling device technologies. Currently, in the 32nm high performance processor technology, the physical gate length is scaled below 20nm, with effective gate oxide thinner than 0.8 nm. This exponential scaling of the physical feature size cannot continue forever, as beyond the 22nm node fundamental as well as practical limitations start restricting the performance of the conventional Si-based MOSFETs. Taking into consideration fig.2, after the development of 90nm device technology, enhanced drive currents were achieved with an exponential increase in the static, off state leakage of the device *[1]*.

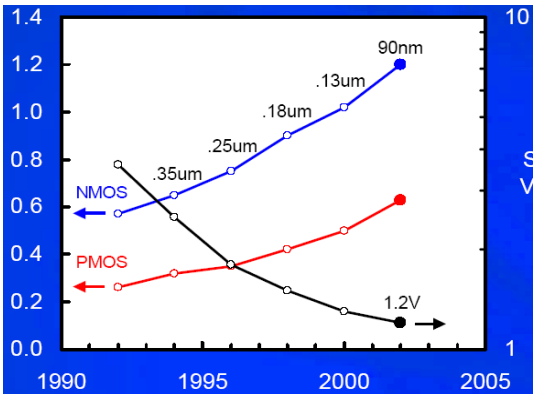

Fig.2: Need to maintain an increase in the drive current (Ion) even at reduced supply voltages (Vdd) in the future *[1]*.

Fig.3 defines the growth of static power dissipation (leakage) and active power dissipation as the devices are scaled down. The static power density on the chip has been exponentially increasing at the much faster rate than the active power density, which increases rather linearly with device scaling. The active power density arises due to the dissipative flow of charges between the transistor gates and ground terminals during switching of the device. The static power, also known as sub-threshold power, or standby power, is dissipated even though switching operation is absent. The major source of the static power dissipation is the sub-threshold leakage in the transistor since the MOSFET at below 50nm gate length scale does not behave as an ideal switch and allows the leakage current. The static power dissipation is relatively insignificant component of the total chip power just few generations back, but it is now comparable in magnitude to the active power.

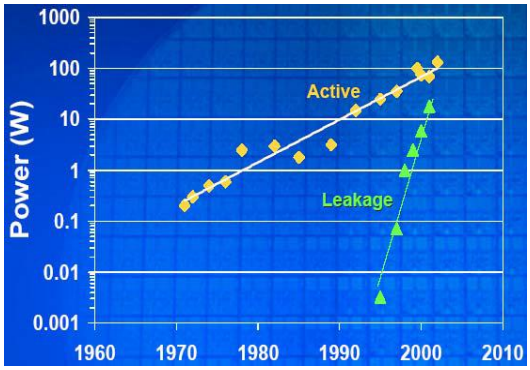

Fig.3: static power dissipation will cross the active power consumption (source: Intel) *[1]*.

When the scaling of the conventional bulk Si-MOSFET starts decreasing, it becomes necessary to insert performance boosters, such as novel materials and non-classical device structures, to enhance performance. In order to enhance the performance without sacrificing off state leakage power, strain technology was adopted to improve the drive current. Mechanically stressed Si has higher mobility than relaxed Si. However, for further scalability of the device, the materials with even higher mobility than strained Si are needed. The materials such as strained Ge, strained Si-Ge or even more futuristic carbon nanotubes and graphene have been actively investigated to study the possibility of substituting Si as a channel material in future as they exhibit 20 to 40 times larger mobility than Silicon, high mobility generally comes along with large dielectric constant and small band gap which are the basic properties of semiconductor materials which have weak bonding between atoms *[1]*.

II. MOTIVATION

Previous work laid stress on providing the explanation regarding the transport in uniaxial strained-Si MOSFETs through simple band structure and mobility calculations. However, as we scale down MOSFETs to very short channel lengths, the effect of the high-field transport, density of states (DOS), band structure, mobility and effective mass, in calculating the eventual drive current, we require expanded investigation *[3]*. Furthermore, strain modifies the band structure and changes the BTBT limited off-state leakage. Here in this work, the band structures are calculated using the non-local Empirical Pseudopotential method. Full-Band Monte-Carlo Simulations were used to evaluate the transport. 1-D Poisson-Schrodinger solver and detailed

BTBT simulations (including direct and indirect transitions) are used here to calculate the electrostatics and the off-state leakage. Then we will systematically compare and benchmark nano-scale (Ts=5nm, Lg=15nm) DG n-FETs, with different high mobility channel materials Si and Ge, in terms of their important performance metrics such as Drive Current, Intrinsic Delay and Off-state Leakage. Two standard channel directions, [100] and [110], on the (001) surface will be taken into consideration *[5]*.

III. UNIAXIAL STRAIN

We have considered uniaxially strained-Si and strained-Ge MOSFETs on a (001) wafer with channel direction in [100] and [110]. In addition, we have taken both tensile and compressive stresses from the –5GPa to +5GPa. Under this simulation study, we have extended our range of stress, however, it must be noted that for values of stress >3GPa, bulk materials are very close to their fracture point and may be impractical to achieve. The uniaxial stress was applied in the channel direction. Also we have considered that the channel direction is denoted 'x', the width direction 'y', and the direction perpendicular to the gate 'z' *[4]*.

IV. BAND STRUCTURE CALCULATION

The band structures are calculated using the non-local Empirical Pseudopotential method. Once we have the band structure of the material, complex movement of carriers in semiconductor can be simplified. The band structure of a semiconductor describes the range of energy and crystal momentum (k) whether an electron is "forbidden" or "allowed" to have. It is because of the diffraction of the quantum mechanical electron waves in the periodic crystal lattice. Also the band structure obtained in real 3-D crystal momentum (k) space gives us the information on carrier's density of states, quantum quantization effective mass, transport effective mass. The band structure also can be expanded in complex k space where k space is no longer real number rather complex number. Band information in complex k-pace provides information on the decaying states coupling two bands *[5]*.

The Principles of Pseudopotential can express the complete Hamiltonian for the periodic semiconductor structure as *[1]*

"Equation 1 is . . ."

$$\mathbf{H = H_{electrons} + H_{nuclei} + H_{nuclei\text{-}electron}}$$

where

"Equation 2 is . . ."

$$\mathbf{H_{electrons}} = \sum_{\mu}\left(-\frac{\hbar^2}{2m_o}\nabla_{\mu}^2 + \sum_{\lambda<\mu}\frac{e^2}{|\mathbf{r}_{\lambda}-\mathbf{r}_{\mu}|}\right)$$

where

$\mathbf{r}_{\lambda}$ is the position of the electron.

m_o is the mass.

"Equation 3 is . . ."

$$\mathbf{H_{nuclei}} = \sum_{v}\left(-\frac{\hbar^2}{2M_v}\nabla_v^2 + \sum_{\lambda<v}\frac{Z_{\lambda}Z_v e^2}{|\mathbf{R}_{\lambda}-\mathbf{R}_v|}\right)$$

where

$\mathbf{R}_v$ is the position.

Z_v is the atomic number.

M_v is the mass of the nuclei.

"Equation 4 is . . ."

$$\mathbf{H_{nuclei\text{-}electron}} =$$

$$-\sum_{\mu,v}\frac{Z_v e^2}{|\mathbf{R}_v-\mathbf{r}_\mu|}$$

There exists infinitely large numbers of electrons in a typical semiconductor, and hence it is almost impossible to track all these electrons. In addition, the strong Coulomb potential of the nucleus terms tend to go to negative infinity as an electron position gets close to the center of a nucleus, which needs very fine special gridding in numerical calculation of this system.

However, there are several approximations that allows one to achieve both acceptably accurate band structure and to reduce the computation complexity.

These are shown in fig.4 and includes *[1]*

1. Pseudopotential approximation under which, the electrons below the outer shell are tightly bound to the nucleus and the core states remain almost unchanged by interaction from electrons in outer shell (or valence bands).This permits us to replace the strong Coulomb potential of the nucleus and the effects of the tightly bound core electron by an effective ionic potential acting on the valence electrons.
2. The independent electron approximation replace the complicated electron-electron interactions with a time averaged potential.

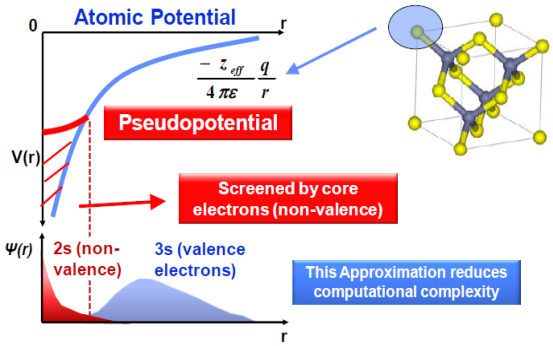

Fig.4: Pseudopotential approximation: The tightly bond inner electron shell can be effectively replaced by the pseudopotential *[1]*.

Thus, equation 4 can be expressed as

"Equation 5 is . . ."

H=

$$-\frac{\hbar^2}{2m_o}\nabla^2+V_c$$

where

V_C is crystal potential that includes the interaction between the electrons and the nuclei and the interaction between the electrons.

V. EFFECTIVE MASS, DOS AND BAND GAP CALCULATION

The effective masses are depicted in figs. 5 (a) and (b). For Si [100] the effective mass reduces slightly for both tensile and compressive in all directions. For Si [110], compressive stress rapidly reduces the mass in the transport direction (x) while greatly increases the mass in the width direction (y), leading to a high density of states. For Ge, compressive stress allows a rapid reduction in the transport mass and in the [110] direction it behaves similar to Si *[5]*.

This allows the simultaneous increase in the DOS. Also, the relative positions of all the different valleys for Ge [110] are shown in fig. 6. The decrease in the band gap for compressive uniaxial stress along [100] for Si is always the X-valley. For Ge [110] it is the L-valley but for Ge [100], the lowest valley shifts from L- to X- for large values of stress, due to the rapid reduction in the X-valley band gap. As seen in the fig. 6, for compressive stress in Ge [110], the valley Γ - band gap increases, while for tensile it sharply reduces.

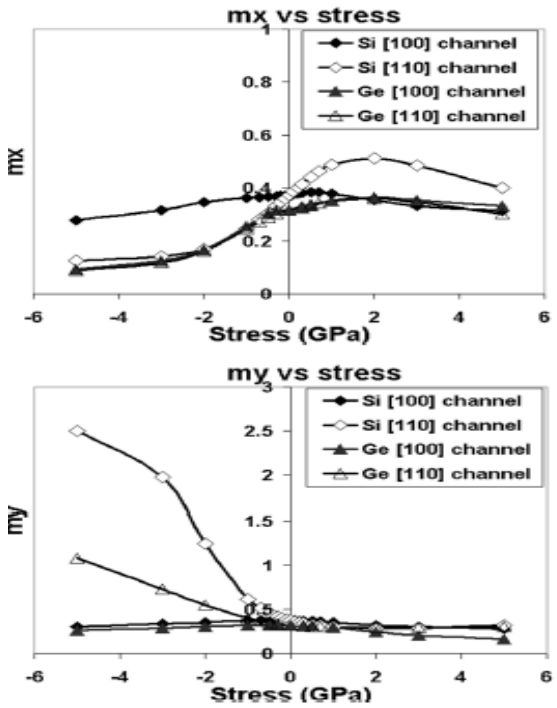

Fig.5 (a) and (b): The effective mass for Si and Ge as a the function of uniaxial strain *[5]*.

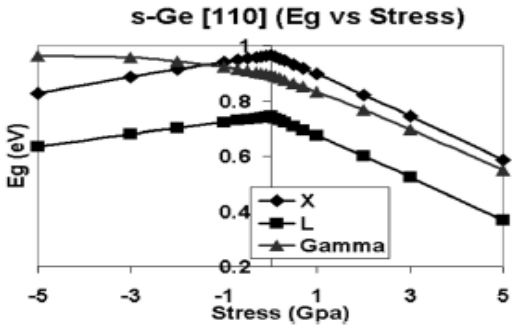

Fig.6: The lowest valley for Ge [110] is always L- and the band gap is relatively large even for large [110] uniaxial stress *[5]*.

VI. LOW-FIELD MOBILITY AND VELOCITY-FIELD CURVES CALCULATION

For a 2-D hole inversion carrier concentration of 1.8x10 ^{13}cm^{-2}, the effective, low driving field mobility in the channel transport direction is shown in fig.7. The mobility for compressively strained [110] strained-Ge is the highest in the channel direction, because of its lower mass and lifting of the band degeneracy. The mobility is ~6 times larger than for the relaxed-Ge and ~2 times larger than for [110] strained-Si. Thus mobility can be increased to ~12 times for strained-Ge [110], ~6 times for strained-Si [110] and ~2 times for relaxed-Ge, in comparison to the relaxed-Si *[5]*.

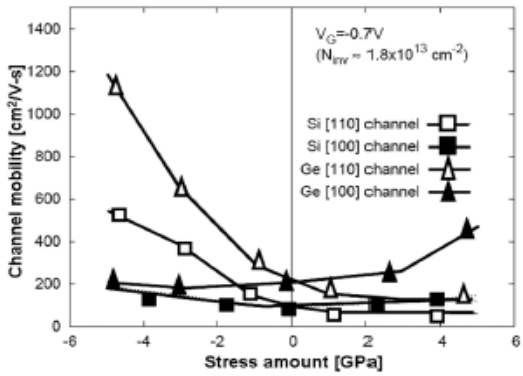

Fig.7: Low-field mobility vs uniaxial stress for Si and Ge *[5]*.

The bulk velocity-field curves for Si and Ge under uniaxial strain are depicted in figs. 8 (a), (b) and (c) (relaxed, compressive and tensile stress). The bulk velocities for compressive Si [110], and Ge [110] are extremely large and exhibit stationary velocity overshoot under bulk conditions. Si [110] shows an increase of ~50%, and Ge [110] exhibits an increase of ~40%, in comparison to their relaxed unstrained cases respectively.

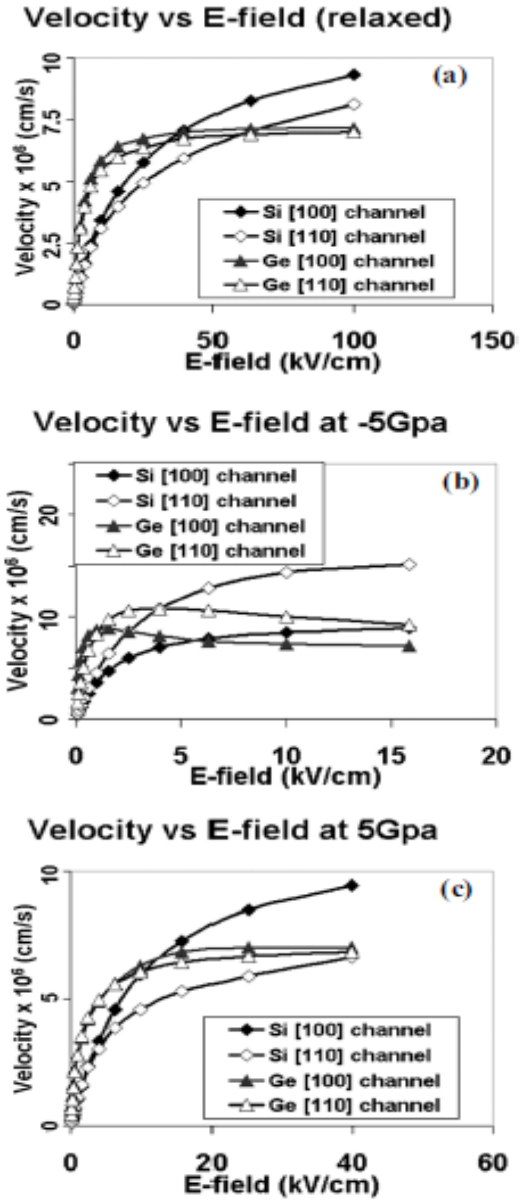

Fig.8 (a), (b) and (c): Velocity-field curves for the uniaxially strained Si and Ge in comparison to relaxed substrates *[5]*.

VII. DRIVE CURRENT, DELAY AND OFF-STATE LEAKAGE CALCULATION

On studying fig.9, we find the large increase in the bulk velocity at high driving fields, in compressive Si [110], which leads to high drive currents. The higher mobility of compressively strained Ge [110] and the enhanced high driving field bulk velocity leads to a very high drive current, which is the highest among all the channels taken. The minimum off-state leakage in compressively strained-Ge [110] is an order of magnitude lower than in strained-Ge [100] due to the larger L- and Γ -valley band gaps (Fig. 10). Si [110] shows the lowest leakage, (100 times lower than Ge), because of its large indirect X-valley band gap *[5]*.

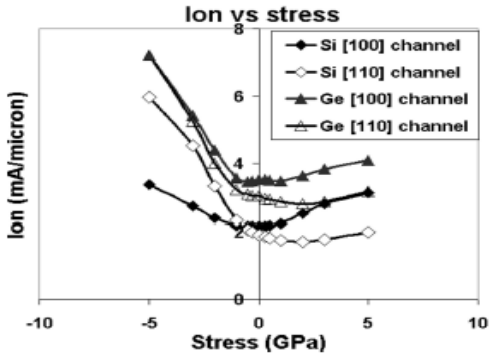

Fig. 9: The drive current for Ge [100] and Ge[110] under uniaxial compressive stress *[5]*.

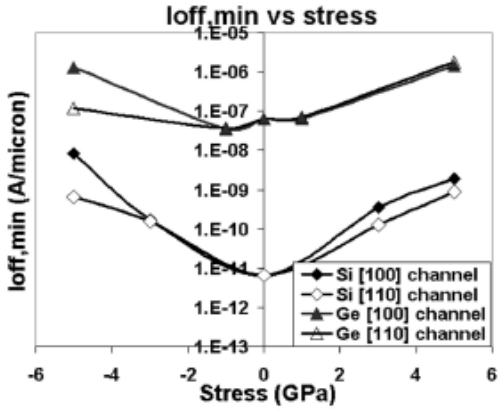

Fig.10: The minimum achievable off-state leakage under compressive stress *[5]*.

VIII. CONCLUSION

The parameters such as strain, channel orientation, band structure, DOS, effective mass, band gap, mobility and velocity helps us in calculating the performance n-MOSFETs. For the lower values of the uniaxial stress, compressively strained-Ge gives us the best performance in terms of the drive current, the delay reduction (~2 times in comparison to relaxed-Si). Although, the minimum off-state leakage because of BTBT is rather high (100nA/μm).

For the larger values of uniaxial strain, mainly because of the large increase in the bulk velocity at high driving fields, the anisotropic effective mass and large band gap, Si [110] strained compressively to >-3GPa gives the best performance the in terms of the drive current ,delay reduction (~3 times) and very low off-state leakage (<1nA/μm). However, it should be keep in mind that the values of stress > +3GPa for bulk materials is very closer to their fracture point and may be impractical to achieve.

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