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Simulation and Analysis of 2:1 Multiplexer Circuits at 90nm Technology

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ABSTRACT

A multiplexer, sometimes referred to as a "MUX", is a device that selects between a numbers of input signals. It is a unidirectional device and used in any application in which data must be switched from multiple sources to a destination. This paper represents the simulation of different 2:1 MUX configurations and their comparative analysis on different parameters such as Power Supply Voltage, Operating Frequency, Temperature, Load Capacitance and Area Efficiency etc. All the simulations have been carried out on BSIM 3V3 90nm technology at Tanner EDA tool.

Keywords – CMOS Logic, Low power, 2:1 Multiplexer and VLSI.

I. INTRODUCTION

Low power has emerged as a principal theme in today's electronics industry. The need for low power has caused a major paradigm shift where power dissipation has become as important a consideration as performance and area. A 2:1 multiplexer is a basic building block of the "switch logic". The concept of the switch logic is that logic circuits are implemented as combination of switches, rather than logic gate. Multiplexers are used in building digital semiconductors such as CPUs and graphics controller, as programmable logic devices, in telecommunications, in computer networks and digital video. This paper compares the different 2:1 multiplexer circuits on the basis of the power dissipation, speed, operating frequency range and their temperature dependence with the area efficiency of the circuit.

II. LITERATURE REVIEW OF DIFFERENT 2:1 MULTIPLEXER CIRCUITS

2.1 NMOS MULTIPLEXER CIRCUIT

The schematic diagram of NMOS 2:1 MUX is shown in Fig.1. The technique is based on Complementary Pass Transistor Logic. It reduces the count of transistors used to make different logic gates, by eliminating redundant transistors [1]. Transistors are used as switches to pass logic levels between nodes of a circuit, instead of as switches connected directly to supply voltages. This reduces thenumber of active devices, but has the disadvantage that output levels can be no higher than the input level [2].

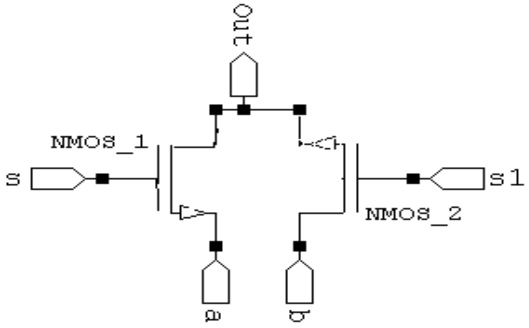

Fig. 1 Schematic of NMOS 2:1 Multiplexer

2.2 CMOS MULTIPLEXER CIRCUIT

Fig. 2 is depicting the circuit diagram of CMOS 2:1 multiplexer based Double Pass Transistor Logic. DPL eliminates some of the inverter stages required for complementary pass transistor logic by using both N and P channel transistors, with dual logic paths for every function. While it has high speed due to low input capacitance, it has only limited capacity to drive a load [2].

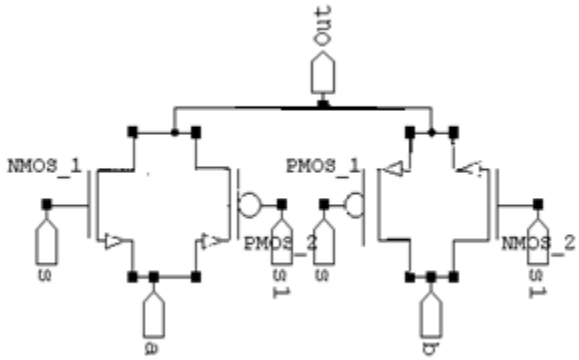

Fig. 2 Schematic of CMOS 2:1 Multiplexer

2.3 MSL MULTIPLEXER CIRCUIT

MSL stands for multiplexer single with level restoration block which is shown in Fig.3. One problem with the CPL or DPL circuits is the requirement of both non-inverting and inverting signals, which leads to a large wiring area [2]. So a new logic design based on CPL like circuits called MSL

arises, which uses only the non-inverting output of the original CPL multiplexer circuit appended by a p-latch inverter which is the heart of this circuit [3].

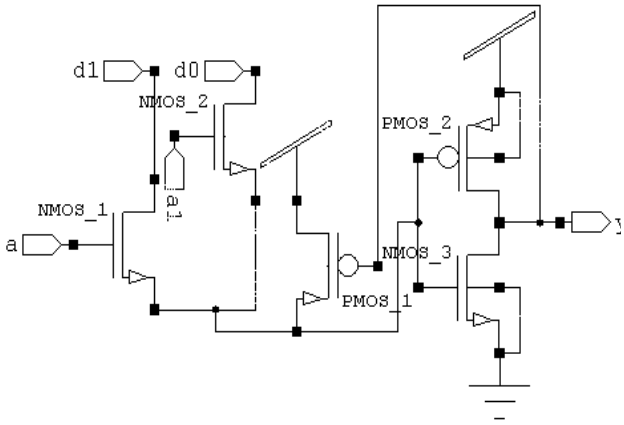

Fig. 3 Schematic of MSL circuit

2.4 MD MULTIPLEXER CIRCUIT

Schematic of MD circuit is shown in the Fig. 4. MD stands for multiplexer double. With the help of this circuit we find the inverted output also [3].

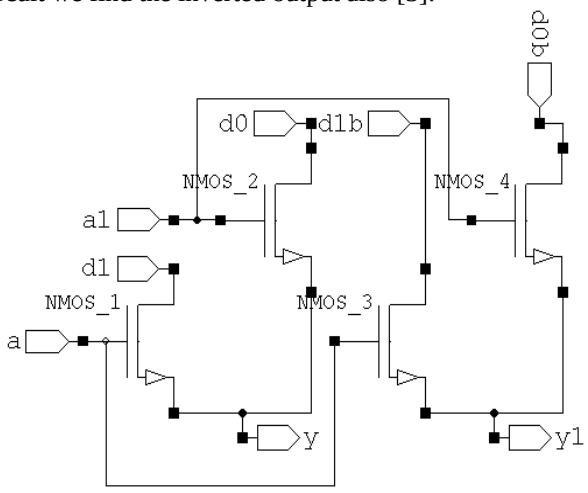

Fig. 4 Schematic of MD circuit

2.5 MDL MULTIPLEXER CIRCUIT

Schematic of MDL Based circuit is shown in the Fig.5.

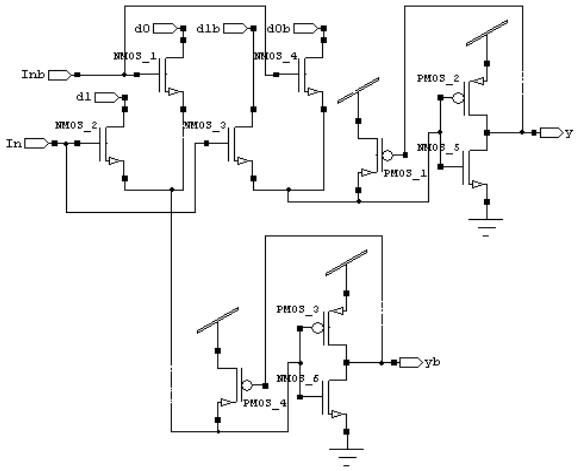

Fig. 5 Schematic of MDL circuit

MDL stands for multiplexer double with level restoration block. With the help of this level restoration block we can avoid swing problems, but it has high-area and high-power drawbacks. [3]

2.6 DCVSL MULTIPLEXER CIRCUIT

Schematic of DCVSL circuit is shown in the Fig. 6. Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family which is designed for certain advantages. A logic function and its inverse are automatically implemented in this logic style. The pull-down network implemented by the NMOS logic tree generated complementary output. This logic family is also known as Differential Cascode Voltage Switch Logic (DCVS or DCVSL).The advantage of DCVSL is in its logic density that is achieved by elimination of large PFETS from each logic function. It can be divided it to two basic parts: a differential latching circuit and a cascaded complementary logic array [4], [5], [6].

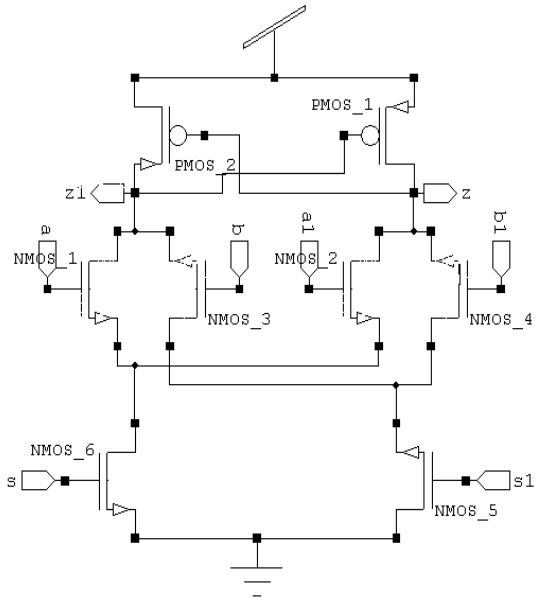

Fig. 6 Schematic of DCVSL circuit

2.7 MDCVSL MULTIPLEXER CIRCUIT

Schematic of MDCVSL circuit is shown in the Fig. 7.

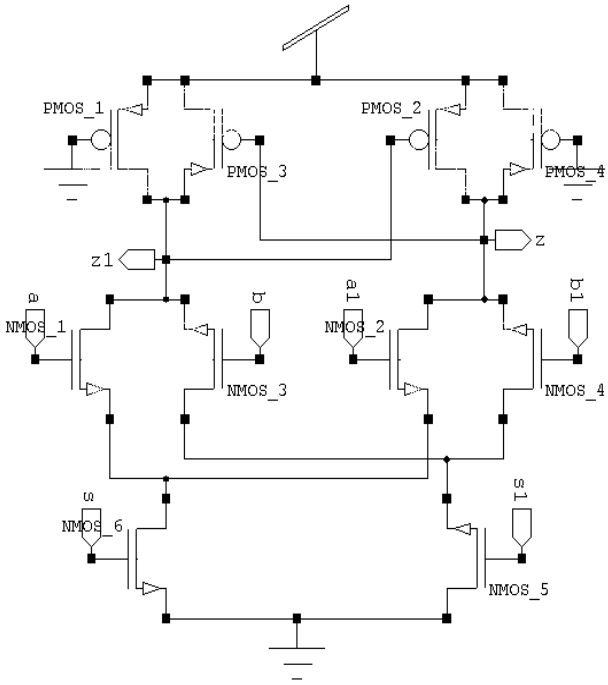

Fig. 7 Schematic of MDCVSL circuit

III. SIMULATION AND ANALYSIS

3.1 SIMULATION ENVIRONMENT

All the circuits have been simulated using BSIM 3V3 90 nm technologies on Tanner EDA tool. To make the impartial testing environment all the circuits has been simulated on the same input patterns. All the simulations have been done on room temperature.

3.2 SIMULATION ANALYSIS

Fig. 8 and Fig. 9 are depicting the power consumption vs. Vdd for different 2:1 multiplexer circuits. MDCVSL circuit shows the least power consumption over other approaches. Fig. 10, Fig. 11 and Fig. 12 shows delay vs. Vdd for 2:1 multiplexer circuits. The MDCVSL circuit shows least delay among all the other design techniques. Fig.13 and Fig.14 shows Power Consumption Vs operating frequency in which up to the range 200 MHz, NMOS circuit showing better result. Fig. 15, Fig. 16, Fig. 17 and Fig. 18 shows power consumption vs. operating temperature and output load capacitance respectively. All these figures depicts shows MDCVSL circuit shows always best performance for the range of operating temperature and output load capacitance among all the other design approaches for different 2:1 multiplexers circuit approaches.

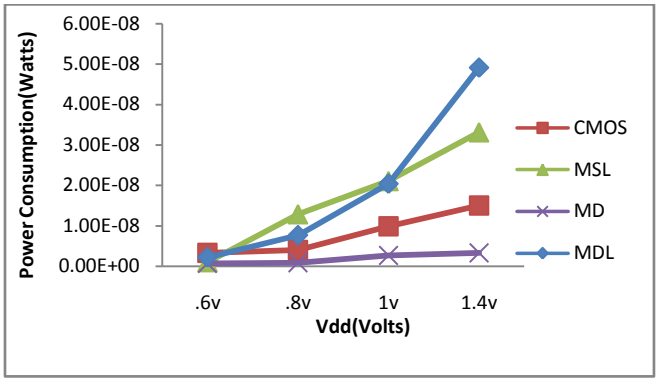

Fig. 8 Power Consumption Vs Vdd for CMOS, MSL,MD & MDL based Multiplexers Circuits.

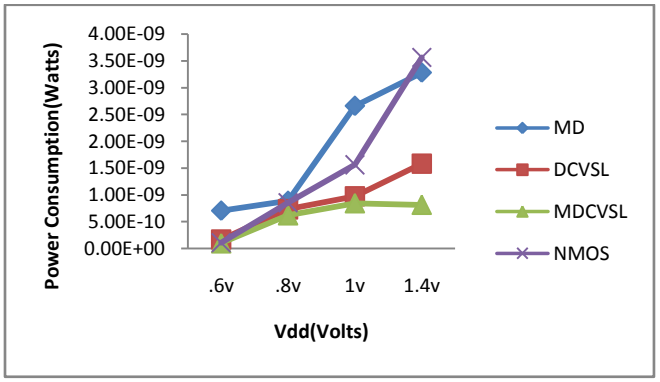

Fig. 9 Power Consumption Vs Vdd for MD, DCVSL, MDCVSL & NMOS based Multiplexers Circuits.

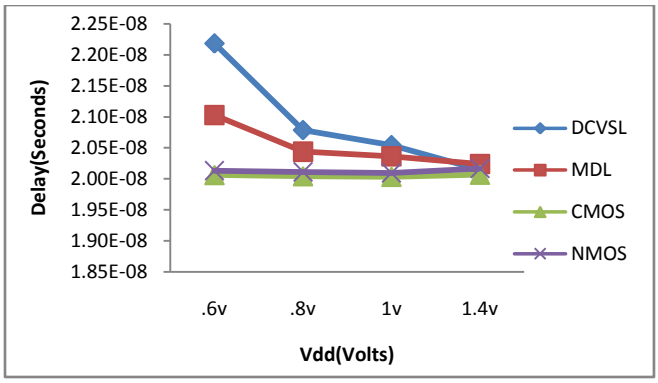

Fig. 10 Delay Vs Vdd for DCVSL,MDL, CMOS & NMOS based Multiplexers Circuits.

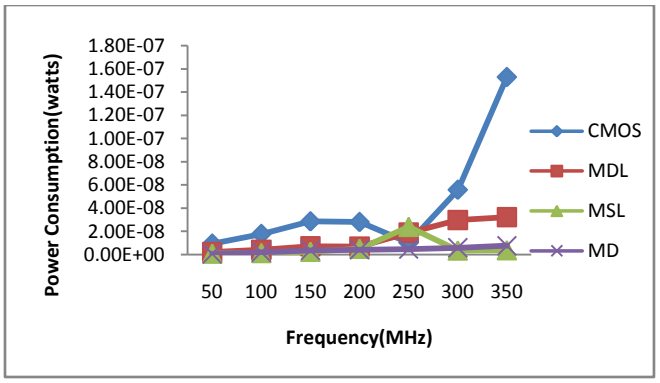

Fig. 13 Power Consumption Vs Operating Frequency for CMOS,MDL, MSL & MD based Multiplexers Circuits.

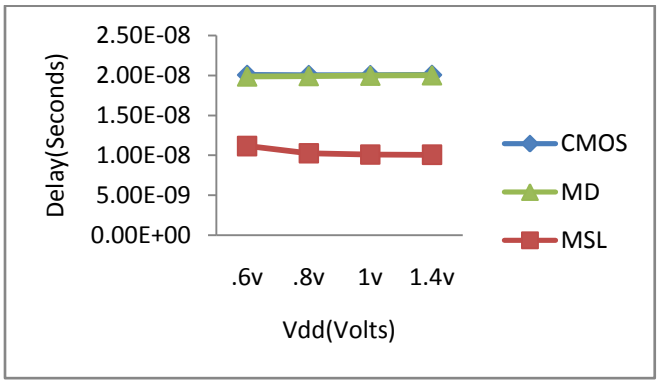

Fig. 11 Delay Vs Vdd for CMOS, MSL & MD based Multiplexers Circuits.

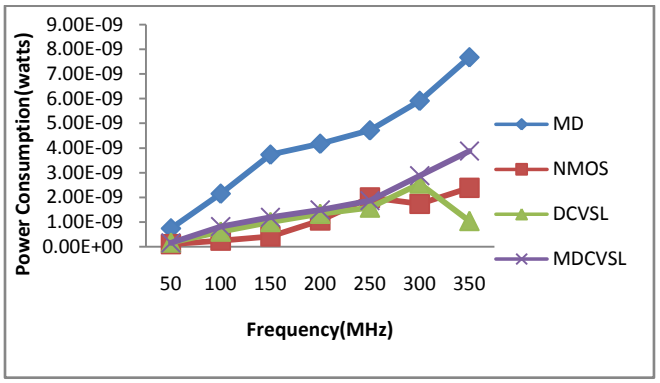

Fig. 14 Power Consumption Vs Operating Frequency for MD, NMOS, DCVSL & MDCVSL based Multiplexers Circuits.

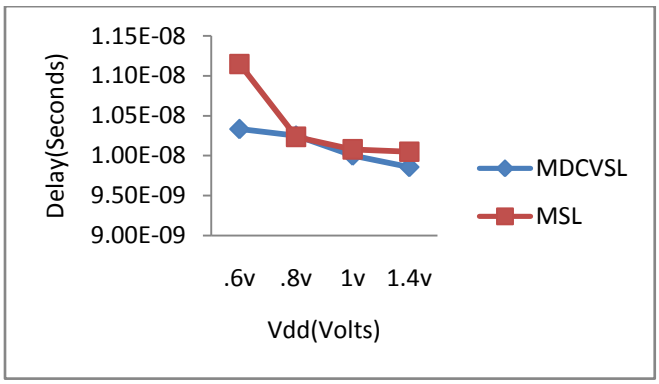

Fig. 12 Delay Vs Vdd for MDCVSL & MSL based Multiplexers Circuits.

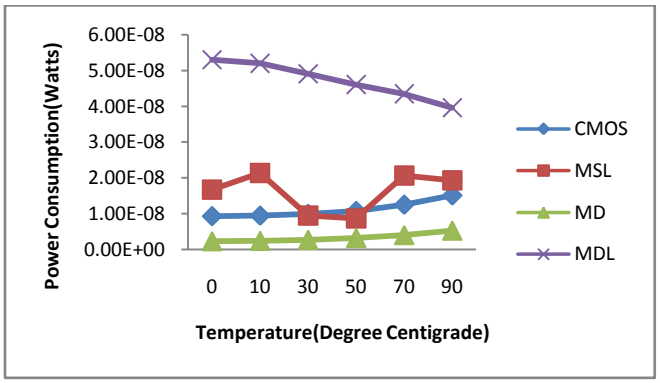

Fig. 15 Power Consumption Vs Operating Temperature for CMOS, MSL, MD & MDL based Multiplexers Circuits.

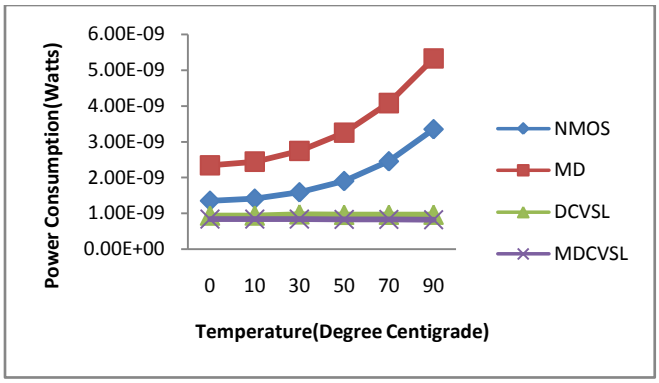

Fig. 16 Power Consumption Vs Operating Temperature for NMOS, MD, DCVSL & MDCVSL based Multiplexers Circuits.

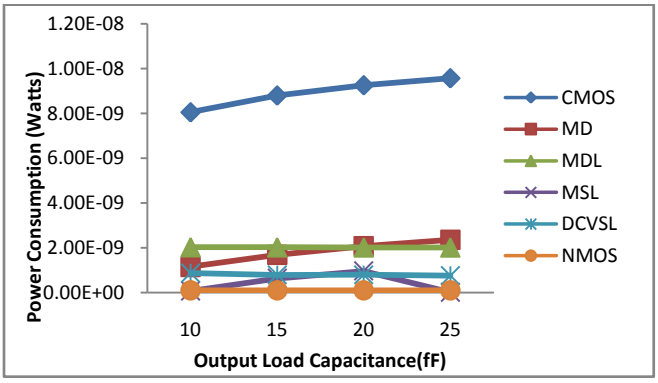

Fig. 17 Power Consumption Vs Output Load Capacitance for CMOS, MD, MDL, MSL, DCVSL & NMOS based Multiplexers Circuits.

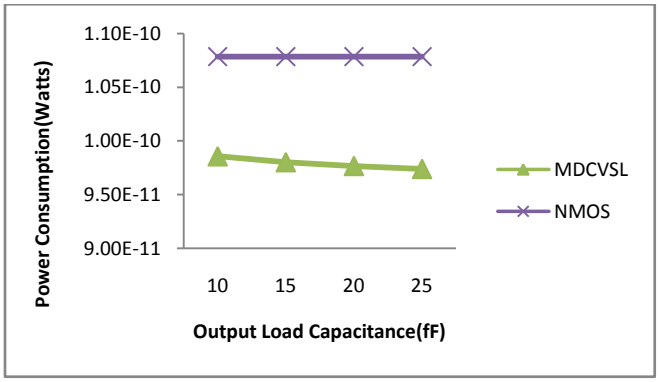

Fig. 18 Power Consumption Vs Output Load Capacitance for MDCVSL & NMOS based Multiplexers Circuits.

TABLE 1 depicts the Power Delay Product over a range of Power Supply voltages and as it is shown in the table that MDCVSL circuit for 2:1 multiplexer shows minimum Power Delay Product.

TABLE 1: Power Delay Product Comparison of different 2:1 Multiplexer Circuits

Different 2:1 Mux circuits	Power Delay Product (Watt-sec)			
	V_{dd}=.6v	V_{dd}=.8v	V_{dd}=1v	V_{dd}=1.4v
NMOS	2.17E-18	1.71E-17	3.13E-17	7.18E-17
CMOS	6.54E-17	7.94E-17	1.96E-16	3.00E-16
MSL	1.08E-17	1.31E-16	2.12E-16	3.32E-16
MD	1.39E-17	1.76E-17	5.30E-17	6.56E-17
MDL	4.61E-17	1.57E-16	4.15E-16	9.94E-16
DCVSL	3.70E-18	1.52E-17	2.00E-17	3.18E-17
MDCVSL	**1.94E-18**	**1.22E-17**	**1.66E-17**	**1.61E-17**

IV. CONCLUSION

The limited battery lifetime typically impose very strict demand on the overall power consumption of the portable system. A very common application of multiplexer is found in computers, where dynamic memory uses the same address lines for both row and column addressing. A set of multiplexers is used to first select the row address to the memory, then switch to the column. For low-leakage and high-speed circuits concern should be on both the factors speed and power. This paper tries to find out the solution for 2:1 Multiplexer in both the aspects power consumption and speed or in terms of power delay product. Modified differential cascade voltage switch logic (MDCVSL) shows least power consumption over a range of power supply voltage, output load capacitance, delay and operating temperature. NMOS circuit showing better result over operating frequency up to the range 200 MHz MDCVSL circuit shows the least power delay product over a range of supply voltages.

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