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Design Methodology of Current Buffer based Two Stage CMOS Op-Amp with Compensation Strategy

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Abstract
High Bandwidth Operational Amplifiers are needed for many applications. The Design methodology with current buffer overcomes the drawbacks in design strategies of nulling resistor and voltage buffer. The approach here provides improved gain bandwidth product and a gain of 42 dB on 0.5µm technology when operated on a supply voltage of 2.5 volts.

Keywords—CMOS analog integrated circuits, Current Buffer, Common Source Stage, Compensation Capacitor, Op-Amp.

Introduction
Operational amplifiers are amplifiers (controlled sources) that have sufficiently high forward gain so that when negative feedback is applied, the closed-loop transfer function is practically independent of the gain of the op-amp. Most of the amplifiers do not have a large enough gain. Consequently, most CMOS op-amps use two or more gain stages [1]-[3].

The goal of compensation is to maintain stability when negative feedback is applied around the op-amp.

I. Op-Amp Gain
Figure below shows block diagram of a two stage op-amp.

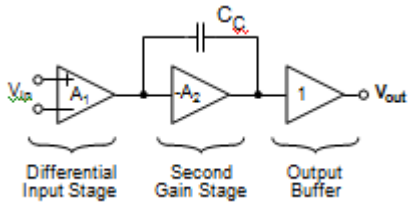

Fig 1 A Two stage Op-amp block Diagram.

First stage differential-to-single ended gain is given by

$$A_{v1} = g_{m1}(r_{ds2} \| r_{ds4}) \quad (1)$$

where
Second stage gain is given by

$$A_{v2} = -g_{m7}(r_{ds6} \| r_{ds7}) \quad (2)$$

Third stage is a source-follower and is only included if resistive loads need to be driven. If the load is purely capacitive in the case of integrated op-amps this stage is seldom included

$$A_{v3} \cong \frac{g_{m8}}{G_L + g_{m8} + g_{ds8} + g_{ds9}} \quad (3)$$

Where G_L is the load conductance being driven by the buffer stage.

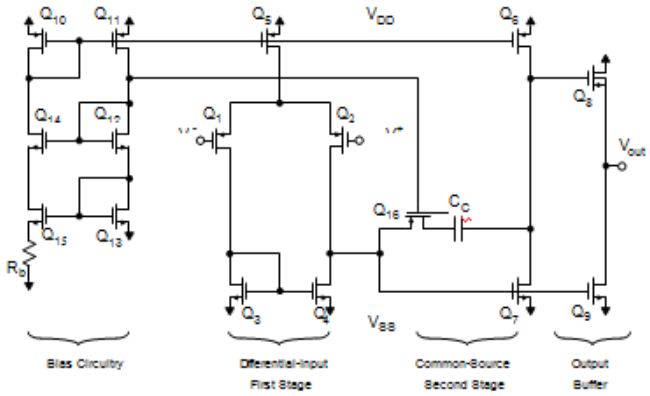

Fig 2 A Two stage Op-amp with second common source stage.

II. Compensation Procedure
Compensation procedure followed is:

a) Start by choosing C_c=5pF arbitrarily.
b) Using SPICE find the frequency where there is a 125° phase shift. Let the gain at this frequency be denoted A'. Also let the frequency be denoted ω_t. This is the frequency that we would like to become the unity-gain frequency of the loop gain[3].
c) Choose a new C_c so that ω_t becomes the unity-gain Frequency of the loop-gain, thus resulting in a 55° phase-margin (and the reason for the choice of 125° used above).This can be achieved by taking C_c according to the equation.
$C_C = C_c' A'$ (4)
It might be necessary to iterate on C_c a couple of times using SPICE.
d) Choose R_C according to

$$R_c = \frac{1}{1.2\,\omega_t} \quad (5)$$

This choice will increase the unity-gain frequency by about 20%, leaving the zero near to the final resulting unity-gain frequency, which will end up about 15% below the equivalent second pole frequency. The resulting phase margin is approximately –85°. This allows a margin of 5° to account for processing variations without the poles of the closed-loop response becoming real. This choice is also near optimum lead-compensation for almost any Opamp when a resistor is placed in series with the compensation capacitor. It might be necessary to iterate on a couple of times to optimize the phase-margin. However, it should be checked that the gain continues to steadily decrease at frequencies above the new unity-gain frequency, otherwise the transient response can be poor.
This situation sometimes occurs when unexpected zeros at frequencies only slightly greater than are present[1]-[3].

e) If after d), the phase-margin is not adequate, then increase C_C while leaving R_C constant. This will move both ω_t and the lead-zero to lower frequencies, while keeping their ratio approximately constant, thus minimizing the effects of higher frequency poles and zeros which, hopefully, do not also move to lower frequencies.

In most cases, the higher-frequency poles and zeros (except for the lead zero) will not move to significantly-lower frequencies when increasing.

TABLE I
Robust Bias OpAmp Design Procedure [4]

Step 1	$C_C = \frac{16kT}{3\omega_u S_n(f)}\left[1+\frac{SR}{\omega_u(V_{HR}^{CM+}+V_{tn})}\right]$
Step 2	$I_{D7}= SR(C_C+C_L)$
Step 3	$L_6 = \sqrt{\frac{3\mu_p V_{HR}^{out+} C_C}{2\omega_u C_L \tan\phi_M}}$
Step 4	$W_6 = \frac{2SR(C_C+C_L)}{\mu_p C_{OX}\left(V_{HR}^{out+}\right)^2} L_6$
Step 5	$I_{D5}= C_C SR$
Step 6	$(W/L)_{1,2} = \frac{\omega_u^2 C_C}{\mu_n C_{OX} SR}$
Step 7	$(W/L)_{5,8} = \frac{2SRC_C}{\mu_n C_{OX}\left(V_{HR}^{CM-}-V_{tn}-SR/\omega_u\right)^2}$
Step 8	$(W/L)_7 = \left(\frac{C_C+C_L}{C_C}\right)(W/L)_{5,8}$
Step 9	$(W/L)_{3,4} = \frac{(W/L)_6}{2(W/L)_7}(W/L)_{5,8}$
Step 10	$I_{D9} = \frac{(\tan\phi_M \omega_u C_L)^2\left(C_C+\frac{2}{3}W_9 L_9 C_{OX}\right)^2}{2\mu_n C_{OX}(W_9/L_9)}$

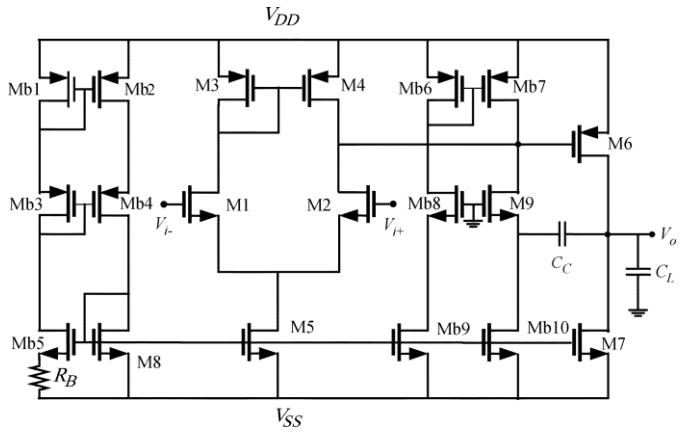

Fig. 3 Opamp with robust bias circuit

TABLE II
Design Parameters For Robust Bias Op Amp

$(W/L)_{1,2}$	.7µm/1µm
$(W/L)_{3,4}$	1.8µm/1µm
$(W/L)_{5,8}$	1.6µm/1µm
$(W/L)_{6}$	38.6µm/1µm
$(W/L)_{7}$	17µm/1µm
$(W/L)_{9}$	27µm/1µm
$(W/L)_{b1-b4}$	1.6µm/1µm
$(W/L)_{b5}$	6.4µm/1µm
$(W/L)_{b6-b7}$	131µ/1µm
$(W/L)_{b8}$	27µm/1µm
$(W/L)_{b9-b10}$	7.4µm/1µm
R_b	32K
C_c	0.5pF

TABLE III
Simulation Results

Opamp with Common Source Stage	Opamp with Current Buffer
GAIN in db	
62	42

III. CONCLUSIONS

Compared to the procedure based upon the nullifying resistor compensation the value of C_C of the proposed procedure [4] can be made much smaller. The wider range of the allowable value of C_C provides a higher flexibility for noise-power tradeoff.

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