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A NEW CIRCUIT TOPOLOGY FOR OPEN CIRCUIT AND SHORT CIRCUIT FAULT TOLERANT DC-DC CONVERTER

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ABSTRACT
This paper describes a new design for a fault tolerant H-bridge dc-dc converter. Open circuit and short circuit fault tolerance is achieved using multilevel converter topology in combination with pulse width modulation control strategy allowing a large set of converter switching states to produce bidirectional power flows at any required output voltage. If two switches fail at particular instant then also fault tolerant can be achieved. Fault tolerant ability of proposed converter to recover the required output voltage is verified by computer simulation using MATLAB/SIMULINK with 1kw resistive load.

***Keywords*-** DC-**DC power conversion, fault tolerant, multilevel system**.

I. INTRODUCTION
DC-DC converters are commonly used in wide variety of applications, including a number of critical applications in which very high levels of reliability are required because the loss of converter operation can have serious consequences. For example, control of car is lost when the supply voltage for a brake-by-wire system has collapsed due to converter failure. Another critical application is the use of dc-dc converter in low-power refrigeration application developed for use in an ambulance to maintain saline temperature within a specific range for immediate injection into a patient [1]. In such an application, the loss of control of the converter voltage can lead to a temperature difference of several degrees and serious medical complications.

In order to achieve highly reliable dc-dc conversion systems, N+M redundancy concepts have been proposed in the past [2], [3]. This is costly option in which one or more additional dc-dc converters are connected in parallel to achieve the required levels of redundancy in case of failure of the main converter. More recently, it has been shown that multilevel dc-ac converter topologies can be operated as fault tolerant circuits [4]-[6]. Multilevel dc-dc converters with multiple dc sources and no magnetic storage components have been proposed recently to achieve variable dc output voltage operation [7]. Initial investigations of the multilevel concept as applied to dc-dc converters for fault tolerant applications have also been presented [8]-[10]. Khan et al., for example, described a pseudo fault tolerant modular multilevel dc-dc converter [9], which could continue to operate in the event of a short circuit fault in any of the series connected modules the circuit however, could not operate successfully if one of its power devices had experienced an open circuit fault, as recognized by the authors.

Ceglia et al. [11] developed a circuit in that circuit, as proposed by Ceglia et al., suffers from a number of potential problems and drawbacks when operated as a dc-dc converters including high operational losses and long term reliability problems, as some of the switches are required to conduct permanently. In this paper, a new pulse width modulation (PWM) control strategy is developed and applied to modified circuit topology, in which the original converter is extended by the addition of an extra switching leg and bidirectional selector switches, to overcome these problems. If fault occur in an extra switching leg and also in the converter switches we can add one more leg to overcome these problems. In this paper the proposed convert has two auxiliary legs and selector cells so it can be called as HBALSC (H-bridge with auxiliary leg and selector cells).

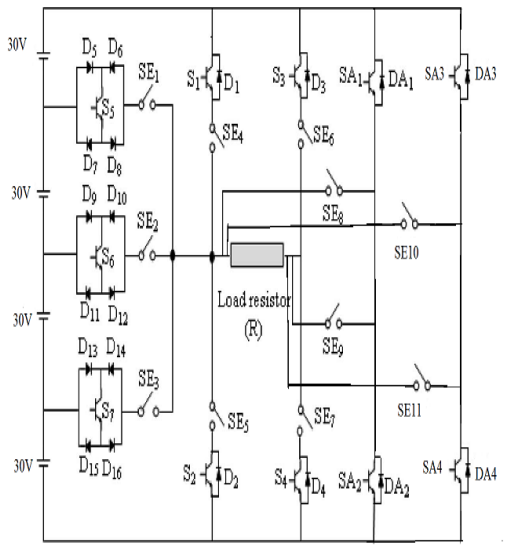

Fig.1.power circuit of the multilevel dc-dc converter

Fig. I shows the proposed H-bridge with two auxiliary leg and selector cells fault tolerant multi level dc-dc converter. The main H-bridge power circuit i.e., power devices S1-S4 and diodes D1-D4 is extended by four auxiliary switches (SA1/DA1, SA2/DA2, SA3/DA3 and SA4/DA4), three selector cells (power devices S5-S7, diodes D5-D16 and bidirectional switches SE1-SE3) and six additional bidirectional switches SE4-SE9 to form the multi level topology. Fault tolerant operation is achieved by using different switching states and controlling the PWM duty cycles of the individual switches to produce the required average output voltage with the minimum number of switches and power diodes.

The paper examines different fault scenarios to demonstrate the full fault tolerant capacity of the proposed converter. Different combinations of switching states and duty cycles are evaluated. The variety of switching combinations and PWM duty cycles provide fault tolerant operation.

II. PROPOSED CONVERTER

The operation of the H-bridge, dc-dc converter with resistive load under normal operating conditions is described in this section.

TABLE I
SWITCHING STATES FOR EACH VOLTAGE LEVEL:

Voltage levels	Current paths
30v	D13, S7, D16, SE3, SE7, S4.
60v	D9, S6, D12, SE2, SE7, S4.
90v	D5,S5,D8,SE1,SE7,S4
120v	S1, SE4, SE7, S4.
0v	SE5, S2, SE7, S4.
-30v	S3, SE6, SE1, D6, S5, D7.
-60v	S3, SE6, SE2, D10, S6, D11.
-90v	S3, SE6, SE3, D14, S7, D15.
-120v	S3, SE6, SE5, S2.

The proposed converter allows bidirectional power flow and depending on the switching states used, can produce nine different output voltage levels (-120, -90, -60, -30, 0, 30, 60, 90, 120V) when operating without PWM control, as shown in Table I. The application of PWM control allows operation at any required average voltage between -120V and +120V. It should be noted here, that the circuit cannot achieve the redundancy needed for fault tolerant operation by varying the switching states alone, each voltage level can be generated by only one switching combination as shown in Table I. The current path for the conduction state corresponding to an output voltage of 30V is shown in Fig. 2 as an example.

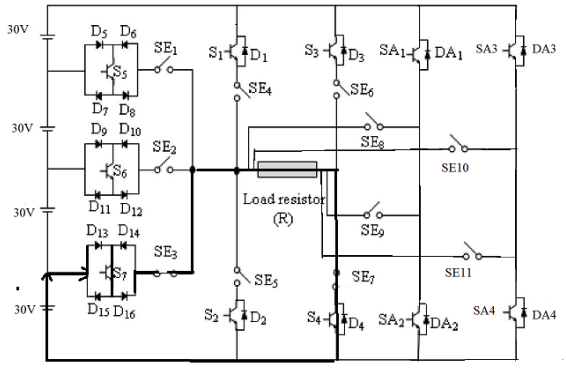

Fig.2. current path for conduction state corresponding to 30v output voltage.

In the following analysis, only forward power flow switch combinations will be considered i.e., no negative voltage switching states will be considered.

Fig.3 shows four output voltage levels V_{Ln} with PWM control at a fixed duty cycle D and a constant switching frequency. Assuming each voltage level is applied for an equal time T/4, the average output voltage V_o can be calculated from

$$V_o = \frac{D}{M}\sum_{N=1}^{M} V_{Ln} \qquad (1)$$

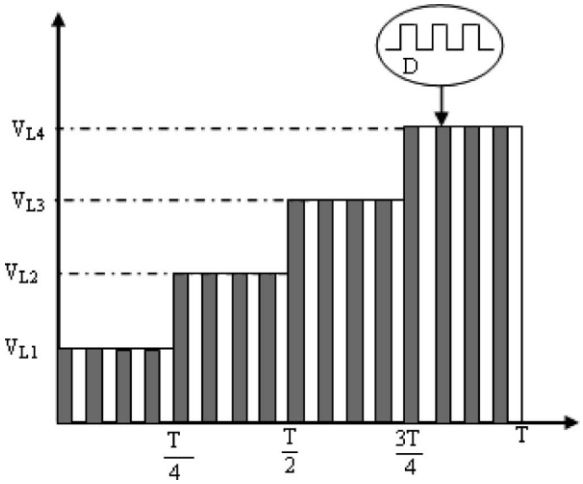

Fig. 3. Output voltage levels.

Where *D* is the duty cycle, *m* is the number of voltage levels and V_{Ln} is the output voltage associated with level *n*.

Equation (1) shows that the different switching states can produce a large number of possible output voltages when combined with all the possible values of converter duty cycles *D*. For example, Table II shows five possible switching states combinations with different values of D to generate a 60V average output voltage.

TABLE II
POSSIBLE SWITCH COMBINATIONS TO GENERATE 60V AVERAGE OUTPUT

State number	Output voltage level			PWM duty cycle D	Average output voltage
	30v	90v	120v		
1	Yes	Yes	Yes	0.75	60v
2	Yes	-	Yes	0.80	60v
3	-	Yes	Yes	0.57	60v
4	-	Yes	-	0.67	60v
5	-	-	yes	0.50	60v

Similarly Table III shows five possible switching states combinations with different values of D to generate a 45V average output voltage.

TABLE III
POSSIBLE SWITCH COMBINATIONS TO GENERATE 45V AVERAGE OUTPUT

State number	Output voltage level			PWM duty cycle D	Average output voltage
	30v	90v	120v		
1	Yes	Yes	Yes	0.5625	45v
2	Yes	-	Yes	0.6	45v
3	-	Yes	Yes	0.42	45v
4	-	Yes	-	0.5	45v
5	-	-	yes	0.375	45v

The operation of the proposed converter was investigated using MATLAB/SIMULINK.

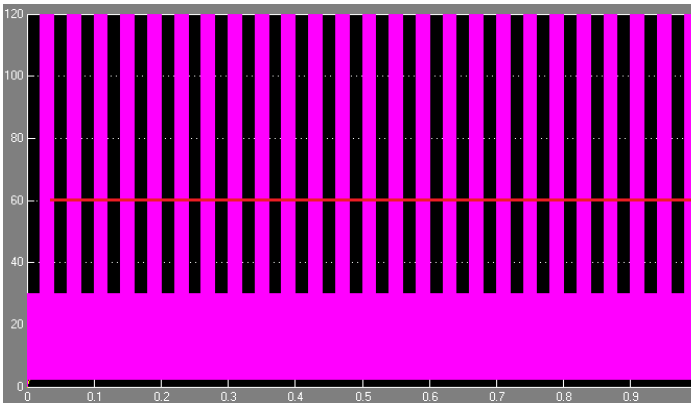

Fig.4. Measured output voltage waveform for V_o=60V PWM duty cycle D=0.8 with the voltage levels of 30V and 120V respectively.

Here there are two output voltage levels but the average output voltage is 60v only.

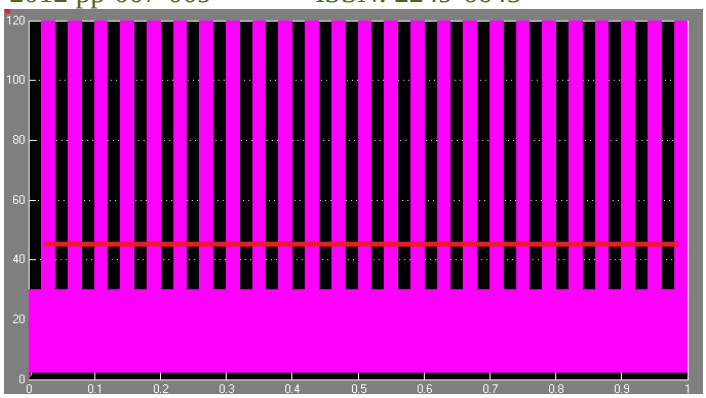

Fig.5. Measured output voltage waveform for V_o=45V PWM duty cycle D=0.6 with the voltage levels of 30V and 120V respectively.

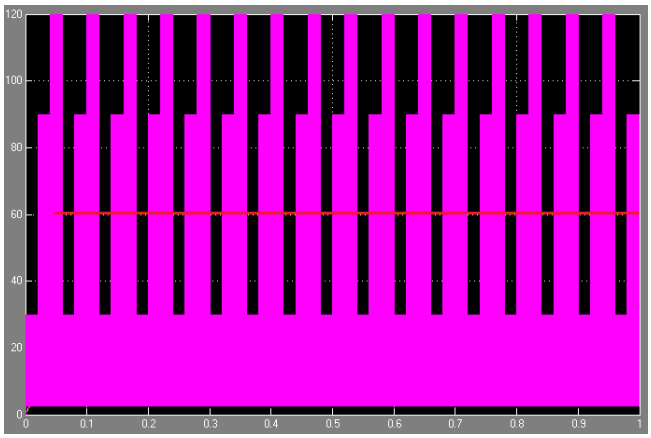

Fig.6. Measured output voltage waveform for V_o=60V; PWM duty cycle D=0.75 with the voltage levels of 30V, 90V and 120V respectively.

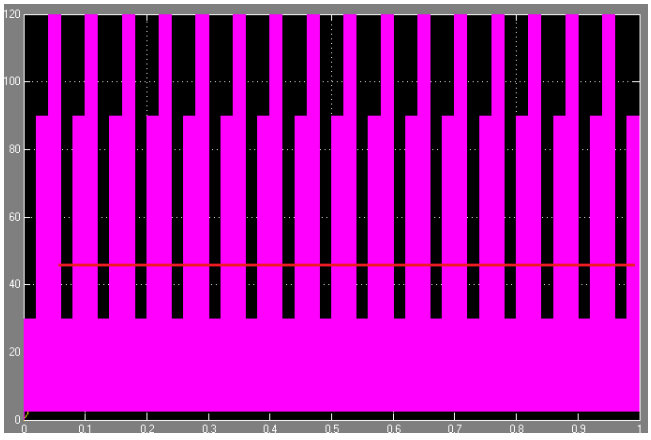

Fig.7. Measured output voltage waveform for V_o=45V; PWM duty cycle D=0.5625 with the voltage levels of 30V, 90V and 120V respectively.

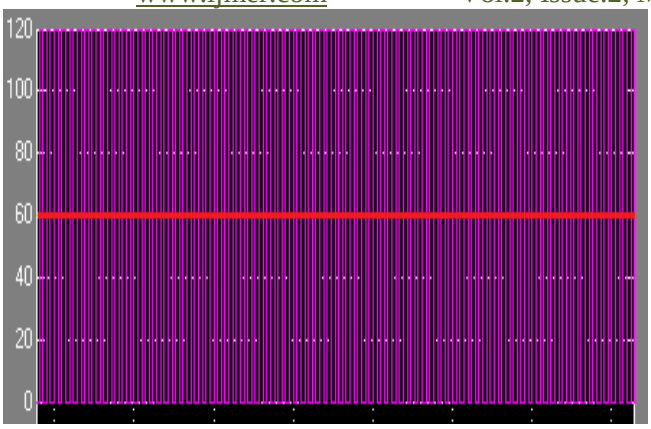

Fig.8. Measured output voltage waveform for V_o=60V; PWM duty cycle D=0.5 with the voltage levels of 120V respectively.

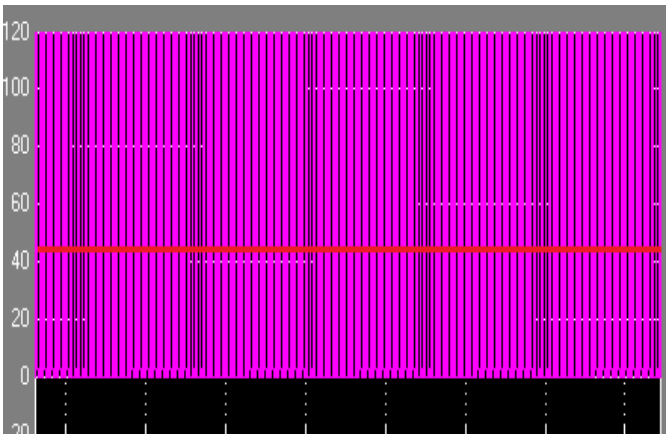

Fig.9. Measured output voltage waveform for V_o=45V; PWM duty cycle D=0.375 with the voltage levels of 120V respectively.

In Fig 4-9 y-axis represents the voltage divisions and x-axis represents time divisions

Figs. 4, 6, 8 show measured output voltages for three different device switching combinations (states 2, 1 and 5 in table II) to get 60V as average output voltage. Similarly Figs 5, 7, 9 show measured output voltages for three different device switching combinations (states 2, 1, 5 in table III) to get 45V as average output voltage. It is apparent from the figures that PWM control allows alternative switching options for the required output voltage level. Converter operation with the same switch combinations was also simulated using PSpice showing good agreement with measurement.

III. FAULT TOLERANT INVESTIGATION

Fault that can occur in the switches may be open circuit or short circuit fault. In this section both open and short circuit faults are discussed and the fault tolerant behavior of the converter is evaluated using the 60V operating states discussed in section II as an example. Here only one fault can be occur at a time or two faults can be occur the proposed converter must demonstrate the ability to detect a short circuit or open circuit component fault and must change the switching states appropriately to recover the required average output voltage. Here voltage and current sensors are used in order to sense the faults.

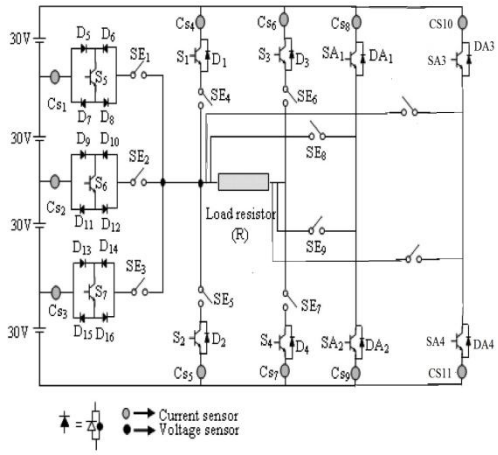

Fig.10. fault tolerant multi level H-bridge dc-dc converter.

Total number of sensors is low when compared with alternative circuit topologies [8]. However, the number sensors can be reduced even further by monitoring the output voltage using a neural network technique [12] or by using a smart IGBT gate drive with self-diagnosis and fault protection [13], the complete fault tolerant of the converter is shown in Fig

IV. OPEN CIRCUIT FAULTS

If an open circuit fault occurs in any of the main switches S1-S4 or D1-D4, the extended additional leg1 must be activated. If the open circuit fault occurs in both main switches and also additional leg1 then activate additional leg2. The switching sequence following an open circuit fault in S1 is discussed here in detail as an example.

Under normal operating conditions, S1 is switched ON and the controller receives a current measurement from C_{s4}. If the controller does not receive this signal while S1 is still switched ON, the controller will flag this as an open circuit fault in S1. The controller now identifies a new switching state that needs to be activated, in this case switches SA1 and SE8, in order to provide the required voltage. Fig 10 shows how SA1 and SE8 are switched on to maintain normal operation at the same output voltage when an open circuit fault occurs in S1. After the fault, the current passing through S1 falls to zero, but load current continues to flow through SA1 and SE8.

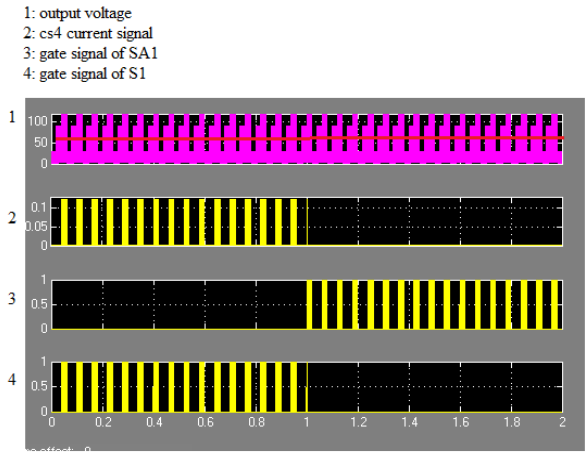

Fig.10. Output voltage waveform before and after an open circuit fault in main switch S1.

Under this conditions i.e., switch S1 is open circuited, load current flowing through SA1 and SE8 controller receives a current measurement from C_{s8} if the open circuit fault occurs in SA1 then controller will identifies a new switching state that needs to be activated now switches SA3 and SE10 will be activated after the fault current passing through SA1 falls to zero and load current continues to flow through SA3and SE10 as shown in the Fig.11

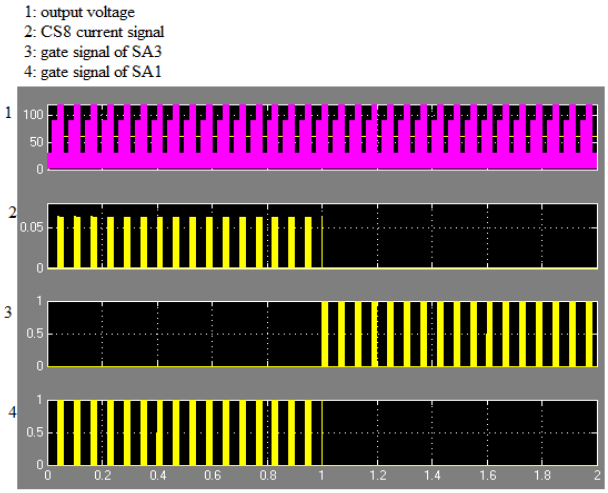

Fig.11. Output voltage waveform before and after an open circuit fault in main switch S1 and auxiliary switch SA1.

If the open circuit fault occurs in any of the selector switching cells (devices S5-S7, diodes D5-D16 and bidirectional switches SE1-SE3), the converter will no longer be able to produce the required average output voltage using the existing switch state combination. For example, under normal operating conditions, the converter produces output voltage levels of 30, 90, 120 with duty cycle off D=0.75 to generate $V_o = 60V$. If an open circuit fault were to occur in switch S5 (say), the converter is no longer able to produce a voltage level of 90V leading to the loss of the required 60V output voltage. On detecting the fault, the sequence of switching states need to change to operate the convert at 120V and a duty cycle of D=0.5.

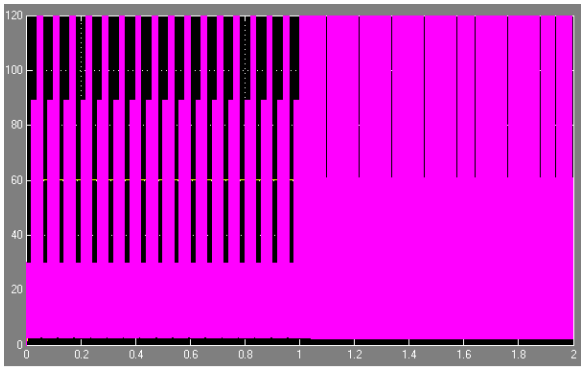

Fig.12. Output voltage waveform when open circuit fault occurs in switch S5

Fig.12. shows measured output voltage waveform when open circuit fault occurs in S5; similar results are obtained when simulating the operation of the circuit under the same fault conditions.

V. SHORT CIRCUIT FAULT

Diode short circuit faults are detected using the voltage sensors circuits shown in Fig13 short circuit faults in the power devices are detected via the gate drive circuits. On detection, short circuit faults are isolated by deactivating the corresponding selector switch. The control of the system is more complex when compared with open circuit faults responses due to the large number of voltage sensors and switches needed to detect and isolate each fault. The switching sequence following a short circuit fault in S1 is discussed here as an example.

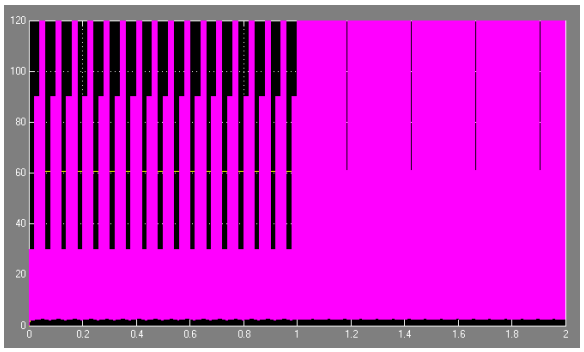

Fig.13. Output voltage waveform when short circuit fault occurs in selector switch S5

If the short circuit fault occurs in switch S1. On detecting the fault, SE4 is switched OFF and SE8 and SA1 switched on to initiate the new conduction state. Fig.13 show output voltage waveform generating 60V average output voltage and voltage after the fault is zero along switch S5.

VI. CONCLUSION

Fault tolerant multilevel H-bridge dc-dc converter topology has been presented in this paper. Different switching states are combined with PWM control to produce and maintain a constant average output voltage despite the occurrence of converter open circuit and short circuit fault. This converter also works even though fault occur in auxiliary leg

APPENDIX

TABLE VI

FAULT TOLERANT INVESTIGATIONS IN THE DIODES

	ACTIONS	
Switches	Open circuit faults	Short circuit faults
D1	Not involved in forward power flow operation	Deactivate SE4 and activate SA1 and SE8
D2	Not involved in forward power flow operation	Keep SE5 open
D3	Not involved in forward power flow operation	Keep SE6 open
D4	Not involved in forward power flow operation	Deactivate SE7 and activate SA2 and SE9
DA1	Not involved in forward power flow operation	Deactivate SE8 and activate S1 and SE4
DA2	Not involved in forward power flow operation	Deactivate SE9 and activate S4 and SE7
D5	Change to different switching states Combinations and D	Deactivate SE1 and change to different switching states combinations and D
D6	Not involved in forward power flow operation	
D7	Not involved in forward power flow operation	
D8	Change to different switching states Combinations and D	
D9	Change to different switching states Combinations and D	Deactivate SE2 and change to different switching states combinations and D
D10	Not involved in forward power flow operation	
D11	Not involved in forward power flow operation	
D12	Change to different switching states Combinations and D	
D13	Change to different switching states Combinations and D	Deactivate SE3 and change to different switching states combinations and D
D14	Not involved in forward power flow operation	
D15	Not involved in forward power flow operation	
D16	Change to different switching states Combinations and D	

Table VII

FAULT TOLERANT INVESTIGATION IN POWER DEVICES

	Actions	
Switches	Open circuit faults	Short circuit faults
S1	Activate SA1 and SE8	Deactivate SE4 and activate SA1 and SE8
S2	Not involved in forward power flow operation	keep SE5 always open
S3	Not involved in forward power flow operation	Keep SE6 always open
S4	Activate SA2 and SE9	Deactivate SE7 and activate SA2 and SE9
SA1	Activate S1 and SE4	Deactivate SE8 and activate S1 and SE4
SA2	Activate S4 and SE7	Deactivate SE9 and activate S4 and SE7
S5	Change to different Switching states combinations and D	Deactivate SE1 and Change to different Switching states combinations and D
S6	Change to different Switching states combinations and D	Deactivate SE2 and Change to different Switching states combinations and D
S7	Change to different Switching states combinations and D	Deactivate SE3 and Change to different Switching states combinations and D

Table VIII
FAULT TOLERANT INVESTIGATION IN THE POWER DEVICES IF TWO SWITCHES FAILS

switches	Open circuit fault	Short circuit fault
S1, SA1	Activate SA3 and SE10	Deactivate SE4 and activate SA3 and SE10
S4, SA2	Activate SA4, SE 11	Deactivate SE47 and activate SA4 and SE11
S3	Not involved in forward power flow operation	Keep SE6 always open
S2	Not involved in forward power flow operation	keep SE5 always open

REFERENCE

[1] M. R. Holman and S. J. Rowland, "Design and development of a new cryosurgical instrument utilizing the Peltier thermoelectric effect,"*J. Med. Eng. Technol.*, vol. 21, no. 3–4, pp. 106–110,1997.

[2] P. A. Kullstam, "Availability, MTBF and MTTR For repairable M out of N system," *IEEE Trans. Rel.*, vol. R-30, no. 4, pp. 393–394, Oct. 1981.

[3] R. V.White and F.M.Miles, "Principles of fault tolerance," in *Proc. IEEE Appl. Power Electron. Conf. Expo.—APEC*, San Jose, Cost Rica, 1996, pp. 18–25.

[4] A. Chen, L. Hu, L. Chen, Y. Deng, and X. He, "A multilevel converter topology with fault-tolerant ability," *IEEE Trans. Power Electron.*, vol. 20, no. 2, pp. 405–415, Mar. 2005.

[5] X.Kou, K. A. Corzine, andY. L. Familiant, "A unique fault-tolerant design for flying capacitor multilevel inverter," *IEEE Trans. Power Electron.*, vol. 19, no. 4, pp. 979–987, Jul. 2004.

[6] B. Francois and J. P. Hautier, "Design of a fault tolerant control system for a N.P. C. multilevel inverter," in *Proc. IEEE Int. Symp. Ind. Electron.*, L'Aquila, Italy, 2002, vol. 4, pp. 1075–1080.

[7] S.Miaosen, P. F. Zheng, and L.M. Tolbert, "MultilevelDC-DC power conversion system with multiple DC sources," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 420–426, Jan. 2008.

[8] K. Ambusaidi, V. Pickert, and B. Zahawi, "Computer aided analysis of fault tolerant multilevel DC-DC converters," in *Proc. IEEE Conf. Power Electron., Drives Energy Syst. Ind. Growth*, New Delhi, India, 2006, pp.1–6.

[9] F. H. Khan and L. M. Tolbert, "Multiple load-source integration in a multilevel modular capacitor clamped dc/dc converter featuring fault tolerant capability," *IEEE Trans. Power Electron.*, vol. 24, no. 1, pp. 14–24, Jan. 2009.

[10] V. Choudhary, E. Ledezma, R. Ayyanar, and R.M. Button, "Fault tolerant circuit topology and control method for input-series and output-parallel modular DC-DC converters," *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 402–411, Jan. 2008.

[11] G. Ceglia,V. Guzman, C. Sanchez, F. Ibanez, J.Walter, and M. I. Gimenez, "A new simplified multilevel inverter topology for DC-AC conversion," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1311–1319, Sep. 2006.

[12] S. Khomfoi and L. M. Tolbert, "Fault diagnostic system for a multilevel inverter using a neural network," *IEEE Trans. Power Electron.*, vol. 22, no. 3, pp. 1062–1069, May 2007.

[13] C. Lihua, F. Z. Peng, and C. Dong, "A smart gate drive with self-diagnosis for power MOSFETs and IGBTs," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC 2008)*, pp. 1602–1607.