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Design, Fault Detection and Mitigation in Cascaded H-Bridge STATCOM

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***Abstract*-The concept of multilevel inverters, introduced about 20 years ago entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. The benefits are especially clear for medium-voltage drives in industrial applications and are being considered for future naval ship propulsion systems. This dissertation is dedicated to a comprehensive study of static synchronous compensator (STATCOM) systems utilizing cascaded-multilevel converters (CMCs). Among flexible AC transmission system (FACTS) controllers, the STATCOM has shown feasibility in terms of costeffectiveness in a wide range of problem-solving abilities from transmission to distribution levels. Referring to the literature reviews, the CMC with separated DC capacitors is clearly the most feasible topology for use as a power converter in the STATCOM applications. The controls for the CMC-based STATCOM were, however, very complicated. The intricate control design was begun without well-defined system transfer functions. The control compensators were, therefore, randomly selected. The stability of the system was achieved by trial and error processes, which were time-consuming and ineffective. To be able to operate in a high-voltage application, a large number of DC capacitors are utilized in a CMC-based STATCOM. All DC capacitor voltages must be balanced in order to avoid over-voltages on any particular link. Not only do these uneven DC voltages introduce voltage stress on the semiconductor switches, but they also lower the quality of the synthesized output waveforms of the converter.A SIMULINK based model is developed and Simulation results are presented.**

Keywords-Cas caded H-Bridge, Multilevel Converter, PWM

I. INTRODUCTION

With the advancement of power electronics and emergence of new multilevel converter topologies, it is possible to work at voltage levels beyond the classicsemiconductor limits. The multilevel converters achieve high-voltage switching by means of a series of voltage steps, each of which lies within the ratings of the individual power devices. Among the multilevel Converters [1-4], the cascaded H-bridge topology (CHB) is particularly attractive in high-voltage applications, because it requires the least number of components to synthesize the same number of voltage levels.

Additionally, due to its modular structure, the hardware implementation is rather simple and the maintenance operation is easier than alternative multilevel converters.The multilevel voltage source inverter is recently applied in many industrialapplications such as ac power supplies, static VAR compensators, drive systems, etc. Oneof the significant advantages of multilevel configuration is the harmonic reduction in theoutput waveform without increasing switching frequency or decreasing the inverter power output [5-11]. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitor voltagesources. The so-called multilevel starts from three levels. As the number of levels reachinfinity, the output THD approaches zero. The number of the achievable voltage levels,however, is limited byvoltage unbalance problemsvoltage clamping requirement, circuitlayout, andpackaging constraints.

As higher level converters are used for high output rating power applications, a large number of power switching devices will be used. Each of these devices is a potential failure point. Therefore, it is important to design a ophisticated control to produce a fault-tolerant STATCOM. A faulty power cell in a cascaded H-Bridge STATCOM can potentially cause switch modules to explode [10] leading to the fault conditions such as a short circuit or an overvoltage on the power system resulting in an expensive down time [11]. Subsequently, it is crucial to identify the existence and location of the fault for it to be removed. Several fault detection methods have been proposed over the last few years [10]–[18]. Resistor sensing, current transformation, and V_{CE} sensing are some of the more common approaches. For example, a method based on the output current behavior is used to identify IGBT short circuits [12]. The primary drawback with the proposed approach is that the fault detection time depends on the time constant of the load. Therefore, for loads with a large RL time constant, the faulty power cell can go undetected for numerous cycles, potentially leading to circuit damage. Another fault detection approach proposed in [13] is based on a switching frequency analysis of the output phase voltage. This method was applied to flying capacitor converters and has not been extended to cascaded converters. AI-based methods proposed to extract pertinent signal features to detect faults in [14]. In [15], sensors are used to measure each IGBT current and to initiate switching if a fault is detected. A fault-tolerant neutral point-clamped converter was proposed in [16].In [17], a reconfiguration system based on bidirectional switches has been designed for three-phase asymmetric cascaded H-bridge inverters. The fundamental output voltage phase shifts are used to rebalance a faulted multilevel cascaded converter in [18].

In this paper, the method we propose requires only that the output dc link voltage of each phase be measured. This measurement is typically accomplished anyway for control purposes. If a fault is detected, the module in which the fault occurred is then isolated and removed from service. This approach is consistent with the modular design of cascaded converters in which the cells are designed to be interchangeable and rapidly removed and replaced. Until the module is replaced, the multilevel STATCOM continues to operate with slightly decreased, but still acceptable, performance. In summary, this approach offers the following advantages:

- No additional sensing requirements;
- Additional hardware is limited to two by-pass switches per modle;
- Is consistent with the modular approach of cascaded multilevel inverter;and
- The dynamic performance and THD of the STATCOM is not significantly impacted.

II.PROPOSED NOVEL CONVERTER

III. DESIGN OF MULTILEVEL BASED STATCOM

A. Principle of STATCOM

A STATCOM, which is schematically depicted in Figure-1, consists of a two-level VSC, a dc energy storage device, a coupling transformer connected in shunt to the DS. The VSC converts the dc voltage across the storage device into a set of three-phase ac output voltages. These voltages are in phase and coupled with the ac system through the reactance of the coupling transformer. Suitable adjustment of the phase and magnitude of the STATCOM output voltages allows effective control of active and reactive power exchanges between the STATCOM and the ac system. Such configuration allows the device to absorb or generate controllable active and reactive power.

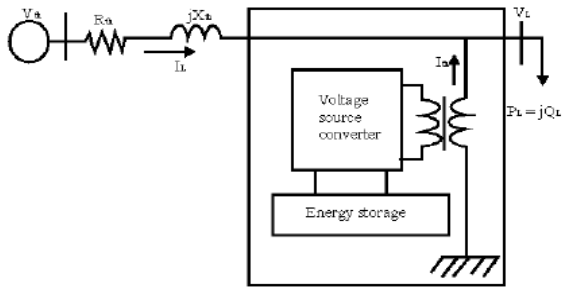


Figure –1 Schematic Diagram of a STATCOM

Here, such device is employed to provide continuous voltage regulation using an indirectly controlled converter. As shown in Figure-1 the shunt injected current I_{sh} corrects the voltage sag by adjusting the voltage drop across the system impedance Z_{th}. The value of I_{sh} can be controlled by adjusting the output voltage of the converter. The shunt injected current I_{sh} can be written as,

$$I_{sh} = I_L - I_S = I_L - (Vth - V_L) / Z_{th} \quad (1)$$

$$I_{sh} /\_\eta = I_L /\_- \theta \quad (2)$$

The complex power injection of the STATCOM can be expressed as,

$$S_{sh} = V_L I_{sh}^{*} \quad (3)$$

B. Control for Reactive Power Compensation

The main aim of the control scheme is to maintain constant voltage magnitude at the load point. The control system only measures the rms voltage at the load point, i.e., no reactive power measurements are required.

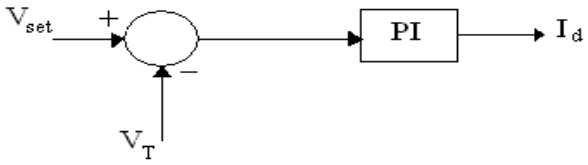


Figure-2 PI control for reactive power compensation

The controller input is an error signal obtained from the reference voltage and the rms terminal voltage measured. Such error is processed by a PI controller; the output is the I_d, which is provided to the PWM signal generator as shown in figure-2. The PI controller processes the error signal and generates the required active power component to drive the error to zero, i.e. the load rms voltage is brought back to the reference voltage.

C.Control for Harmonics Compensation

The Modified SRFT method is presented in [7]. It is called the instantaneous current component (i_d-i_q) method. This is similar to the SRFT method. The transformation angle 'θ'is now obtained with the voltages of the ac network. The major difference is that, due to voltage harmonics and imbalance, the speed of the reference frame is no longer constant. It varies instantaneously depending of the waveform of the three phase voltage system. In this method the compensating currents are obtained from the instantaneous active and reactive current components of the nonlinear load. In the same way, the mains voltages $V_{(a,b,c)}$ and the available currents $i_{l(a,b,c)}$ in α-β components must be calculated as given by (4), where C is Clarke Transformation Matrix. However, the load current components are derived from a SRF based on the Park transformation, where 'θ' represents the instantaneous voltage vector angle (5).

$$\begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix} = [C] \begin{bmatrix} I_{la} \\ I_{lb} \\ I_{lc} \end{bmatrix} \quad (4)$$

$$\begin{bmatrix} I_{ld} \\ I_{lq} \end{bmatrix} = \begin{bmatrix} cos\theta & sin\theta \\ -sin\theta & cos\theta \end{bmatrix} \begin{bmatrix} I_{l\alpha} \\ I_{l\beta} \end{bmatrix}, \theta = tan^{-1} \frac{V_\beta}{V_\alpha} \quad (5)$$

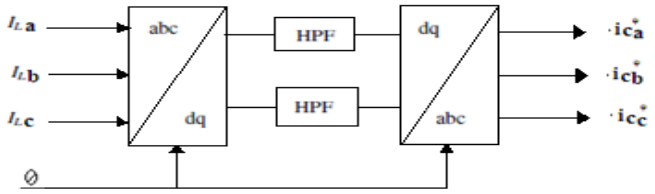


Figure-3 Block diagram of SRF method

Fig-3 shows the block diagram SRF method. Under balanced and sinusoidal voltage conditions angle θ is a uniformly increasing function of time. This transformation angle is sensitive to voltage harmonics and unbalance; therefore dθ/dt may not be constant over a period. With transformation given below the direct voltage component is

$$\begin{bmatrix} i_{ld} \\ i_{lq} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2+V_\beta^2}} \begin{bmatrix} V_\alpha & V_\beta \\ -V_\beta & V_\alpha \end{bmatrix} \quad (6)$$

$$\begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} = \frac{1}{\sqrt{V_\alpha^2+V_\beta^2}} \begin{bmatrix} V_\alpha & -V_\beta \\ V_\beta & V_\alpha \end{bmatrix} \begin{bmatrix} i_{cd} \\ i_{cq} \end{bmatrix} \quad (7)$$

$$\begin{bmatrix} I_{Comp,a} \\ I_{Comp,b} \\ I_{Comp,c} \end{bmatrix} = [C]^T \begin{bmatrix} i_{c\alpha} \\ i_{c\beta} \end{bmatrix} \quad (8)$$

D. Cascaded H-Bridge Multilevel Inverter

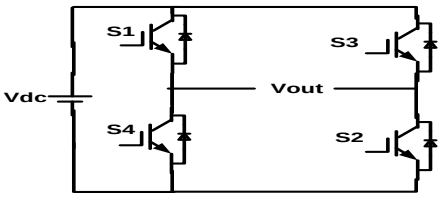


Figure-4 Circuit of the single cascaded H-Bridge Inverter

Fig.4 shows the circuit model of a single CHBinverter configuration. By using single H-Bridge we can get 3 voltage levels. The number of output voltage levels of CHB is given by 2n+1 and voltage step of each level is given by Vdc/2n,where n is number of H-bridges connected in cascaded. The switching sequence is given in Table-I.

E. PWM Techniques for CHB Inverter

The most popular PWM techniques used for CHB inverter are 1. Phase Shifted Carrier PWM (PSCPWM), 2. Level Shifted Carrier PWM (LSCPWM)

Case-1:- Phase Shifted Carrier PWM (PSCPWM)

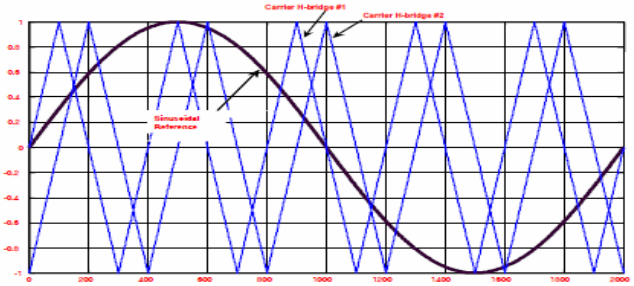


Fig-5 phase shifted carrier PWM

Figure-5 shows the PSCPWM. In general, a multilevel inverter with *m* voltage levels requires (*m*–1) triangular carriers. In the PSCPWM, all the triangular carriers havethe same frequency and the same peak-to-peak amplitude, but there is a phase shiftbetween any twoadjacent carrier waves, given by $\varphi_{cr}=360^0/(m-1)$. The modulating signal is usually a three-phase sinusoidal wave with adjustable amplitudeand frequency. The gate signals are generated by comparing the modulatingwave with the carrier waves.Itmeans for five-level inverter, four triangular carriers are needed with a 90° phasedisplacement between any two adjacent carriers. In this case the phase displacement ofV_{cr1}=0°, V_{cr2}=90°, V_{cr1-}=180° *and* V_{cr2-} = 270°.

Case-2:- Level Shifted Carrier PWM (LSCPWM)

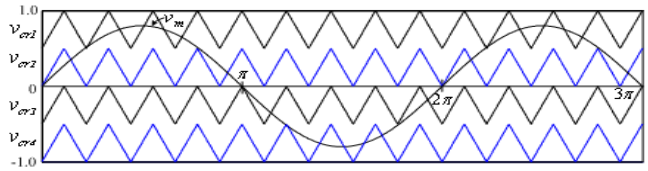


Figure-6 Level shifted carrier PWM (IPD)

Figure-6 shows the LSCPWM.The frequency modulation index is given by $m_f = f_{cr} / f_m$, (34)
where f_m is modulating frequency and f_{cr} are carrier waves frequency. The amplitude modulation index 'm_a' is defined by$m_a = V_m / V_{cr}$ (m-1) for $0 \le m_a \le 1$ (35)
Where V_m is the peak value of the modulating wave and V_{cr} is the peak value of the each carrier wave [1]. Theamplitude modulation index, m_a is 1 and the frequency modulation index, m_f is 6.The triggering circuit is designed based on the three phase sinusoidal modulation waves V_a, V_b, and V_c. The sources have been obtained with same amplitude and frequency but displaced 120° out of the phase with each others. For carriers signals, the time values of each carrier waves are set to [0 1/600 1/300] while the outputs values are set according to the disposition of carrier waves. After comparing, the output signals of comparator are transmitted to the IGBTs. Figures9, 10 and 11show the waveforms based on three schemes of LSCPWM: (a) in phase disposition (IPD) fig-9, where all carriers are in phase; (b) alternative phase opposite disposition (APOD) fig-10, where all carriers are alternatively in opposite disposition; and (c) phase opposite disposition (POD) fig-11, where all carriers above zero reference are in phase but in opposition with those below the zero reference [1].Out of IPD, APOD and POD; the authors studied that, IPD give better harmonic performance.

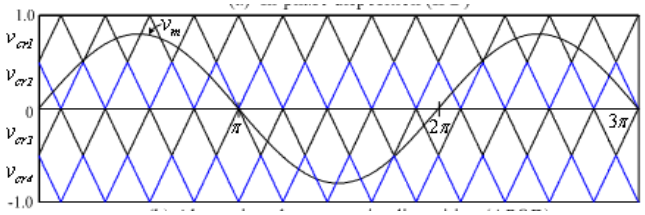


Fig. 7 Alternative phase opposite disposition (APOD)

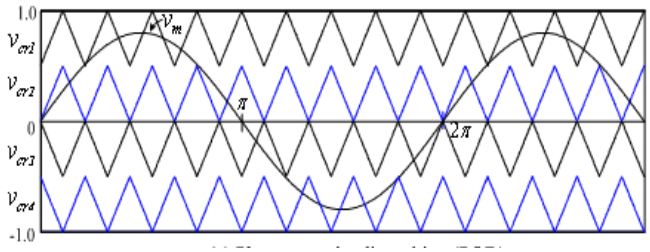


Fig.8phase opposite disposition (POD)

IV. DESIGN OF SINGLE H-BRIDGE CELL

A Device Current

The IGBT and DIODE currents can be obtained from the load current by multiplying with the corresponding duty cycles. Duty cycle, d = ½(1+Kmsinωt)

Where, m = modulation index K = +1 for IGBT, -1 for Diode.

$$i_{ph} = \sqrt{2} I \sin(\omega t - \phi)$$

Where i = RMS value of the load (output) current,

Ø = Phase angle between load voltage and current.

Then the device current can be written as follows.

$$\therefore i_{device} = \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) * (1 + km \sin \omega t)$$

The average value of the device current over a cycle is calculated as

$$i_{avg} = \frac{1}{2\pi} \int_{\phi}^{\pi+\phi} \frac{\sqrt{2}}{2} I \sin(\omega t - \phi) * (1 + km \sin \omega t) d\omega t$$

$$= \sqrt{2} I \left[\frac{1}{2\pi} + \frac{Km}{8} \cos \phi \right]$$

The device RMS current can be written as

$$i_{rms} = \sqrt{\int_{\phi}^{\pi+\phi} \frac{1}{2\pi} \left(\sqrt{2}\, I \sin(\omega t - \phi)\right)^2 * \frac{1}{2} * \left((1 + k\, m sin\omega t) d\omega t\right)}$$

$$= \sqrt{2} I \sqrt{\left[\frac{1}{8} + \frac{Km}{3\pi} \cos \phi \right]}$$

B IGBT Loss Calculation

IGBT loss can be calculated by the sum of switching loss and conduction loss. Where conduction loss can be calculated by,

$$P_{on\,(IGBT)} = V_{ceo} * I_{avg\,(igbt)} + I^2_{rms\,(igbt)} * r_{ceo}$$

$$I_{avg\,(igbt)} = \sqrt{2} I \left[\frac{1}{2\pi} + \frac{m}{8} \cos \phi \right]$$

$$I_{rms\,(igbt)} = \sqrt{2} I \sqrt{\left[\frac{1}{8} + \frac{m}{3\pi} \cos \phi \right]}$$

Values of V_{ceo} and r_{ceo} at any junction temperature can be obtained from the output characteristics (Ic vs. Vce) of the IGBT as shown in Fig .9.

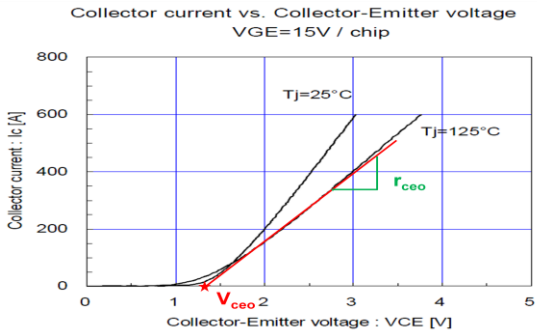


Figure9 IGBT output characteristics

The switching losses are the sum of all turn-on and turn-off energies at the switching events

$$E_{sw} = E_{on} + E_{off} = a + bI + cI^2$$

Assuming the linear dependence, switching energy $E_{sw} = (a + bI + cI^2) * \frac{V_{DC}}{V_{nom}}$

Here V_{DC} is the actual DC-Link voltage and V_{nom} is the DC-Link Voltage at which E_{sw} is given.Switching losses are calculated by summing up the switching energies.

$$P_{sw} = \frac{1}{T_o} \sum_{n} E_{sw}\,(i)$$

Here 'n' depends on the switching frequency.

$$P_{sw} = \frac{1}{T_o} \sum_{n} (a + bI + cI^2)$$

$$= \frac{1}{T_o} \left[\frac{a}{2} + \frac{bI}{\pi} + \frac{cI^2}{4} \right]$$

After considering the DC-Link voltage variations switching losses of the IGBT can be written as follows.

$$P_{sw\,(IGBT)} = f_{sw} \left[\frac{a}{2} + \frac{bI}{\pi} + \frac{cI^2}{4} \right] * \frac{V_{DC}}{V_{nom}}$$

So, the sum of conduction and switching losses gives the total losses.

$$P_{T(IGBT)} = P_{on\,(IGBT)} + P_{sw\,(IGBT)}$$

C Diode Loss Calculation

The DIODE switching losses consists of its reverse recovery losses and the turn-on losses are negligible.

$$E_{rec} = a + bI + cI^2$$

$$P_{sw\,(DIODE)} = f_{sw} \left[\frac{a}{2} + \frac{bI}{\pi} + \frac{cI^2}{4} \right] * \frac{V_{DC}}{V_{nom}}$$

So, the sum of conduction and switching losses gives the total DIODE looses.

$$P_{T(DIODE)} = P_{on\,(DIODE)} + P_{sw\,(DIODE)}$$

The total loss per one switch (IGBT+DIODE) is the sum of one IGBT and DIODE loss.

$$P_T = P_{T(IGBT)} + P_{T(DIODE)}$$

D. Thermal Calculations

The junction temperatures of the IGBT and DIODE are calculated based on the device power losses and thermal resistances. The thermal resistance equivalent circuit for a module is shown in Fig 5. In this design the thermal calculations are started with heat sink temperature as the reference temperature. So, the case temperature from the model can be written as follows.

$$T_c = P_T R_{th(c-h)} + T_h$$

Here $R_{th(c-h)}$ = Thermal resistance between case and heat sink

P_T = Total Power Loss (IGBT+DIODE)

IGBT junction temperature is the sum of the case temperature and temperature raise due to the power losses in the IGBT.

$$T_{j(IGBT)} = P_{T(IGBT)} R_{th(j-c)IGBT} + T_c$$

DIODE junction temperature is the sum of the case temperature and temperature raise due to the power losses in the DIODE.

$$T_{j(DIODE)} = P_{T(DIODE)} R_{th(j-c)DIODE} + T_c$$

The above calculations are done based on the average power losses computed over a cycle. So, the corresponding thermal calculation gives the average junction temperatures. In order to make the calculated values close to the actual values, transient temperature values are to be added to the average junction temperatures.

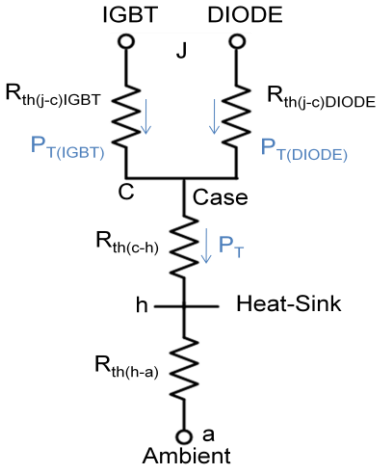


Figure. 10Thermal resistance equivalent circuit

A. DC-Capacitor Selection

The required capacitance for each cell depends on the allowable ripple voltage and the load current. The rms ripple current flowing into the capacitor can be written as follows and the ripple current frequency is double the load current frequency (Novel Hybrid H-Bridge).

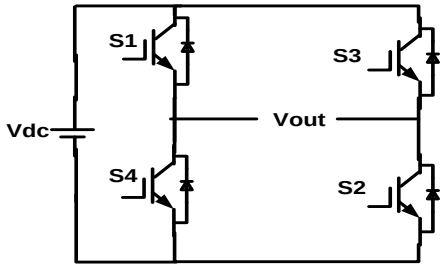


Fig. 11H-Bridge converter

$$I_c = -\frac{I}{V_{dc}}\frac{1}{2}(|U_{ac}| * K + I\omega L)\sin(2\omega t)$$

Since the value of 'L' is very small, the above equation can be written as below.

$$I_c = -\frac{I}{V_{dc}}\frac{1}{2}(|U_{ac}| * K)\sin(2\omega t)$$

$$I_C = -K\frac{1}{2}\frac{|U_{ac}|}{V_{dc}} * \sin(2\omega t)$$

$$= -K\frac{m}{2}\sin(2\omega t)$$

Here 'm' is the modulation index.

$$\text{Here } I_{cp} = C\frac{du_{pp}}{dt}$$

$$\frac{m}{2}I\sqrt{2} = \mathrm{C}\, 2\omega * \Delta V V_{dc}$$

$$\mathrm{C} = \frac{m}{4\omega}\frac{1}{\Delta V V_{dc}}\sqrt{2}I$$

V. MATLAB/SIMULINK MODELING AND SIMULATION RESULTS

Figure-12 shows the Matab/Simulink power circuit model of DSTATCOM. The system parameters chosen are source voltage (V_s) as 11kv, 50Hz AC supply, DC bus capacitance 1550μF, Inverter series inductance 10mH, Source resistance of 0.1Ω and inductance of 0.9mH. Nonlinear loads with resistance and inductance are chosen as 30mH and 60Ω respectively.

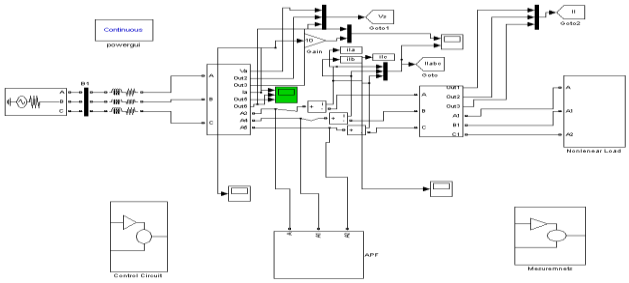


Fig-12Matlab/Simulink power circuit model of DSTATCOM

Case-1 STATCOM without Fault in Gate Driver

Fig. 13 shows the phase-A voltage of five level output of phase shifted carrier PWM inverter.

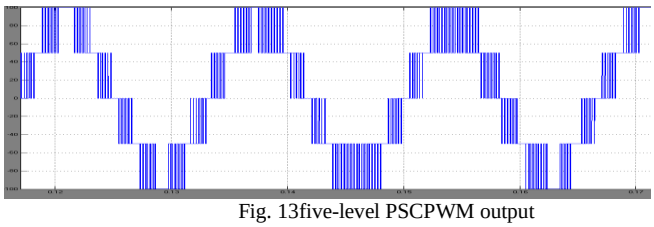


Fig. 13five-level PSCPWM output

Fig. 14 shows the three phase source voltages, three phase source currents and load currents respectively without DSTATCOM. It is clear that without DSTATCOM load current and source currents are same.

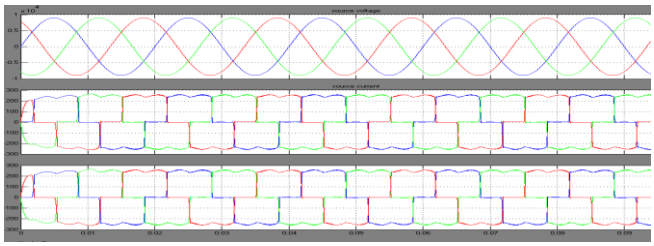


Fig. 14Source voltage, current and load current without DSTATCOM

Fig. 15 shows the three phase source voltages, three phase source currents and load currents respectively with DSTATCOM. It is clear that with DSTATCOM even though load current is non sinusoidal, source currents are sinusoidal.

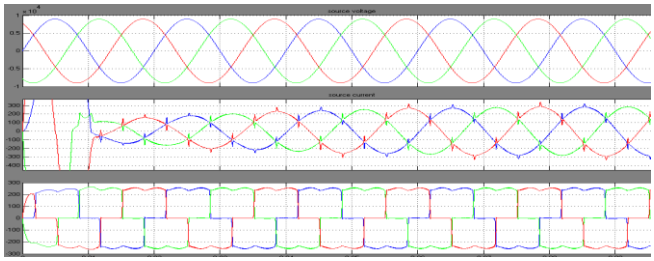


Fig. 15Source voltage, current and load current with DSTATCOM

Fig. 16 shows the DC bus voltage is regulated to 11kv by using PI regulator.

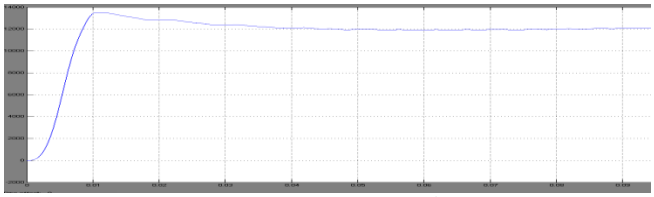


Fig. 16DC Bus Voltage for PSCPWM

Fig. 17 shows the phase-A source voltage and current, even though the load is non linear RL load the source power factor is unity.

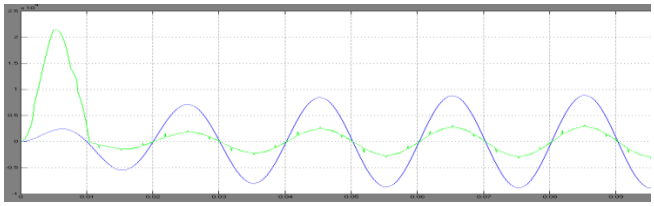


Fig. 17Phase-A source voltage and current

Fig. 18 shows the harmonic spectrum of Phase –A Source current without DSTATCOM. The THD of source current without DSTACOM is 36.89%.

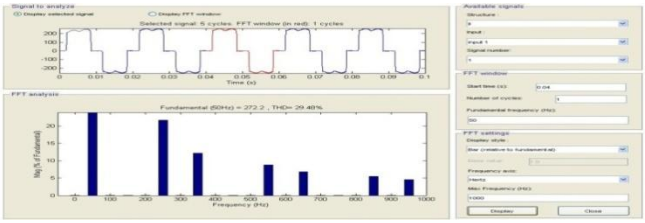


Fig. 18Harmonic spectrum of Phase-A Source current without DSTATCOM

Fig. 19 shows the harmonic spectrum of Phase –A Source current with DSTATCOM. The THD of source current with DSTACOM is 5.05%

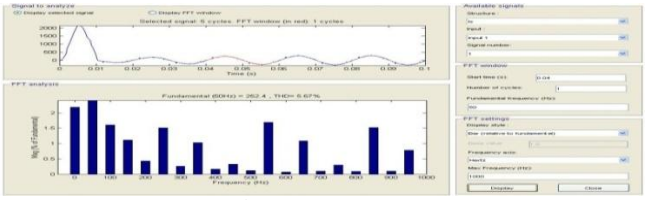


Fig. 19Harmonic spectrum of Phase-A Source current with DSTATCOM

Case-2 STATCOM withFault in Gate Driver

Fig. 20 shows the phase-A voltage of five level output of phase shifted carrier PWM inverter with fault in the gate driver. The fault is applied between 0.1 and 0.2 sec.

Here one voltage level is missing during the period of fault.

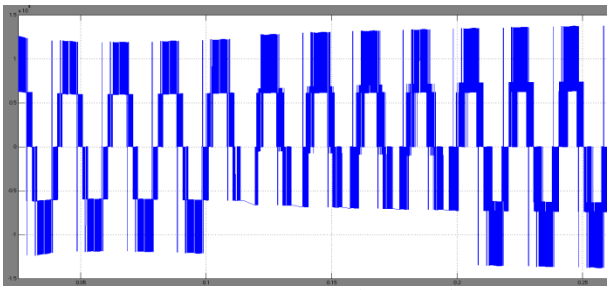
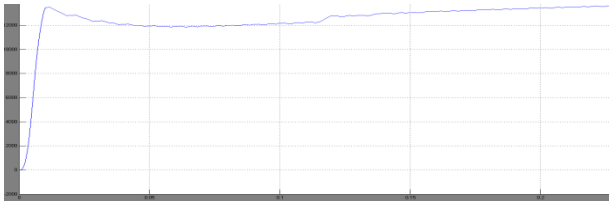


Fig.20 output waveform with fault

Figure 21 shows the filtered waveform by using the filter. The fall in the voltage is clearly observed during the fault.

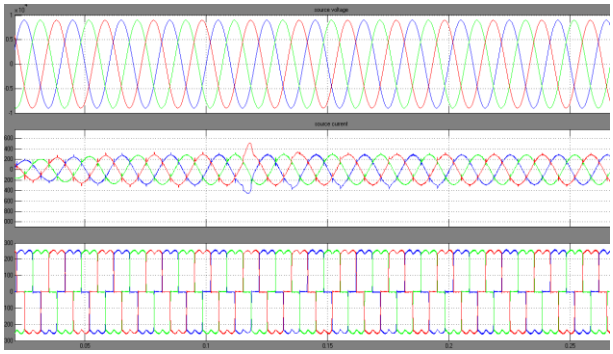
Fig.21 Filtered waveform

Fig 22 shows the dc capacitor voltage which clearly shows the fall in voltage during the fault and regain after mitigation.



Fig;22 DC capacitor voltage

Fig 23 shows the source voltage, source current and load current before, during and after the fault.



Fig;23. Source voltage, sourcecurrent, load currentbefore, during and after fault

VI. CONCLUSION

This paper presents Novel Hybrid H-Bridge multilevel converter. The proposed converter produces more voltage levels with less number of switches compared to H-bridge configuration. This will reduce number of gate drivers and protection circuits which in turn reduces the cost and complexity of the circuit. In this paper, the design procedure for single cell based on cost and losses optimization is carried out. The selection of a single cell is based on SSOA (safe operating Area) and Thermal Rating .The selection of capacitor and heat sink is also carried out. A SIMULINK based model is developed and Simulation results are presented.The total harmonic distortion is also caluculated.THD before fault is 0.64%,THD during fault is 1.28% and THD after the fault is 0.64%.

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