A Series-Connected Multilevel Inverter Topology for Squirrel-Cage Induction Motor Drive

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Abstract: **The concept of multilevel inverters, introduced about 20 years ago entails performing power conversion in multiple voltage steps to obtain improved power quality, lower switching losses, better electromagnetic compatibility, and higher voltage capability. The benefits are especially clear for medium-voltage drives in industrial applications and are being considered for future naval ship propulsion systems. The application of pulsewidth-modulated (PWM) voltages using two-level high-voltage inverters to a squirrel-cage induction motor (SQIM) can cause heating of rotor shaft, voltage spike across the motor terminals, etc. The increase in the number of steps of the motor voltage and hence decreasing the *dv/dt* applied to the machine terminals can be a solution to this problem. The existing topologies that generate this multistep voltage include cascading of a number of single-phase inverters or use of higher order multilevel inverters. In this paper, a topology with series connection of three-phase three-level inverters is proposed, which addresses the problems of medium-voltage drives.**

Keywords: Medium-voltage ac drives, multilevel converter topologies.

I. INTRODUCTION

Multilevel power conversion has been receiving increasing attention in the past few years for high power applications. Numerous topologies and modulation strategies have been introduced and studied extensively for utility and drive applications in the recent literature. These converters are suitable in high voltage and high power applications due to their ability to synthesize waveforms with better harmonic spectrum and attain higher voltages with a limited maximum device rating. In the family of multilevel inverters the three-level topology, called Neutral Point Clamped (NPC) inverter, is one of the few topologies that has received a reasonable consensus in the high power community [2]. These NPC inverters have also been implemented successfully in the industrial applications for high power drives [3].The conventional three-level inverter comprises four switches per phase with a diode clamp connected to the mid-point of the dc link. By closing two of the four switches, the load can be either connected to the top, middle or bottom of the dc link, thereby generating a three-level voltage waveform at the phase leg output. The LC sine filter connected at the output is used to filter out the high link. By closing two of the four switches, the load can

be either connected to the top, middle or bottom of the dc link, thereby generating a three-level voltage waveform at the phase leg output. The LC sine filter connected at the output is used to filter out the high the output of the NPC inverter is directly connected through an LCL filter to the 4160V utility network. Optionally the utility side reactor can be replaced by a feeder transformer which adjusts to higher utility voltages by employing an appropriate turns-ratio. The voltages on the dc link capacitors are maintained at their nominal values by drawing necessary real power from the utility. One of the primary concerns for a successful operation is meeting the harmonic requirements given by IEEE 519-1992 even at very low short-circuit ratio. Hence, the LCL filter connected at the output of the inverter needs to be adequately sized as to meet the stringent current and voltage requirements. At multi-megawatt power levels, where inherently lower short circuit ratios are existing, the dimensioning of such filters becomes a important issue. Similar voltage profiles can also be obtained by using higher order neutral-point-clamped (NPC) multilevel inverters [8], [9] or by cascading a number of two-level inverters [6], [7]. However, the multilevel NPC inverters suffer from dc-bus imbalance [11]–[13], device underutilization problems and unequal ratings of the clamped diodes [9], [10], etc., which are not very serious problems for inverters with three levels or lower. The capacitor voltage imbalance for a five-level one is presented in [14]– [15] which suggest the need of extra hardware in the form of dc choppers or a back-to-back connection of multilevel converters. The cascaded H-bridge topology [6]–[8] suffers from the drawbacks of the usage of huge dc-bus capacitors and complex input transformers for isolated dc bus for each module. These drawbacks are addressed in the proposed topology. Furthermore, the power circuit is modular in structure, and hence, the number of modules to be connected in series depends on the power of the drive.

II. PROPOSED CONVERTER TOPOLOGY

The proposed general configuration of "*n*" number of three level inverters connected in series is shown in Fig. 1. Each inverter module is a three-phase NPC three-level inverter. At the output stage, transformers are used to have the series connection of three-level inverters, as shown in Fig. 1. If "*Vdc*" is the dc-bus voltage of each inverter module, then "*α*" is the turns ratio of each transformer and "*n*" is the number of inverter modules then for sine PWM (SPWM)

strategy; the motor rms phase voltage (VPh_motor) can be expressed as follows

$$\text{Rms of V}_{ph\_motor} \; _= \; \sqrt{3}\,\alpha mn\frac{V_{dc}}{2\sqrt{2}}$$

Where m is the modulation index of the inverter topology defined as follows

$$m = \frac{Peak\ of\ V_{ph\_inverter}}{n\frac{V_{dc}}{2}}$$

Vph_inverter is the total phase voltage reference of the inverter topology. For the given peak of VPh_motor, peak of Vph_inverter can be computed as follows

$$Peak\ of\ V_{ph\_inverter} = \frac{Peak\ of\ V_{ph\_motor}}{\sqrt{3}\alpha}$$

The generation of individual reference voltage signal of each inverter is discussed as follows.

The gate pulses for each three-level inverter module can be derived using two carrier signals. Thus, "n" numbers of such three-level inverter modules require "$2n$" number of carriers [10], [13]. The three-phase voltage reference signals are then compared with these carrier waves to produce the gate pulses for the inverters. For example, the carrier waves and the sinusoidal modulating voltage signal (SPWM technique) for R phase is shown in Fig. 2 for four series-connected three-level inverters. The carrier waves 1 and 1' (Fig. 2) with R-phase voltage reference controls the inverter module 1. Similarly, 2 2', 3–3', and 4–4' carrier waves with R-phase voltage reference generate the gate pulses for the three-level inverter modules 2, 3, and 4, respectively. Thus, each inverter module produces the voltage proportional to a part of the reference phase voltage signals. It is important to note that no two three-level inverter modules switch simultaneously (Fig. 2). Thus, the maximum dv/dt rate of the output voltage of this topology is limited to that of a single three-level inverter module (Fig. 5). The references of each inverter are shown in Fig. 3. The corresponding output line voltages of each inverter are shown in Fig. 4. The four windings, one from each transformer, are connected in series and produced the net R-phase voltage, as shown in Fig. 5 Similarly, the other two phase voltages are generated.
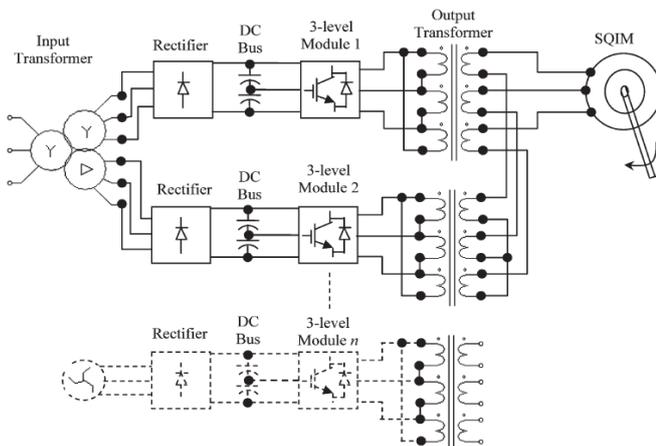
Figure.1 Block diagram of three-phase three-level inverter modules connected in series driving an SQIM.
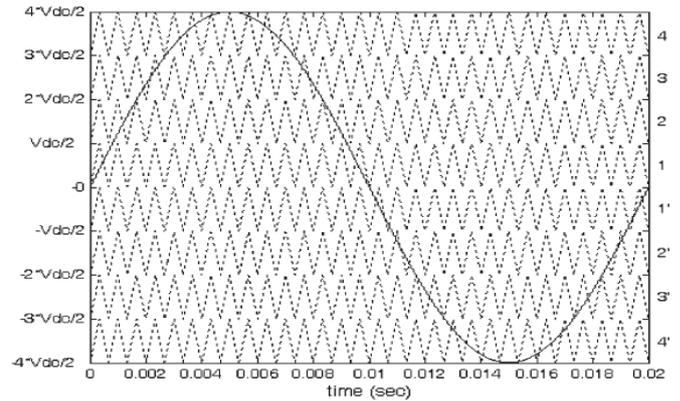
Figure.2 Carrier waves and the sinusoidal modulating voltage signal for R phase in SPWM technique

The line voltage spectra of individual inverters are shown in Fig. 4 for switching frequency of 2.5 kHz. These line voltages get added to produce the net phase voltage of the topology. The voltage spectra are expressed as a percentage of the maximum total fundamental (Vpeak) that can be produced by the topology.

$$V_{peak} \; = \sqrt{2}*V_{ph\_motor}$$

or Vpeak = 2078.5 V for Vdc = 600 V, n = 4, α = 1, and m = 1 using (1). Hence, the spectra show the percentage share of the fundamental of each inverter module. These spectra also suggest that the line voltages of all these inverters contain additional small amount of the 5th-, 7th-, 11th-, 13th-, and higher order harmonics besides the normal switching harmonics. However, the net phase voltage and line voltage of this topology do not contain any of these harmonics, as suggested by the spectra shown in Fig. 5. These harmonics get canceled when the line voltages of the individual inverters are added by the transformers to produce the net phase voltages. The increased number of steps in the motor terminal voltage reduces the dv/dt as that compared with a conventional two-level inverter.
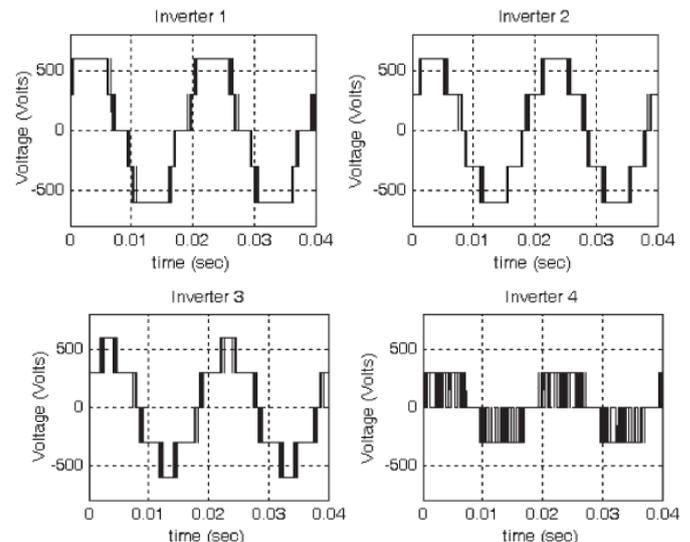
Figure.3 Four series connected Inverters Individual voltages

III.   DYNAMIC MODEL OF INDUCTION MOTOR

The induction machine d-q or dynamic equivalent circuit is shown in Fig. 1 and 2. One of the most popular induction motor models derived from this equivalent circuit is Krause's model detailed in [5]. According to his model, the modeling equations in flux linkage form are as follows:
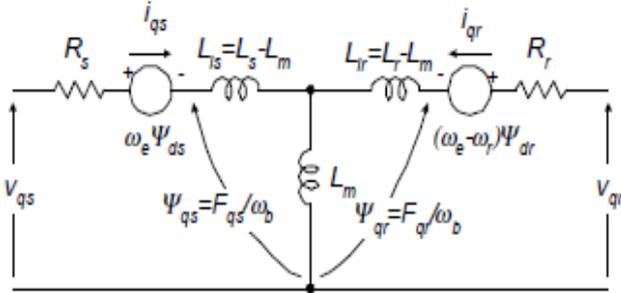
Figure. 4 Dynamic q-axis model
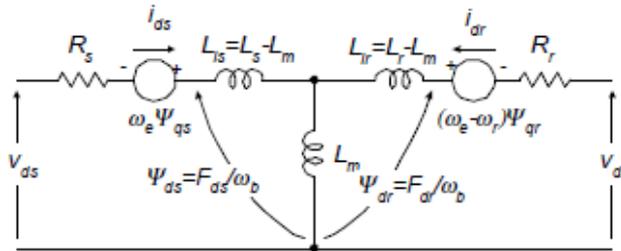
Figure. 5 Dynamic d-axis model

$$\frac{dF_{qs}}{dt} = \omega_b\left[v_{qs} - \frac{\omega_e}{\omega_b}F_{ds} + \frac{R_s}{x_{ls}}\left(F_{mq} + F_{qs}\right)\right] \qquad (1)$$

$$\frac{dF_{ds}}{dt} = \omega_b\left[v_{ds} + \frac{\omega_e}{\omega_b}F_{qs} + \frac{R_s}{x_{ls}}\left(F_{md} + F_{ds}\right)\right] \qquad (2)$$

$$\frac{dF_{qr}}{dt} = \omega_b\left[v_{qr} - \frac{(\omega_e - \omega_r)}{\omega_b}F_{dr} + \frac{R_r}{x_{lr}}\left(F_{mq} - F_{qr}\right)\right] \qquad (3)$$

$$\frac{dF_{dr}}{dt} = \omega_b\left[v_{dr} + \frac{(\omega_e - \omega_r)}{\omega_b}F_{qr} + \frac{R_r}{x_{lr}}\left(F_{md} - F_{dr}\right)\right] \qquad (4)$$

$$F_{mq} = x_{ml}^*\left[\frac{F_{qs}}{x_{ls}} + \frac{F_{qr}}{x_{lr}}\right] \qquad (5)$$

$$F_{md} = x_{ml}^*\left[\frac{F_{ds}}{x_{ls}} + \frac{F_{dr}}{x_{lr}}\right] \qquad (6)$$

$$i_{qs} = \frac{1}{x_{ls}}\left(F_{qs} - F_{mq}\right) \qquad (7)$$

2.2 Voltage Source Converter (VSC)

$$i_{ds} = \frac{1}{x_{ls}}\left(F_{ds} - F_{md}\right) \qquad (8)$$

$$i_{qr} = \frac{1}{x_{lr}}\left(F_{qr} - F_{mq}\right) \qquad (9)$$

$$i_{dr} = \frac{1}{x_{lr}}\left(F_{dr} - F_{md}\right) \qquad (10)$$

$$T_e = \frac{3}{2}\left(\frac{p}{2}\right)\frac{1}{\omega_b}\left(F_{ds}i_{qs} - F_{qs}i_{ds}\right) \qquad (11)$$

$$T_e - T_L = J\left(\frac{2}{p}\right)\frac{d\omega_r}{dt} \qquad (12)$$

where d : direct axis,
   q : quadrature axis,
   s : stator variable,
   r : rotor variable,
   F_{ij} is the flux linkage ($i=q$ or d and $j=s$ or r),
   v_{qs}, v_{ds} : q and d−axis stator voltages,
   v_{qr}, v_{dr} : q and d−axis rotor voltages,
   F_{mq}, F_{md} : q and d axis magnetizing flux linkages,
   Rr : rotor resistance,
   Rs : stator resistance,
   X_{ls} : stator leakage reactance ($\omega_e L_{ls}$),
   X_{lr} : rotor leakage reactance ($\omega_e L_{lr}$),
   $X_{ml}^* : 1/\left(\frac{1}{x_m} + \frac{1}{x_{ls}} + \frac{1}{x_{lr}}\right)$,
   i_{qs}, i_{ds} : q and d−axis stator currents,
   i_{qr}, i_{dr} : q and d−axis rotor currents,
   p : number of poles,
   J : moment of inertia,
   T_e : electrical output torque,
   T_L(or T_l) : load torque,
   ω_e : stator angular electrical frequency,
   ω_b : motor angular electrical base frequency,
   ω_r : rotor angular electrical speed.

For a squirrel cage induction machine, as in the case of this paper, *vqr* and *vdr* in (3) and (4) are set to zero. An induction machine model can be represented with five differential equations as shown. To solve these equations, they have to be rearranged in the state-space form, In this case, state-space form can be achieved by inserting (5) and (6) in (1–4) and collecting the similar terms together so that each state derivative is a function of only other state variables and model inputs. Then, the modeling equations (1-4) of a squirrel cage induction motor in state-space become

$$\frac{dF_{qs}}{dt} = \omega_b \left[v_{qs} - \frac{\omega_e}{\omega_b} F_{ds} + \frac{R_s}{x_{ls}} \left(\frac{x_{ml}^*}{x_{lr}} F_{qr} + \left(\frac{x_{ml}^*}{x_{ls}} - 1 \right) F_{qs} \right) \right] \quad (13)$$

$$\frac{dF_{ds}}{dt} = \omega_b \left[v_{ds} + \frac{\omega_e}{\omega_b} F_{qs} + \frac{R_s}{x_{ls}} \left(\frac{x_{ml}^*}{x_{lr}} F_{dr} + \left(\frac{x_{ml}^*}{x_{ls}} - 1 \right) F_{ds} \right) \right] \quad (14)$$

$$\frac{dF_{qr}}{dt} = \omega_b \left[- \frac{(\omega_e - \omega_r)}{\omega_b} F_{dr} + \frac{R_r}{x_{lr}} \left(\frac{x_{ml}^*}{x_{ls}} F_{qs} + \left(\frac{x_{ml}^*}{x_{lr}} - 1 \right) F_{qr} \right) \right] (15)$$

$$\frac{dF_{dr}}{dt} = \omega_b \left[\frac{(\omega_e - \omega_r)}{\omega_b} F_{qr} + \frac{R_r}{x_{lr}} \left(\frac{x_{ml}^*}{x_{ls}} F_{ds} + \left(\frac{x_{ml}^*}{x_{lr}} - 1 \right) F_{dr} \right) \right] (16)$$

$$\frac{d\omega_r}{dt} = \left(\frac{p}{2J} \right) (T_e - T_L) \quad (17)$$

IV.   MATLAB/SIMULINK MODEL & SIMULATION RESULTS

Here simulation is carried out for two cases. In case I conventional three phase three level induction motor is simulated and in case II proposed multilevel drive is simulated.
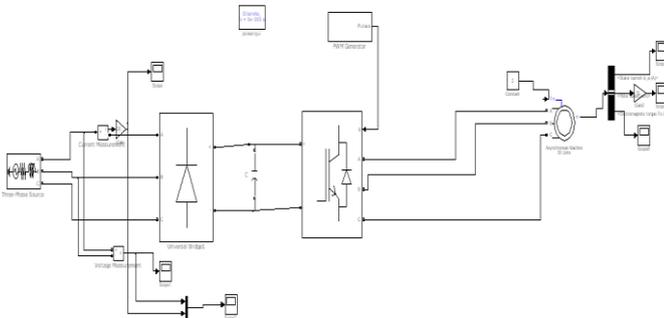
Fig. 6 Matlab/Simulink Model of Convention IM Drive

Fig. 6 shows the Matlab/Simulink model of conventional three phase three level induction motor drive. It consists of front end rectifier followed by three phase inverter.
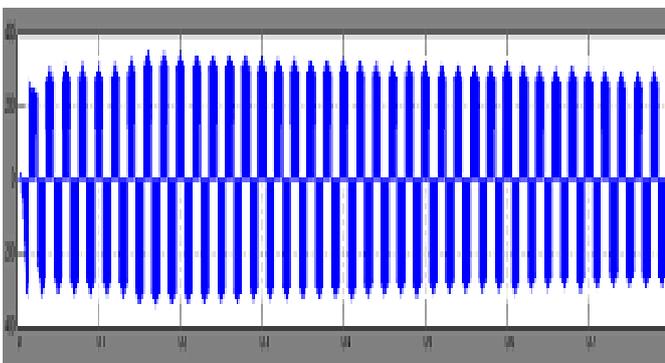
Fig. 7 Three Level output

Fig. 7 shows the three level output of the conventional inverter. Her switching frequency is taken as 1050 hz.

Fig.8 Stator Current, Speed and Motor Torque
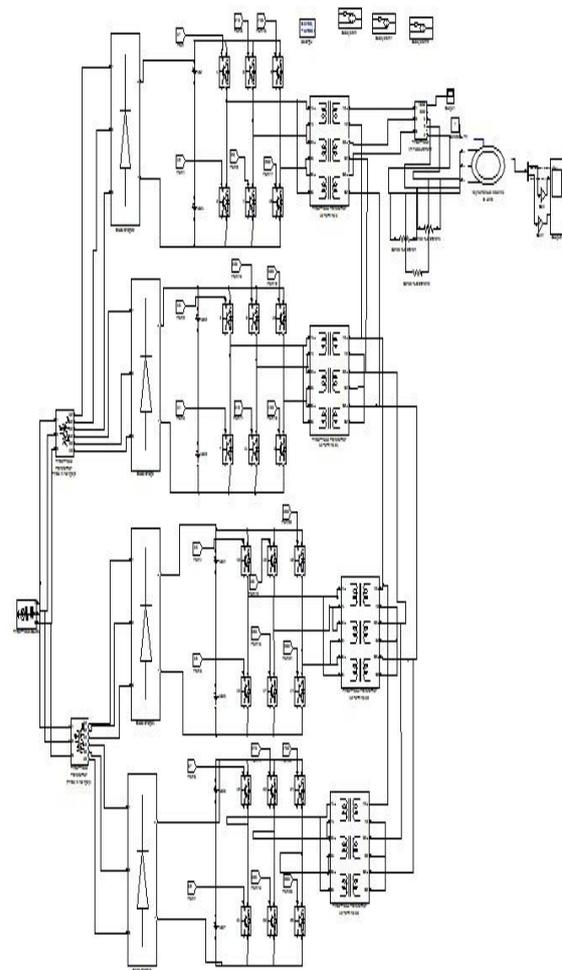
Figure.9 Block diagram of proposed circuit

Fig. 9 shows the block diagram of proposed series connected multilevel inverter fed induction motor drive. It consists of four inverters. Here we are using phase shifted carrier PWM.
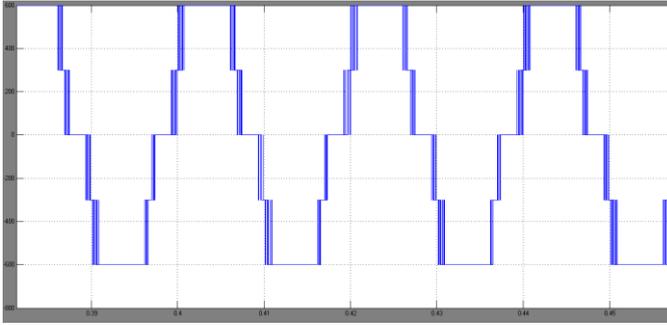
Fig. 10 Three Level output Inverter 1
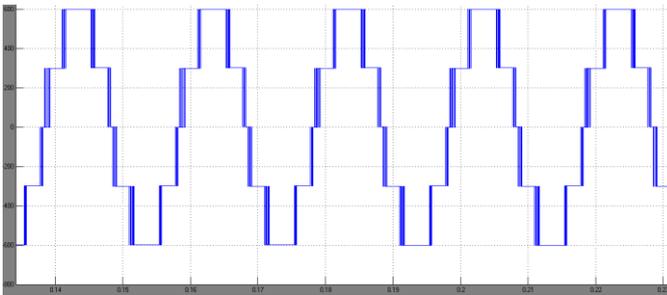
Fig. 11 Three Level output Inverter2
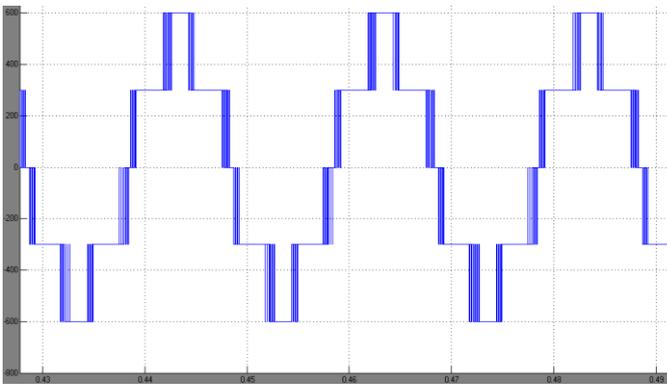
Fig. 12 Three Level output Inverter3
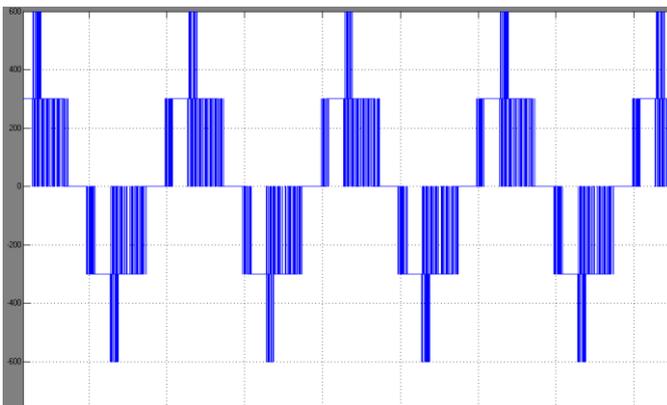
Fig. 13 Three Level output Inverter4

Fig10 to 13 shows the individual inverter outputs. From the figures it is clear that each output consists of only three levels.
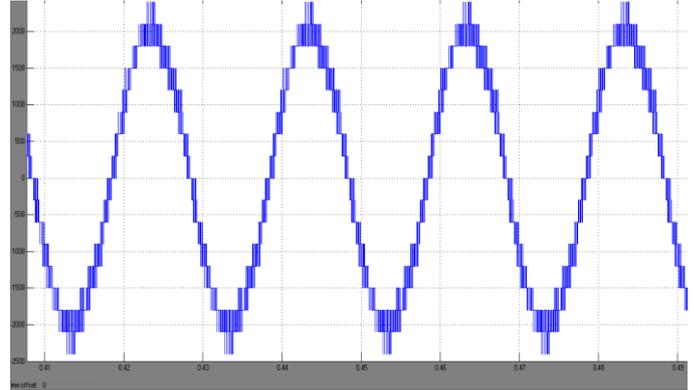
Fig. 14 Multilevel output
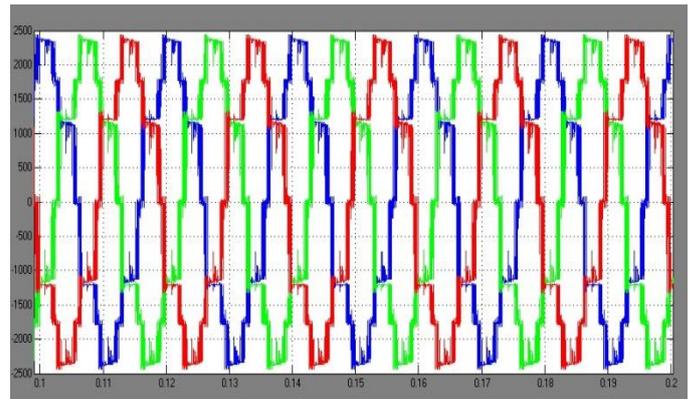
Figure.15.Multilevel output three phase

This waveform represents the output voltage of the three phase multilevel inverter.
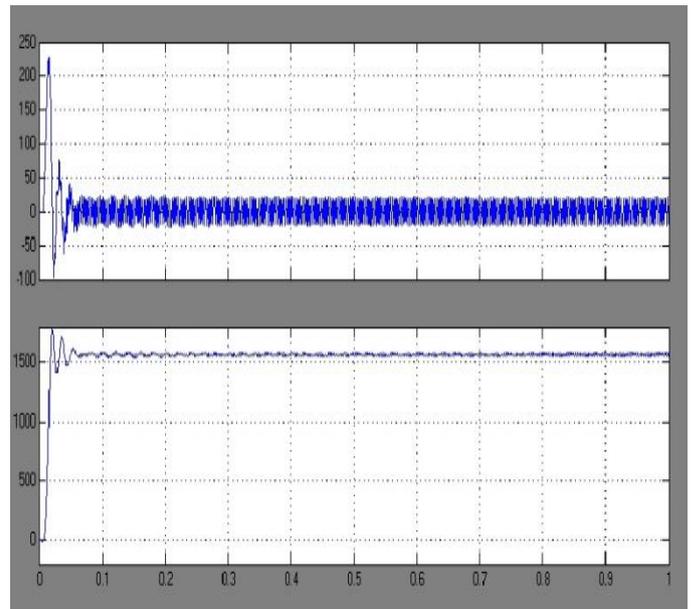
Figure.16Electromagnetic Torque and Speed curves of SQCIM

The first waveform represents the Electromagnetic Torque and rotor speed characteristics of the Squirrel cage Induction motor

V.   CONCLUSION

A series connection of three-level inverters has been proposed for a medium-voltage SQIM drive with increased voltage capacity. The topology ensured high-power operations with medium-voltage output having several voltage levels. The reduction in the ratings of the dc bus capacitor and reduced imbalance problems in the dc bus are some of the advantages of the proposed topology over the existing topologies. The disadvantage of the proposed topology is that it requires additional output transformers which introduce additional cost and losses. However, these transformers do not have complex underutilized windings like that required in cascaded H-bridge topologies. Finally a Matlab/Simulink model is developed and simulation results are presented.

VI.   REFERENCES

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