International Journal of Modern Engineering Research (IJMER)

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1125-1128 ISSN: 2249-6645

Error Tolerant Modified Booth Multiplier for Lossy Applications

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ABSTRACT

Multipliers are the fundamental arithmetic unit in multimedia and digital signal processing applications. The fixed width multipliers are used in those applications where we have to maintain a fixed format and allow a little accuracy loss of output data. In this paper we have proposed a low power technique for high speed modified booth multiplication. Even though modified booth multiplier reduces truncation error it consumes more power for the purpose and reduces speed. To reduce power consumption in truncation process we introduce error tolerant adder in modified fixed width Booth multiplier The ETA is able to ease the strict restriction on accuracy, and at the same time achieve tremendous improvements in both the power consumption and speed performance.

***Keywords*- Digital Signal Processing (DSP), Error tolerant adder, Fixed width multiplier, modified Booth multiplier, Signal Conditioning (SC Generator)**

I. INTRODUCTION

Multiplication is an important part of real-time digital signal processing (DSP) applications ranging from digital filtering to image processing. In these systems multipliers are always the fundamental arithmetic unit and they significantly influence the system's performance and power dissipation. Many application systems based on DSP, especially the recent next-generation optical communication systems, require extremely fast processing of a huge amount of digital data. Most of DSP applications such as fast Fourier transform (FFT) require additions and multiplications. Since the multipliers have a significant impact on the performance of the entire system, many high-performance algorithms and architectures have been proposed to accelerate multiplication.

In analog computations, generation of "acceptable" results is more important than totally accurate results [8]. Hence, by using error tolerance concept in design and test, it is able to develop results. To deal with high speed and low power circuits for analog computations, different types of multipliers have been studied. Multipliers based on word length reduction for multi-precision multiplication [5] showed that power reduction of 56% can be realized in case of 16 bit Wallace tree multipliers for 8 bit truncation. However, power reduction can be achieved only at the expense of precision which exceeds tolerance for minimum bit constants. As for the "low-error area-efficient fixed-width multipliers" [6], it may have an area improvement of 46.67% but has average error reaching 12.4%.

In this paper, the design of an Error Tolerant (ET) Modified Booth Multiplier is proposed to deal with this problem. It utilizes the concept of error tolerant addition [9] for accumulation of partial products bits of modified booth multiplier. Since the system that incorporates this circuit produces acceptable results, it is said to be error tolerant. Not all digital based applications can use error tolerant concept. In digital systems such as control systems, the correctness of the output signal is extremely important, and this doesn't allow the usage of the error tolerant circuit. However, for many Digital Signal Processing (DSP) systems that process signals relating to human senses such as hearing, sight, smell and touch, e.g., the image processing and speech processing systems, the error-tolerant circuits may be applicable [7]-[9].

II. ERROR TOLERANT ADDER

2.1.ERROR TOLERANT ADDITION

The commonly used terminologies in Error Tolerant addition are overall error and accuracy. They are defined by the equations discussed below.

Overall error (OE): $OE=|Rc-Re|$ (1)

where Re is the result obtained by the Error tolerant addition technique, and Rc is the correct result (all the results are represented as decimal numbers).

Accuracy (ACC): In the case of the error tolerant design, the accuracy of an addition process is used to indicate how "correct" the output of an adder is for a particular input. Its value ranges from 0-100%.

$$ACC\%=(1-(OE/Rc)) \times 100 \quad (2)$$

In the conventional adder circuit, the delay is mainly due to the carry propagation from the least significant bit (LSB) to the most significant bit (MSB). Glitches in the carry propagation also cause significant power dissipation. Therefore, if the carry propagation can be eliminated or curtailed, a great improvement in speed performance and power consumption [8] can be achieved. This new addition arithmetic can be illustrated via an example shown below.

In error tolerant addition technique, we first split the input operands into two parts: an accurate part that includes higher order bits and the inaccurate part that consists of lower order bits. The length of each part need not necessary be equal. The addition process starts from the middle i.e., starting point in Fig 1 towards the two opposite directions at the same time.

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1125-1128 ISSN: 2249-6645

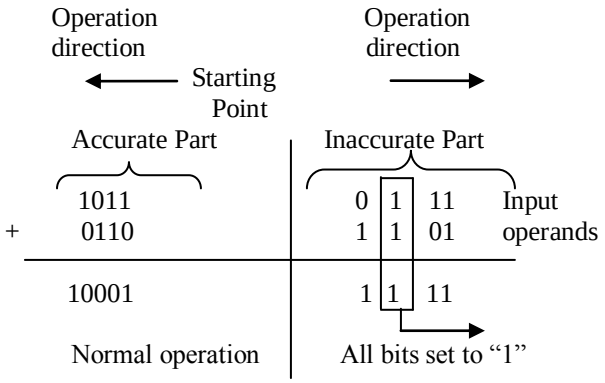

Fig 1. Arithmetic Procedure of Error Tolerant Adder

In the example of Fig. 1, the two 8-bit input operands, A="10110111" (183) and B= "01101101" (109), are divided equally into 4 bits each for the accurate and inaccurate parts. The addition of the higher order bits (accurate part) of the input operands is carried from right to left (LSB to MSB) and normal addition method is applied. This is to preserve its correctness since the higher order bits play a more important role than the lower order bits. The lower order bits of the input operands (inaccurate part) require a special addition mechanism. No carry signal will be considered at any bit position to eliminate the carry propagation path. To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted, and as follows: 1) check every bit position from left to right (MSB to LSB); 2) if both input bits are "0" or different, normal one-bit addition is performed and the operation proceeds to next bit position; 3) if both input bits are "1," the checking process stopped and from this bit onward, all sum bits to the right are set to "1." The addition mechanism described can be easily understood from the example. For the addition of the MSB part in modified booth multiplication we have adopted this technique.

The block diagram of the Error Tolerant adder that adapts to our proposed addition arithmetic is shown in Fig. 2. This most straightforward structure consists of two parts: an accurate part and an inaccurate part. The accurate part is constructed using conventional adder such as the Ripple-Carry Adder (RCA). The carry-in of this accurate part adder is connected to ground. The inaccurate part constitutes two blocks: a carry-free addition block and a control block. The control block is used to generate the control signals to determine the working mode of the carry-free addition block. In addition, the Least Significant Bit (LSB) of the multiplier (bit B_0) is used as control bit for both accurate part and inaccurate part of the proposed adder. For B_0 is one, the adder cells performs normal addition operation. For B_0 equals to zero, the adder cells are brought into OFF state with NMOS and PMOS transistor brought into open state and the line from supply to ground is cut off , thus minimizing leakage power dissipation. Based on the proposed methodology, an 8-bit Error tolerant adder is designed by considering 4 bits in accurate part and 4 bits in inaccurate part.

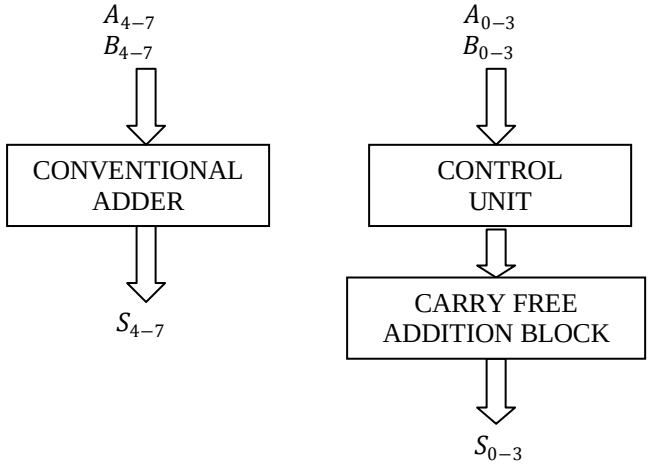

Fig 2. Block Diagram of Error Tolerant Adder

2.2. DESIGN OF THE INACCURATE PART

The inaccurate part is the most important section in the proposed ETA because it determines the accuracy, speed performance, and power consumption of the adder. The inaccurate part consists of two blocks: the carry free addition block and the control block. The carry-free addition block is designed using 4 modified XOR gates to generate a sum bit individually for LSBs. The block diagram of the carry free addition block is shown in Fig 3. In the modified XOR gate, six extra transistors are added to the conventional XOR gate. CTL is the control signal coming from the control block and is used to set the state of transistors. As the line from supply to ground is open during high impedance state, the chances of leakage power dissipation is minimized.

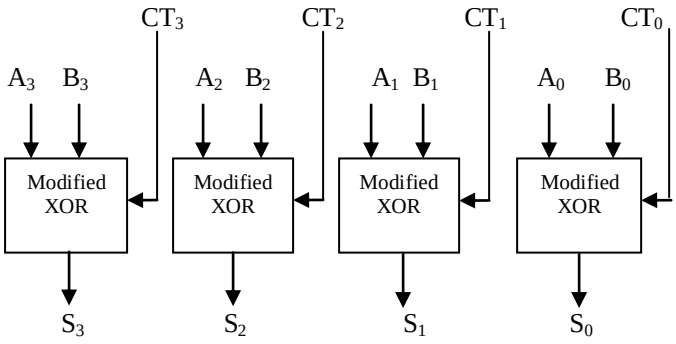

Fig 3. Architecture of Carry Free Addition Block

The function of the control block [9] is to find the first bit position when both input bits are"1," and to set the control signal CTL to high at this position as well as those to its right up to LSB. As the proposed adder has 4 bits in inaccurate part, the control block is designed with 4 control signal generating cells (CSGCs) and each cell generates a control signal for the modified XOR gate in the corresponding bit position of carry-free addition block. Two types of CSGC, labelled as type I and II are designed to develop the control signals. The control signal generated by the leftmost cell in each group is connected to the input of the leftmost cell in the adjacent group. These extra connections allow the propagated high control signal to "jump" from one group to another [8].

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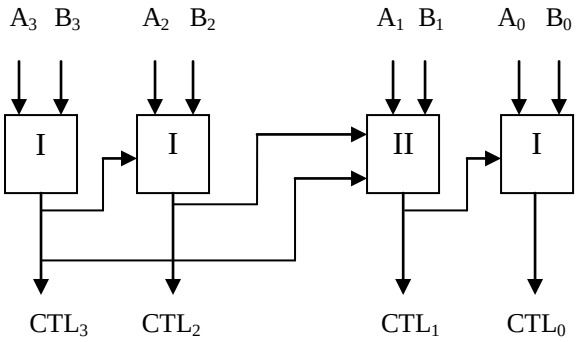

Fig 4. Overall architecture of Control Block

III. PROPOSED ERROR TOLERANT MODIFIED BOOTH MULTIPLIER

In case of existing modified booth multiplier the partial product matrix can be segmented into MP (Major product) and LP (Lower product), where LP is further divided into LP_{major} and LP_{minor}. In the fixed-width modified Booth multiplier, only the partial product bits in LP_{minor} are removed and the carry value propagated from LP_{minor} toLP_{major} must be estimated by a simple circuit to compensate for the truncation error. The final partial product matrix developed by using existing modified fixed width booth multiplier [11] is shown in Fig 5. Even though this increases accuracy but it reduces speed of operation as well as increase power consumption.

In proposed error tolerant booth multiplier for the addition of the partial product obtained we apply the error tolerant adder. We are applying error tolerant adder in modified booth multiplier for lossy applications because we need only "good enough" results not accurate results. By applying error tolerant addition technique we divide the partial products into accurate and inaccurate part. Since it is a fixed width multiplier we append zeros to make the partial products rows of equal length. Here length is 16 bit. For the addition of the partial product bits method described in Section II is used. As Error tolerant adder used for accumulation of partial products involves carry free addition, the delay due to carry propagation can be reduced to a greater extent.

The major components of the proposed design are (i) Modified Booth Encoder (ii) SC Generator and (iii) Error tolerant adder. Fig 6.shows the block diagram for the proposed design. First the values of partial product bits are found out using modified booth encoders and carry value propagated from LP_{minor} toLP_{major}. Then the outputs of modified Booth encoders are taken as inputs and then generates the approximate carry value, is derived to reduce the truncation error and make the error distribution as symmetric and centralized as possible using SC generator [11]. For the addition of the partial product bits we use the error tolerant adder to improve power dissipation as well as speed. At this stage 16 bit output is produced. To further improve the constraints we truncate the output obtained i.e., P to 8 bits. By this technique we can improve power as well as speed.

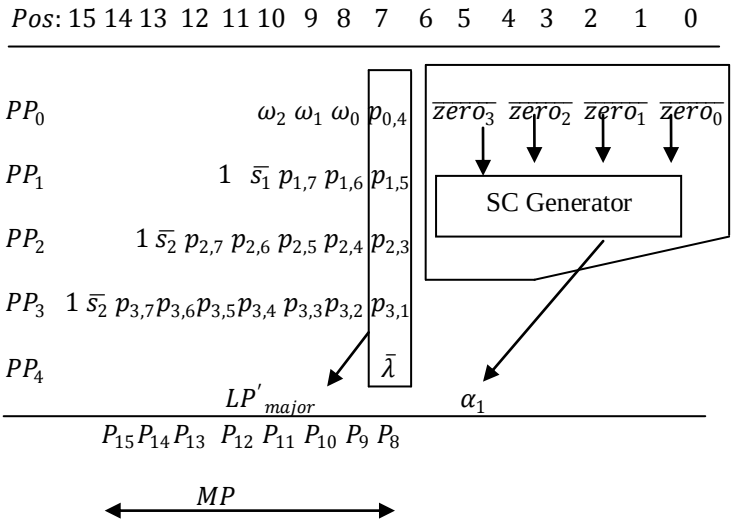

Fig. 5. Final partial product matrix of fixed-width modified Booth multiplier for n=8

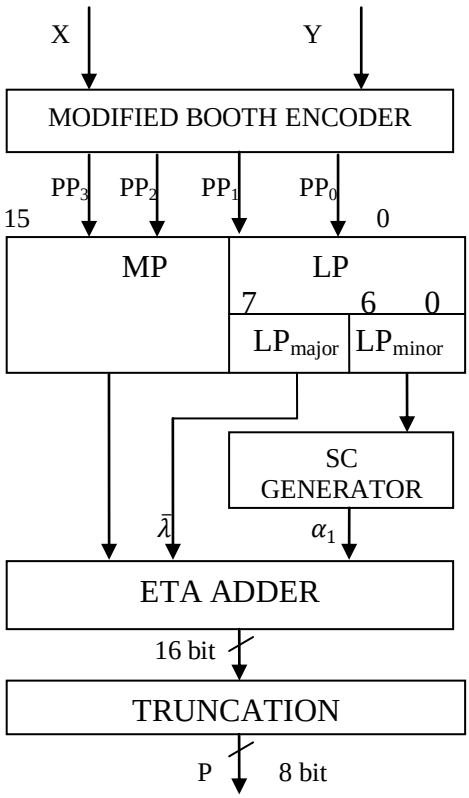

Figure 6. Generalised Arcitecture for ET modified booth multiplier

IV. RESULTS

The proposed Error Tolerant modified Booth multiplier is designed in XILINX 8.1 using VHDL code and simulated using Modelsim5.5.

The power dissipation and delay comparison of the booth multipliers for input data are shown in Table 1.

Reduction in power dissipation is mainly due to the reduced number of switching activities in the proposed Error Tolerant modified booth multiplier. The blocks of Error tolerant adder are brought into high impedance state during

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zero bit value of multiplier, due to that a constant saving in leakage power is achieved.

Parameter	Convetional Booth Multiplier	Modified Booth Multiplier Using SC generator	Error tolerant Modified Booth Multiplier
Area (No. of gates)	2021	835	461
Delay	95ns	65ns	50ns
Power	130mW	89mW	86mW

Table 1. Comparison of (a) Power and (b) Delay of Modified booth multiplier proposed ET modified booth multipliers

Delay of proposed Error Tolerant modified multiplier decreases by 10% when compared to the Modified Booth Multiplier. The reduced delay of proposed multiplier is due to the elimination of carry propagation in inaccurate part of the Error Tolerant adder used**.**

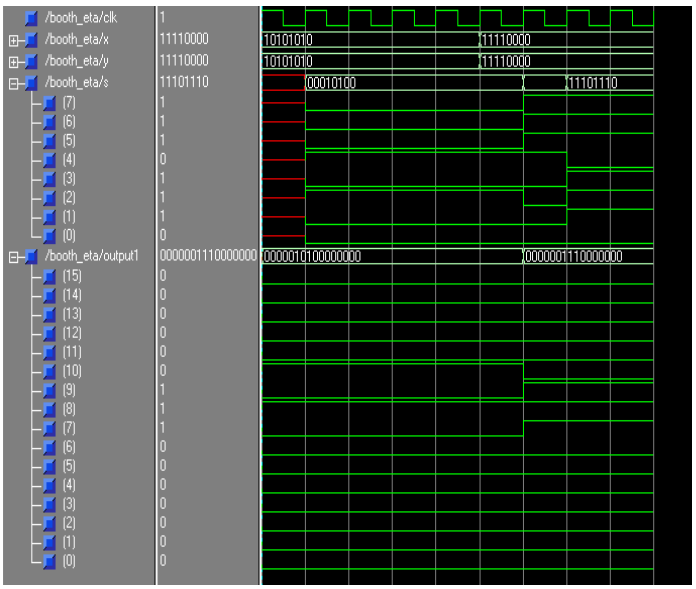

Figure 7. Output obtained for High speed error tolerant modified booth multiplier using Modelsim5.5.

V. CONCLUSION

In this paper, the error tolerance arithmetic is used in design of modified booth multiplier. The proposed multiplier reduces a certain amount of accuracy for significant power saving and performance improvement. Comparisons with conventional multipliers showed that the proposed Error tolerant modified booth multiplier reduces area i.e., number of gate count and improves speed of performance. The applications of the Error Tolerant Multiplier are in those areas where there is no strict restriction on accuracy or when high-speed performance is more important compared to accuracy. Some applications are in Digital Image processing and DSP architectures for cell phones, laptops etc.

REFERENCES

[1] M. A. Breuer, "Intelligible test techniques to support error-tolerance," in Proc. Asian Test Symp., Nov. 2004, pp. 386–393.

[2] K.J. Cho, K.C. Lee, J.G. Chung, and K.K.Parhi, "Design of low- error fixed-width modified Booth multiplier," IEEE Trans. Very Large Scale Integer. Syst., vol.12, no.5, pp. 522-531, May 2004

[3] I.S.Chong and A. Ortega, "Hardware testing for error tolerant multimedia compression based on linear transforms," in Proc. Defect and Fault Tolerance in VLSI Syst. Symp., 2005, pp. 523–531.

[4] F.Elguibaly, "A fast papallel multiplier- accumulator using the modified Booth Algorithm," IEEE Trans. Circuits Syst.ii, Reg. Papers, vol. 47, no.9,pp.902-908, Sep. 2000

[5] International Technology Roadmap for Semiconductors . Available: http://public.itrs.net/

[6] J.M.Jou, S.R.Kuang, and R.D.Chen," Design of low-error fixed –width multipliers for DSP applications," IEEE Trans. Circuits Syst.II, Exp.Briefs, vol.46,no.6, pp.836-842, June 1999.

[7] S.S. Kidambi, F.El-Guibaly, and A.Antoniou, " Area-efficient multipliers for digital signal processing applications," IEEE Trans. Circuits Syst.II, Exp. Briefs, vol. 43, no.2, pp. 90-94, Feb.1996

[8] A.B.Melvin, "Let's think analog," in Proc. IEEE Comput. Soc. Annu. Symp. VLSI, 2005, pp. 2–5.

[9] A.B.Melvin and Z. Haiyang, "Error-tolerance and multi-media," in Proc. 2006 Int. Conf. Intell. Inf. Hiding and Multimedia Signal Process., 2006, pp. 521–524.

[10] L.D.Van and C.-C. Yang, "Generalized low-error area efficient fixed width multipliers," IEEE Trans. Circuits Syst. I, Reg. Papers, vol. 25, no. 8, pp. 1608–1619, Aug. 2005.

[11] Jiun-Ping Wang, Shiann-Rong Kuang, and Shish-Chang Liang, "High-Accuracy Fixed Width Modified Booth Multipliers for Lossy Applications" IEEE Trans. on VLSI Systems, vol. 19, no. 1,pp 52-60, January 2011.