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The Circuits Design using Dual-Rail Clocked Energy Efficient Adiabatic Logic

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ABSTRACT

In this paper, the design of circuits using adiabatic logic and sequential circuits based on the newly proposed Energy efficient adiabatic Logic (EEAL) is presented. EEAL uses dual sinusoidal source as supply-clock. This paper proposes a positive feedback adiabatic logic (PFAL), two-phase clocked adiabatic static CMOS logic (2PASCL) and proposed adiabatic logic circuit that utilizes the principles of adiabatic switching and energy recovery compare than CMOS. 2PASCL has switching activity that is lower than dynamic logic. The power consumption of proposed adiabatic logic becomes lower compare than CMOS. Also design NAND logic gates on the basis of the 2PASCL topology and proposed NAND gate. Comparison has shown a significant power saving to the extent of 70% in case of proposed technique as compared to CMOS logic and NAND gate in 10 to 200MHz transition frequency range. The simulation results are analyzed at 180nm technology to show the technology dependence of the design. The proposed design of CMOS logic and NAND gate is better suitable for the low power VLSI applications.

Keywords: **Adiabatic logic, adiabatic switching, Energy recovery, Low Power applications, Portable Applications, two phase clocked.**

1.INTRODUCTION

Higher power and energy dissipation in high performance systems require more expensive packaging and cooling technologies, increase cost, and decrease system reliability. Nonetheless, the level of on-chip integration and clock frequency will continue to grow with increasing performance demands, and the power and energy dissipation of high-performance systems will be a critical design constraint [12].

The main source of power dissipation in these high performance battery-portable digital systems running on batteries such as note-book computers, cellular phones and personal digital assistants are gaining prominence. For these systems, low power consumption is a prime concern, because it directly affects the performance by having effects on battery longevity. In this situation, low power VLSI design has assumed great importance as an active and rapidly developing field.

Another major demand for low power chips and systems comes from the environmental concerns. Modern offices are now furnished with office automation equipments that consume large amount of power [13]. A study by American Council for an Energy-Efficient Economy estimated that office equipment account for 5% for the total US commercial energy usage in 1997 and could rise to 10% by the year 2004 if no actions are taken to prevent the trend [14].

The idea behind the circuit is built upon the basic diode based circuit proposed in [1] and [2]. In this paper, we propose a two-phase clocked adiabatic static CMOS logic (2PASCL) [10] circuit to achieve low power consumption; we also compare its power consumption with that of a conventional CMOS circuit. A novel method for reducing the power dissipation in a 2PASCL circuit involves the design of a charging path without diodes. In such a case, current flows only through the transistor during the charging. Thus, a 2PASCL circuit is different from other diode-based adiabatic circuits in which current flows through both the diode and transistor. By using the aforementioned 2PASCL circuit, we can achieve high output amplitudes and reduce power dissipation. In addition, in order to minimize the dynamic power consumption in this circuit, we apply a split-level sinusoidal driving voltage.

In conventional CMOS circuits, power dissipation can be minimized by reducing the supply voltage, node capacitance, and switching activity [1, 2] to a certain extent but very nascent adiabatic computing has appeared as a naturally acceptable and very practical solution in low power VLSI systems. Several adiabatic logic families based on energy recovery principle [3-5] where all charge recovered back to power supply without heat generation have been proposed & implemented earlier. The following mathematical analysis based on time period (T), Stored Charge ($C_L V_{dd}$), Load capacitance C_L and channel resistance R is sufficient to have a deeper look on it.

$$E_{diss} = (RC_L/T)C_L Vdd^2 \quad (1)$$

Theoretically, it is possible to reduce the power dissipation by extending the switching time.

The circuit uses a two phase clocked split-level sinusoidal power supply to reduce the voltage difference between the current-carrying electrodes to reduce the power consumption.

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2. ADIABATIC SWITCHING

Adiabatic switching is commonly used to minimize energy loss during the charge/discharge cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation [16]. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time varying voltage source instead of a fixed voltage supply. Here, the load capacitance (C_L) is charged by a constant current source (I). In conventional CMOS logic we use constant voltage source to charge the load capacitance [2]. Here, R is the on-resistance of PMOS network. A constant charging current corresponds to a linear voltage ramp. Assume the capacitor voltage zero initially.

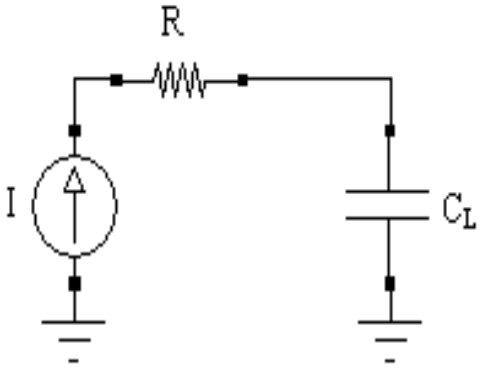

Fig1: Adiabatic logic circuit

The voltage across the switch = IR
P (t) in the switch = I^2R
Energy during charge E = $(I^2R)T$
Also Q □□C_LV_{dd} , I □□C_LV_{dd} /T
E= $(I^2R)T= (RC_L/T)C_LV_{dd}^2$
Where, E [3] is the energy dissipated during charging time,
Q is the charge transferred to the load,
C is the value of the load capacitance,
R is the on-resistance of the PMOS switch,
V is the final value of the voltage at the load,
T is the charging time.
Theoretically, when driving voltage (Va) switching time (T) from 0 V to V_{dd} is long, the energy dissipation is nearly zero. When Va changes from HIGH to LOW in the pull- down network, discharging via the NMOS transistor occurs. From equation (1), it is observed that when energy dissipation is minimized by decreasing the rate of switching transition, the system draws some of the energy that is stored in the load capacitor during the current subsequent computational steps. Systems based on above-mentioned technique for charge recovery is not necessarily reversible [8], [9].

3. CMOS INVERTER

Power dissipation in conventional CMOS circuits primarily occurs during the device switching. When the logic level in the system is "1," there is a sudden flow of current through R. $Q = C_LV_{dd}$ is the charge supplied by the positive power supply rail for charging CL to the level of Vdd. Hence, the energy drawn from the power supply is $Q \cdot V_{dd} = C_LV_{dd}^2$ [4]. By assuming that the energy drawn from the power supply is equal to that supplied to CL, the energy stored in C_L is said to be one-half the supplied energy, i.e., Estored = $(1/2)C_LV_{dd}^2$.
The remaining energy is dissipated in R. The same amount of energy is dissipated during discharging in the nMOS pull-down network when the logic level in the system is "0." Therefore, the total amount of energy dissipated as heat during charging and discharging is

$$E_{total} = E_{charge} + E_{discharge} = 0.5\, C_LV_{dd}^2 + 0.5\, C_LV_{dd}^2 = C_LV_{dd}^2 \quad (2)$$

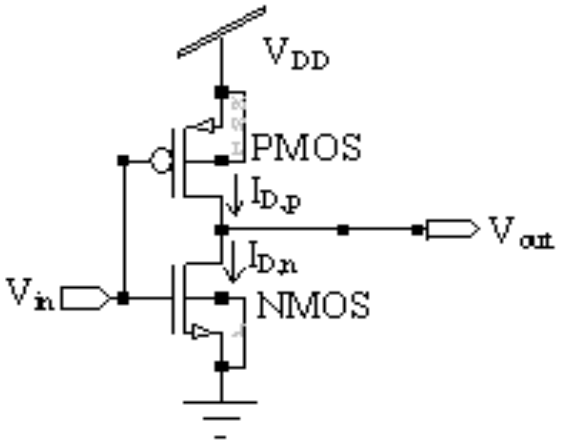

Fig2: CMOS inverter circuit

4. PFAL

The structure of PFAL logic [15], [16] is shown in figure 3. Two n-trees realize the logic functions. This logic family also generates both positive and negative outputs. The two major differences with respect to ECRL are that the latch is made by two PMOSFETs and two NMOSFETs, rather than by only two PMOSFETs as in ECRL, and that the functional blocks are in parallel with the transmission PMOSFETs. Thus the equivalent resistance is smaller when the capacitance needs to be charged. The ratio between the energy needed in a cycle and the dissipated one can be seen in figure 3. During the recovery phase, the loaded capacitance gives back energy to the power supply and the supplied energy decreases.
The partial energy recovery circuit structure so called Positive Feedback Adiabatic Logic (PFAL) [6], has good robustness against technological parameter variations [7], [8]. It is a dual rail circuit; the core of all the PFAL circuit is adiabatic amplifier, a latch made up by the two PMOS and two NMOS that avoids a logic level degradation on the output nodes. The two n-tree release the logic functions. The functional blocks are in parallel with P-MOSFETs and form a transmission gate.

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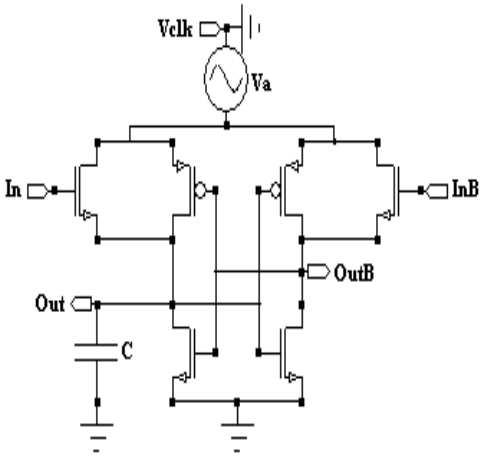

Fig3: PFAL Logic Circuit

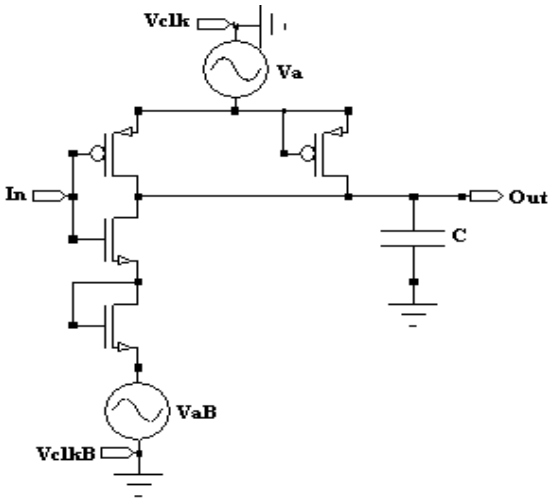

Fig4: 2PASCL Logic Circuit

5.2PASCL

Figure 4 shows a circuit diagram of Two-Phase Adiabatic Static Clocked Logic (2PASCL) inverter. A double diode circuit is used, where one diode is placed between the output node and power lock, and another diode is adjacent to the NMOS logic circuit and connected to the other power source [10]. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous if the signal nodes are preceded by a long chain of switches.

The circuit operation is divided into two phases: evaluation and hold. In the evaluation phase, Va swing up and VaB swings down. On the other hand, in the hold phase, VaB swings up and Va swings down. Let us consider the inverter's logical circuit demonstrated in Figure 7. The operation of the 2PASCL inverter is explained as follows.

1) Evaluation phase:

a) When the output node Y is LOW and the PMOS tree is turned ON, C_L is charged through the PMOS transistor, and hence, the output is in the HIGH state.

b) When node Y is LOW and NMOS is ON, no transition occurs.

c) When the output node is HIGH and the PMOS is ON, no transition occurs.

d) When node Y is HIGH and the NMOS is ON, discharging via NMOS and D2 causes the logic state of the output to be "0" [17].

2) Hold phase:

a) When node Y is LOW and the NMOS is ON, no transition occurs.

b) At the point when the preliminary state of the output node is HIGH and the PMOS is ON, discharging via D1 occurs.

6. PROPOSED ADIABTIC LOGIC INVERTER

Adiabatic switching is commonly used to minimize energy loss during the charge/discharge cycles. During the adiabatic switching, all the nodes are charged/discharged at a constant current to minimize energy dissipation. As opposed to the case of conventional charging, the rate of switching transition in adiabatic circuits is decreased because of the use of a time varying voltage source instead of a fixed voltage supply.

Hence, if I is considered as the average of the current flowing to C_L, the overall energy dissipated during the transition phase can be reduced in proportion to

$$I^2RTp = (C_L V_{dd}/ Tp)^2 RTp = (RCL/Tp) C_L V_{dd}^2 \quad (3)$$

Theoretically, during adiabatic charging, when Tp, the time for the driving voltage Va to change from 0 V to Vdd is long, energy dissipation is nearly zero.

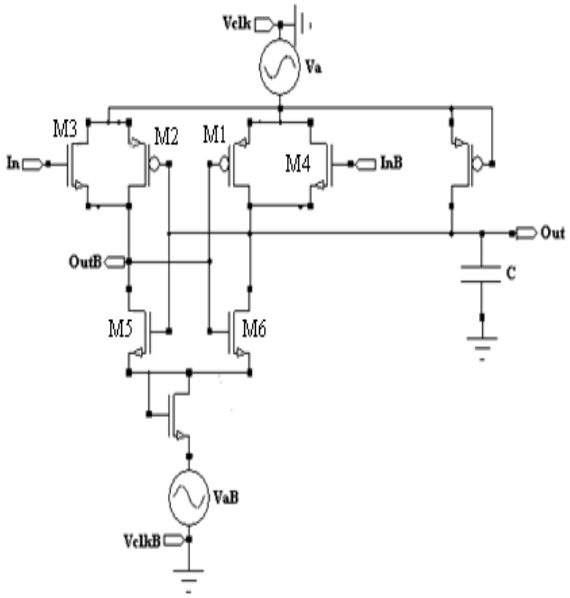

Fig5: Proposed adiabatic logic inverter circuit

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The basic inverter circuit is shown in above figure of this circuit is an adiabatic amplifier, a latch made by the two PMOS M1 and M2 and two NMOS M5 and M6, that avoids the logic level degradation at Out and Out, the logic circuit M3 and M4 are in parallel with M1 and M2 and forms transmission gate [1]. This circuit uses two-phase split level sinusoidal power supplies which are denoted as Va and VaB, where Va & VaB can vary from 1.3 to 1.6V & 0.3 to 0V respectively.

The circuit operates in two phases, evaluation and hold, in evaluation phase, Va swings up and VaB swings down, and in hold phase, VaB swings up and Va swings down. Let us assume, during evaluation phase the input (In) is high and input (InB) goes low accordingly, consequently M3 is conducting and output (OutB) follows the power supply Va, and at the same time M1 gets turned ON by output (Out) and thus reduces the charging resistance. Being in parallel with M3 and during hold phase, charge stored on the load capacitance C_L flows back to power supply through M1. So that power dissipation is reduced. The proposed circuit uses two MOS diodes, one is connected to Out and Va and other diode is connected between common source of M5- M6 and other power supply VaB, Both the MOS diodes are used to increase the discharging rate of internal nodes.

7. DIODE IS ADJACENT TO THE PMOS LOGIC

The proposed circuit uses one MOS diode, which is connected to Out and Va at PMOS logic, the MOS diode is used to increase the discharging rate of internal nodes.

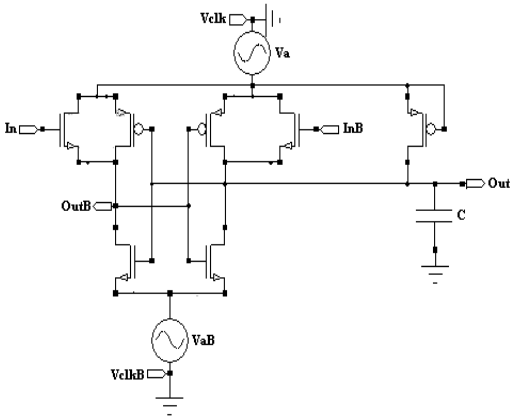

Fig6: Diode is adjacent to the PMOS logic

8. DIODE IS ADJACENT TO THE NMOS LOGIC

The proposed circuit uses one MOS diode, which is connected between common source of M5-M6 and other power supply VaB at NMOS logic, the MOS diode is used to increase the discharging rate of internal nodes.

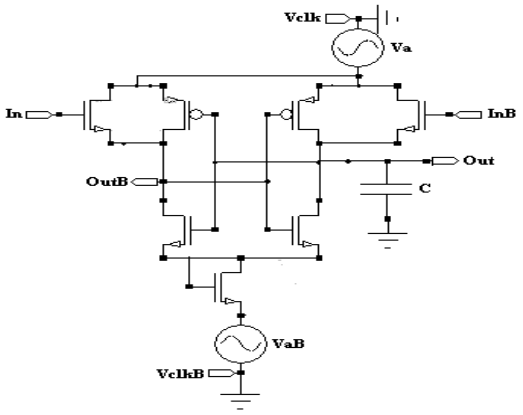

Fig7: Diode is adjacent to the NMOS logic

9. DESIGN AND SIMULATION OF A TWO-INPUT NAND GATE

(i) TWO-INPUT CMOS NAND GATE

The next basic cell to consider is the CMOS-based Two-Input NAND Gate, designed and simulated in the 180nm CMOS Technology and with a load capacitances are vary. The minimum sized NMOS and PMOS transistors have been used for the transient simulations [9].

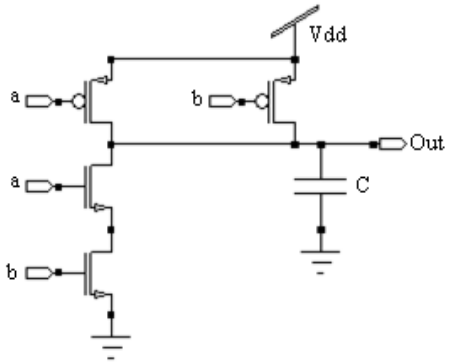

Fig8: Two-input CMOS NAND gate

(ii) TWO-INPUT CMOS NAND GATE BASED 2PASCL

Figure 9 shows a circuit diagram of Two-Phase Adiabatic Static Clocked Logic (2PASCL) inverter. A double diode circuit is used, where one diode is placed between the output node and power lock, and another diode is adjacent to the NMOS logic circuit and connected to the other power source [10]. Both the MOSFET diodes are used to recycle charges from the output node and to improve the discharging speed of internal signal nodes. Such a circuit design is particularly advantageous if the signal nodes are preceded by a long chain of switches.

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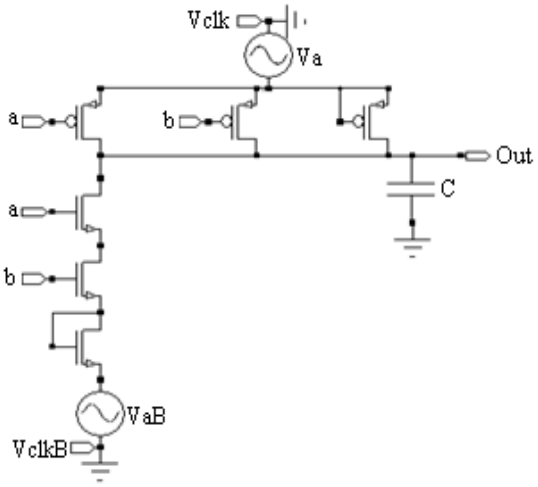

Fig9: 2PASCL NAND gate

(iii) PROPOSED ADIABATIC NAND GATE

In this circuit we use two diodes at PMOS and NMOS logic which shown in below fig10 and are used to increase the discharging rate of internal nodes. The circuit operates in two phases, evaluation and hold, in evaluation phase, Va swings up and VaB swings down, and in hold phase, VaB swings up and Va swings down [11].

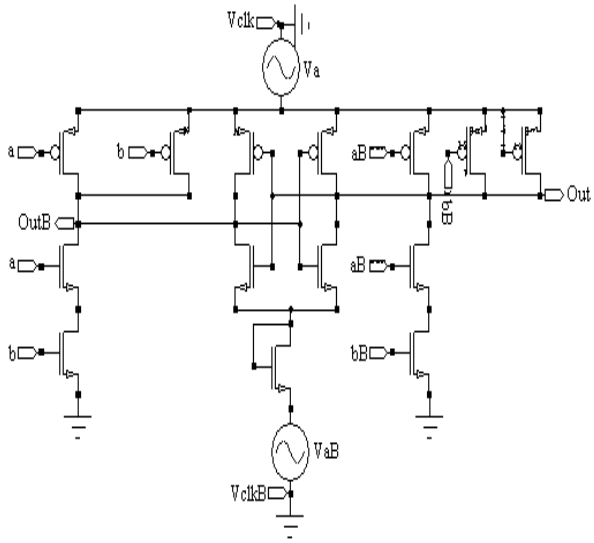

Fig10: Proposed NAND gate

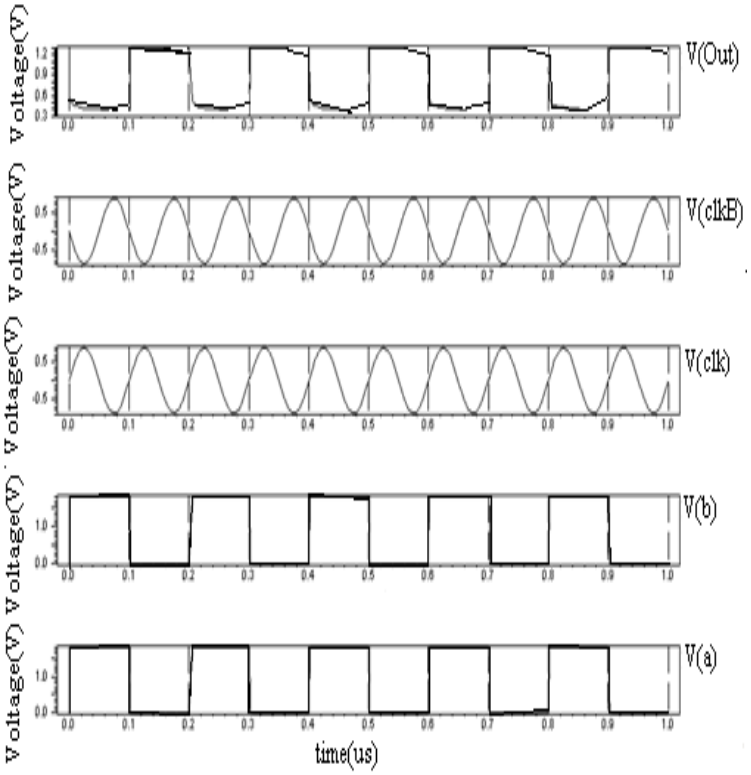

Fig11: Input and Output waveforms for 2PASCL NAND gate

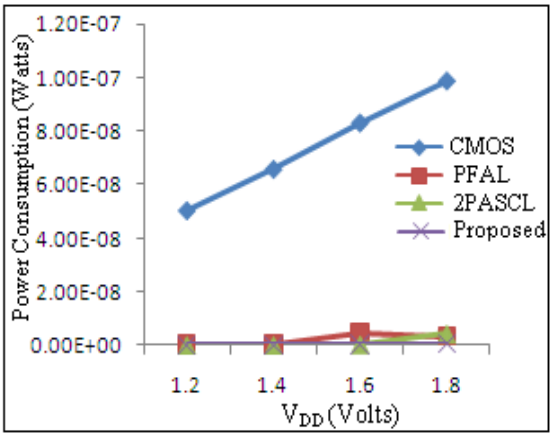

Fig12 Power Consumption comparison of proposed inverter vs CMOS at power supply

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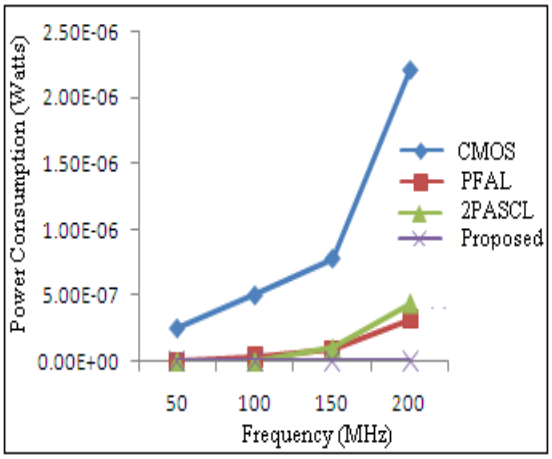

Fig13 Power Consumption comparison of proposed inverter vs CMOS at frequency

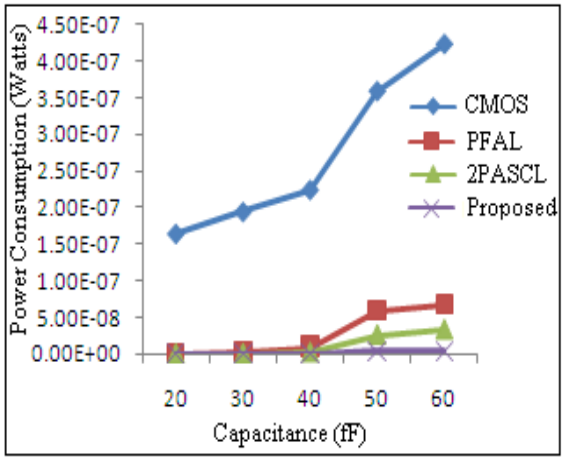

Fig14 Power Consumption comparison of proposed inverter vs CMOS at capacitance

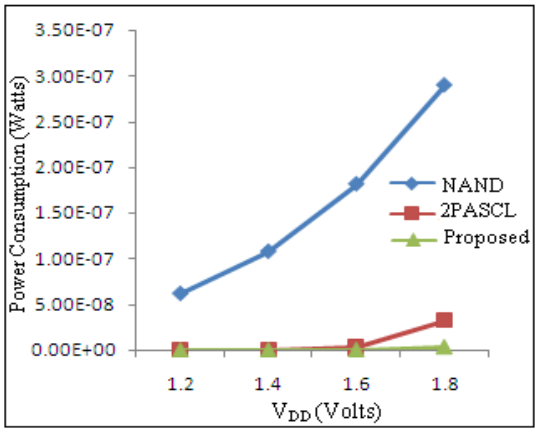

Fig15 Power Consumption comparison of proposed NAND vs NAND at power supply

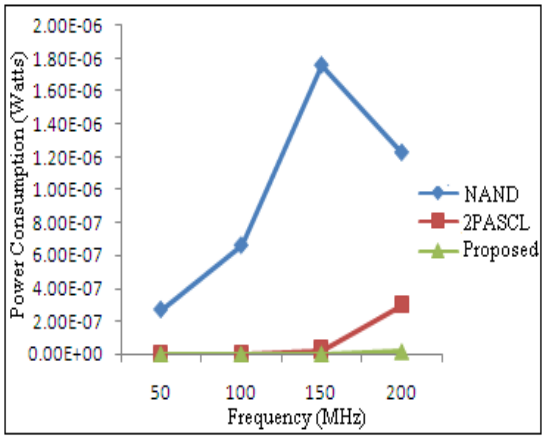

Fig 16 Power Consumption comparison of proposed NAND vs NAND at frequency

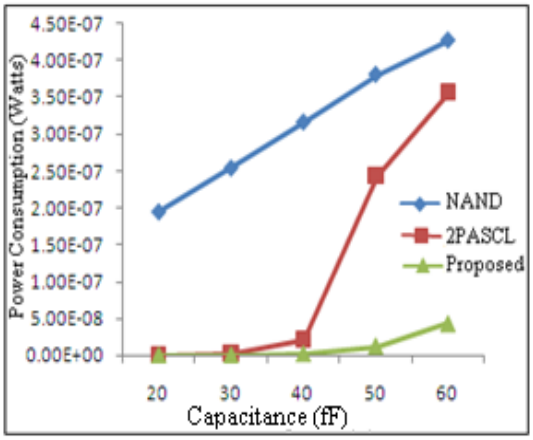

Fig17 Power Consumption comparison of proposed NAND vs NAND at capacitance

In this section, we will not examine the topology and functionality of proposed inverter & 1-bit full adder. The simulation is performed using a SPICE circuit simulator at 180nm technology node & 1.8 V standard CMOS process. The Proposed circuit width *W* & *L* of the NMOS and PMOS logic gates were 600n and 180n respectively. Whereas the length and width of MOS diode D2 is 40 µm beside a load capacitance C_L of 0.05pF connected at the output node. Above figure shows the simulated waveforms of Proposed Adiabatic logic inverter, in which upper most waveform shows the input, and below two waveforms are sinusoidal power clock and compliment of that power clock, last two waveforms are output and compliment of output respectively.

10. CONCLUSION

Simulation results obtained from the proposed inverter and NAND gate has wide acceptance in low power VLSI regime at low frequency. The comparison of the proposed circuit with other traditional methodologies has proved that power consumption with the proposed logic is far less as compared to CMOS, PFAL and 2PASCL based technique. The simulation result show that power consumption of proposed

NAND is less compare than NAND, 2PASCL. The requirement for dual-rail signals and T-gates where single-rail signals and individual FET's could otherwise be used roughly doubles the area required for logic. With dual-rail signals, half of the circuit nodes will switch each cycle. From the results of simulation it has been observed that the replacement of diodes with switches controlled by power clock significantly reduces the power consumption of the adiabatic circuit.

ACKNOWLEDMENTS

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Prof. Singh is the senior fellow of IEEE and life member of IETE.

REFERENCES

[1] N. Waste and K. Eshraghian, Principle of CMOS VLSI Design: A System Prospective, 2nd ed. New York: Addison – Wesley, 1993.

[2] W. C. Athas, L. J. Svensson, J. G. Koller, et al., "Low-power digital systems based on adiabatic switching principles," *IEEE* Trans. On VLSI systems, 2(4), Dec. 1994, pp: 398-407.

[3] S. Samanta "Adiabatic Computing: A Contemporary Review," International conference on computers and devices for communication, Dec. 2009, pp. 1-4.

[4] J. Marjonen, and M. Aberg, "A single clocked adiabatic static logic – a proposal for digital low-power applications," J. VLSI signal processing, vol.27, no.27, Feb.2001, pp.253-268.

[5] M. Pedram, "Power minimization in IC design: principles of applications," ACM Transactions on Design automation of Electronic System, 1(1) Jan 1996, pp 53-56.

[6] A. Vetuli, S. Di Pascoli, and L.M. Reyneri, "Positive feedback in adiabatic logic, Electron.Lett"vol.32, Sept. 1996, pp.1867- 1869.

[7] A. Blotti, M. Castellucci, and R. Saletti, "Designing carry lookahead adders with an adiabatic logic," standard-cell library," in proc. 12th Int. Workshop PATMOS, Seville, Spain, Sept. 2002, pp. 118-127.

[8] E. Amirante, A. Bargagli-Stoffi, J. Fisher, G. Iannaccone, and D.Schmitt-Landsiedel, "Variations of the power dissipation in adiabatic logic gates." In proc. 11th Int. Workshop PATMOS, Yverdon-Les_Bains, Switzerland, Sept. 2001, pp. 7 – 10.

[9] Y. Takahashi, Y. Fukuta, T. Sekine and M. Yokoyama, "2PADCL: Two phase drive adiabatic dynamic logic CMOS logic." Proc. IEEE APCCAS, Dec. 2006, pp. 1486-1489.

[10] N. Anuar, Y. Takahashi, T. Sekine, "Two phase clocked adiabatic static CMOS logic," proc. IEEE SOCC 2009, Oct. 2009, pp. 83-86.

[11] S. Kang and Y. Leblebici, "Low Power CMOS Digital Logic Circuits", 3rd ed., Tata McGraw Hill, 2003.

[12] N. Anuar, Y. Takahashi, T. Sekine, "Two-Phase clocked adiabatic static CMOS logic and its logic family" Journal of semiconductor technology and science, vol 10, no. 1, Mar. 2010, pp. 1-10. 463.

[13] A. P. CHANDRAKASAN, S. SHENG, AND R. W. BRODERSEN, "Low Power CMOS Digital Design," *IEEE Journal of Solid-state Circuits*, Vol. 27, No. 04, pp. 473-484, April 1999.

[14] J. M. RABAEY, AND M. PEDRAM, "*Low Power Design Methodologies*," Kluwer Academic Publishers, 2002.

[15] Vetuli, A., Di Pascoli, S., Reyneri, L.M.: Positive feedback in adiabatic logic. Electronics Letters, Vol. 32, No. 20, Sep. 1996, pp. 1867ff.

[16] Atul Kumar Maurya, Ganesh Kumar, "Energy Efficient Adiabatic Logic for Low Power VLSI Applications" 2011 International Conference on Communication Systems and Network Technologies.

[17] Blotti, A., Di Pascoli, S., Saletti, R.: Sample Model for positive feedback adiabatic logic power consumption estimation. Electronics Letters, Vol. 36, No. 2, Jan. 2000, pp. 116-118.

[18] Y. Takahashi, Y. Fukuta, T. Sekine and M. Yokoyama, "2PADCL: Two phase drive adiabatic dynamic CMOS logic," *Proc. IEEE APCCAS*, pp. 1486–1489, Dec. 2006.