International Journal of Modern Engineering Research (IJMER)

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1273-1279 ISSN: 2249-6645

Investigations on Three Phase Five Level Diode Clamped Multilevel Inverter

C. R. Balamurugan[1], S. P. Natarajan[2], R. Bensraj[3]

[1]*Department of EEE, Arunai Engineering College,Tiruvannamalai, Tamilnadu, India*

[2]*Department of EIE, Annamalai University, Chidambaram, Tamilnadu, India*

[3]*Department of EEE, Annamalai University,Chidambaram, Tamilnadu, India*

ABSTRACT

Multilevel inverters have become more popular over the years in high power electric applications without use of a transformer and with promise of less disturbance and reduced harmonic distortion. This work proposes three phase five level Diode Clamped Multilevel Inverter (DCMLI) to simulate various modulating techniques for induction motor load. These Pulse Width Modulation (PWM) techniques include Carrier Overlapping (CO) strategy, Variable Frequency (VF) strategy, Phase Shift (PSPWM) strategy and Sub-Harmonic Pulse Width Modulation (SHPWM) i.e. Phase Disposition (PD) strategy, Phase Opposition Disposition (POD) strategy and Alternate Phase Opposition Disposition (APOD) strategy. The Total Harmonic Distortion (THD), V_{RMS} (fundamental), crest factor, form factor and distortion factor are evaluated for various modulation indices. Simulation is performed using MATLAB-SIMULINK. It is observed that PODPWM method provides output with relatively low distortion and COPWM is found to perform better since it provides relatively higher fundamental RMS output voltage for Induction Motor (IM) load.

Keywords: **CF, DCMLI, FF, PWM, THD, V_{rms}**

I. INTRODUCTION

In recent years, industry has begun to demand higher power equipment, which now reaches the megawatt level. Controlled AC drives in the megawatt range are usually connected to the medium-voltage network. Today, it is hard to connect a single power semiconductor switch directly to medium voltage grids. For these reasons, a new family of multilevel inverters has emerged as the solution for working with higher voltage levels. Depending on voltage levels of the output voltage, the inverters can be classified as two-level inverters and multi level inverters. The inverters with voltage level 3 or more are referred as multi level inverters. Multilevel inverters have become attractive recently particularly because of the increased power ratings, improved harmonic performance and reduced EMI emission that can be achieved with the multiple DC levels that are available for synthesis of the output voltage. Xiaoming Yuan and Ivo Barbi [1] proposed fundamentals of a new diode clamping multilevel inverter. Bouhali et al[2] developed DC link capacitor voltage balancing in a three phase diode clamped inverter controlled by a direct space vector of line to line voltages. Anshuman Shukla et al [3] introduced control schemes for DC capacitor voltages equalization in diode clamped multilevel inverter based DSTATCOM. Monge et al [4] proposed multilevel diode clamped converter for photovoltaic generators with independent voltage control of each solar array. Renge and Suryawanshi [5] developed five level diode clamped inverter to eliminate common mode voltage and reduce dv/dt in medium voltage rating induction motor drives. Hideaki Fujita and Naoya Yamashita [6] discussed performance of a diode clamped linear amplifier. Hatti et al [7] proposed a 6.6-KV transformer less motor drive using a five level diode clamped PWM inverter for energy savings of pumps and blowers. Srinivas in [8] discussed uniform overlapped multi carrier PWM for a six level diode clamped inverter. Engin Ozdemir et al [9] introduced fundamental frequency modulated six level diode clamped multilevel inverter for three phase stand alone photovoltaic system. Berrezzek Farid and Berrezzek Farid [10] made a study on new techniques of controlled PWM inverters. Anshuman shukla et al [11] proposed flying capacitor based chopper circuit for DC capacitor voltage balancing in diode clamped multilevel inverter. This literature survey reveals few papers only on various PWM techniques and hence this work presents a novel approach for controlling the harmonics of output voltage of chosen MLI fed IM employing sinusoidal switching strategies. Simulations are performed using MATLAB-SIMULINK. Harmonics analysis and evaluation of performance measures for various modulation indices have been carried out and presented.

II. MULTILEVEL INVERTER

The general structure of the multilevel inverter is to synthesize a sinusoidal voltage from several levels of voltages typically obtained from capacitor voltage sources. The so-called "multilevel" starts from three levels. A three-level inverter, also known as a "neutral-clamped" inverter, consists of two capacitor voltages in series and uses the center tap as the neutral. Each phase leg of the three-level inverter has two pairs of switching devices in series. The center of each device pair is clamped to the neutral through clamping diodes. The output obtained from a three-level inverter is a quasi-square wave output if fundamental frequency switching is used. Multilevel inverters are being considered for an increasing number of applications due to their high power capability associated with lower output harmonics and lower commutation losses. Multilevel inverters have become an effective and practical solution for increasing power and reducing harmonics of AC load.The main multilevel topologies are classified into three categories: diode clamped inverters, flying capacitor inverters, and cascaded inverters. In a three-phase inverter

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1273-1279 ISSN: 2249-6645

system, the number of main switches of each topology is equal. Comparing with the number of other components, for example, clamping diodes and dc-link capacitors having the same capacity per unit, diode clamped inverters have the least number of capacitors among the three types but require additional clamping diodes. Flying capacitor inverters need the most number of capacitors. But cascaded inverters are considered as having the simplest structure.

The diode clamped inverter, particularly the three-level one, has drawn much interest in motor drive applications because it needs only one common voltage source. Also, simple and efficient PWM algorithms have been developed for it, even if it has inherent unbalanced dc-link capacitor voltage problem. However, it would be a limitation to applications beyond four-level diode clamped inverters for the reason of reliability and complexity considering dc-link balancing and the prohibitively high number of clamping diodes. Multilevel PWM has lower *dv/dt* than that experienced in some two-level PWM drives because switching is between several smaller voltage levels. Diode clamped multilevel inverter is a very general and widely used topology. DCMLI works on the concept of using diodes to limit voltage stress on power devices. A DCMLI typically consists of (m-1) capacitors on the DC bus where m is the total number of positive, negative and zero levels in the output voltage. Figure1 shows a three phase half-bridge five level diode clamped inverter. The order of numbering of the switches for phase a is Sa_1, Sa_2, Sa_3, S_{a4}, Sa_1', Sa_2', Sa_3' and Sa_4' and like wise for other two phases. The DC bus consists of four capacitors C_1, C_2, C_3 and C_4 acting as voltage divider. For a DC bus voltage Vdc, the voltage across each capacitor is Vdc/4 and voltage stress on each device is limited to Vdc/4 through clamping diode. The middle point of the four capacitors 'n' can be defined as the neutral point. The principle of diode clamping to DC-link voltages can be extended to any number of voltage levels. Since the voltages across the semiconductor switches are limited by conduction of the diodes connected to the various DC levels, this class of multilevel inverter is termed diode clamped MLI. Table 1 shows the output voltage levels and the corresponding switch states for one phase of the chosen five level DCMLI. The switches are arranged into 4 pairs (Sa_1, Sa_1'), (Sa_2, Sa_2'), (Sa_3, Sa_3'), (Sa_4, Sa_4'). If one switch of the pair is turned on, the complementary switch of the same pair must be off. Four switches are triggered at any point of time to select the desired level in the five level DCMLI.

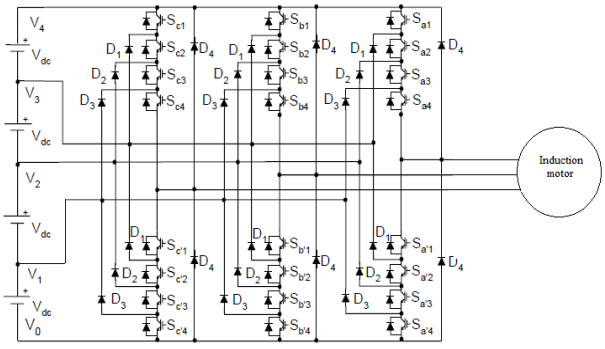

Figure 1 A three phase five level DCMLI

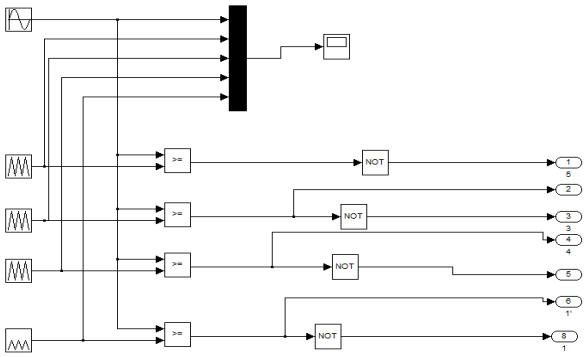

Figure 2 Sample PWM generation logic using SIMULINK developed for PDPWM technique

The steps to synthesis the five level phase a output voltage in this work are as follows:

1. For phase a output voltage of Van=0, two upper switches Sa_3, Sa_4 and two lower switches Sa_1' and Sa_2' are turned on.
2. For an output voltage of Van=Vdc/4, three upper switches Sa_2, Sa_3, Sa_4 and one lower switch Sa_1' are turned on.
3. For an output voltage of Van=Vdc/2, all upper switches Sa_1 through Sa_4 are turned on.
4. To obtain the output voltage of Van= -Vdc/4, upper switch Sa_4 and three lower switches Sa_1', Sa_2' and Sa_3' are turned on.
5. For an output voltage of Van = -Vdc/2, all lower switches Sa_1' through Sa_4' are turned on.

The phase a output voltage Van has five states: Vdc/2, Vdc/4, 0, - Vdc/4 and - Vdc/2. The gate signals for the chosen five level DCMLI are developed using MATLAB-SIMULINK. The gate signal generator model developed is tested for various values of modulation index. The results of the simulation study are presented in this work in the form of the PWM outputs of the chosen multilevel inverter.

TABLE 1 Switching Scheme for one phase of three phase five Level DCMLI

Sa_1	Sa_2	Sa_3	Sa_4	Sa_1'	Sa_2'	Sa_3'	Sa_4'	V_{an}
1	1	1	1	0	0	0	0	$V_{dc}/2$
0	1	1	1	1	0	0	0	$V_{dc}/4$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	- $V_{dc}/4$
0	0	0	0	1	1	1	1	- $V_{dc}/2$

III. MULTI CARRIER BASED PWM METHODS

This work used the intersection of a sine wave with a triangular wave to generate firing pulses. There are many alternative strategies to implement this. They are as given below.

1) Phase disposition PWM strategy.
2) Phase opposition disposition PWM strategy.
3) Alternate phase opposition disposition PWM strategy.
4) Carrier overlapping PWM strategy.

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1273-1279 ISSN: 2249-6645

5) Variable frequency PWM strategy.
6) Phase shift PWM strategy.

III.1. Phase Disposition PWM Strategy

The rules for phase disposition method Fig.3 for a multilevel inverter are

1) 4 carrier waveforms in phase are arranged.
2) The converter is switched to + Vdc/2 when the sine wave is greater than both upper carrier.
3) The converter is switched to + Vdc/4 when the sine wave is greater than first upper carrier.
4) The converter is switched to zero when sine wave is lower than upper carrier but higher than the lower carrier.
5) The converter is switched to – Vdc/4 when the sine wave is less than first lower carrier.
6) The converter is switched to - Vdc/2 when the sine wave is less than both lower carrier.

The following formula is applicable to sub harmonic PWM strategy i.e. PD, POD and APOD

The frequency modulation index

$$m_f = f_c/f_m$$

The Amplitude modulation index

$$m_a = 2A_m/ (m-1) A_c$$

where

f_c – Frequency of the carrier signal
f_m – Frequency of the reference signal
A_m –Amplitude of the reference signal
A_c – Amplitude of the carrier signal
m – number of levels.

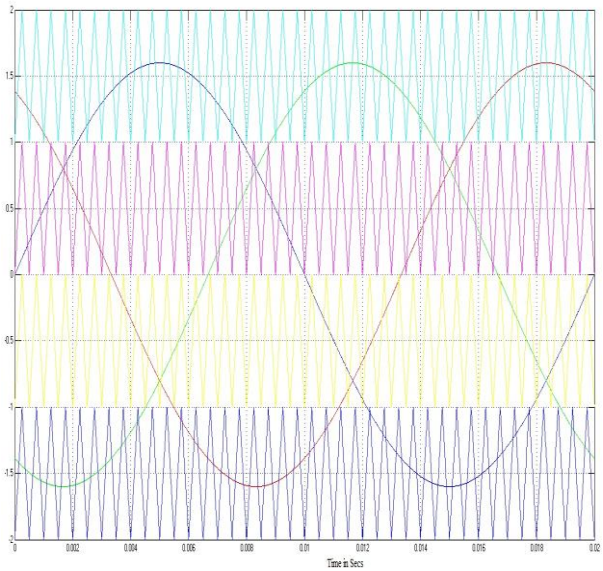

Figure 3 Carrier arrangement for PDPWM strategy (m_a=0.8 and m_f=40)

III.2. Phase Opposition Disposition Strategy

Four carrier waveforms are arranged so that all carrier waveforms above zero are in phase and they are 180 degrees out of phase with those below zero (Fig.4)

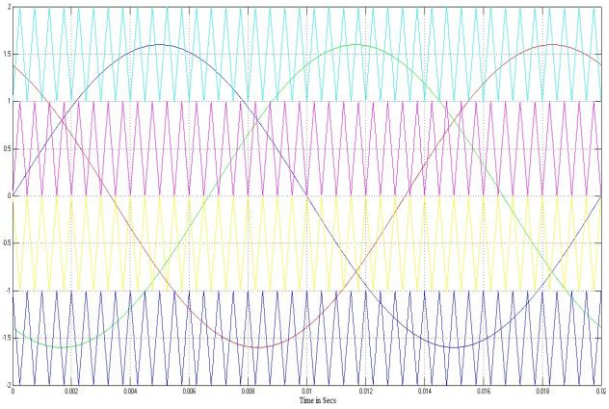

Figure 4 Carrier arrangement for PODPWM strategy (m_a=0.8 and m_f=40)

III.3. Alternative Phase Opposition and Disposition Strategy

Carriers are arranged in such a manner that each carrier is out of phase with its neighbor by 180 degrees (Fig.5).

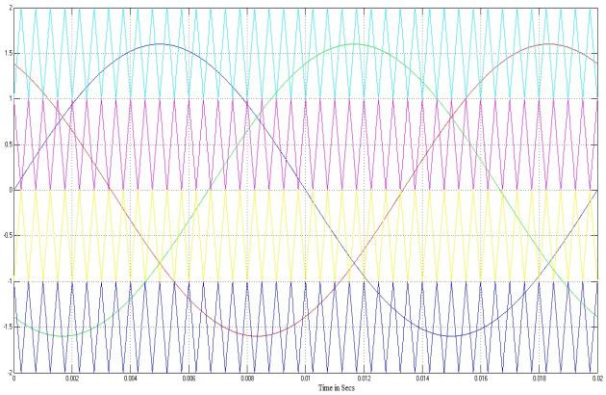

Figure 5 Carrier arrangement for APODPWM strategy (m_a=0.8 and m_f=40)

III.4. Phase Shift PWM (PSPWM) Strategy

The phase shift multicarrier PWM technique (Fig.6) uses four carrier signals of the same amplitude and frequency which are shifted by 90 degrees to one another to generate the five level inverter output voltages. The gate signals for the chosen inverter can be derived directly from the PWM signals (comparison of the carrier with the sinusoidal reference).

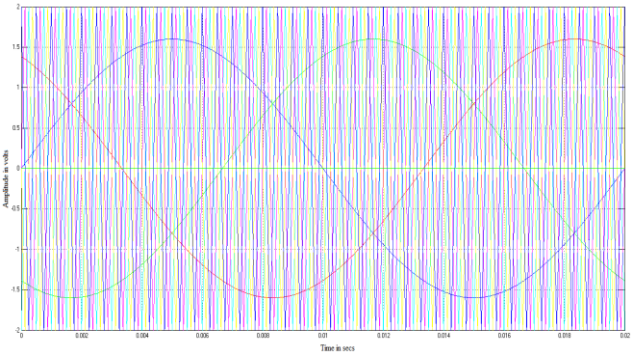

Figure 6 Carrier arrangement for PSPWM strategy (m_a=0.8 and m_f=40)

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1273-1279 ISSN: 2249-6645

III.5. Carrier Overlapping PWM (COPWM) Strategy

For an m-level inverter using carrier overlapping technique, m-1 carriers with the same frequency f_c and same peak-to-peak amplitude Ac are disposed such that the bands they occupy overlap each other; the overlapping vertical distance between each carrier is Ac/2. The reference waveform has amplitude of A_m and frequency of fm and it is centred in the middle of the carrier signals. The reference wave is continuously compared with each of the carrier signals. If the reference wave is more than a carrier signal, then the active devices corresponding to that carrier are switched on. Otherwise, the devices switch off. The amplitude modulation index m_a and the frequency ratio m_f are defined in the carrier overlapping method (Fig.7) as follows:

$$m_a = A_m / (m / 4)* A_c$$
$$m_f = f_c / f_m$$

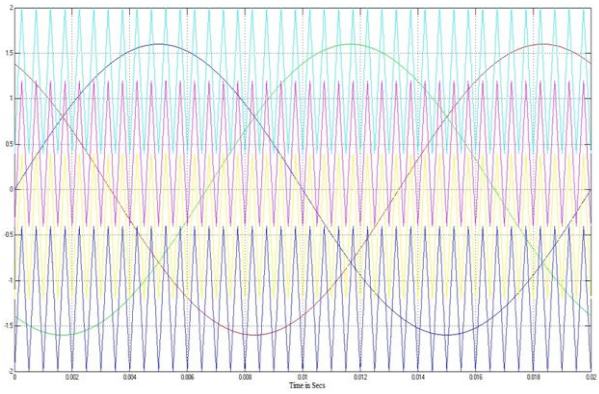

Figure 7 Carrier arrangement for COPWM strategy (m_a=0.8 and m_f=40)

III.6. Variable Frequency PWM (VFPWM) Strategy

The number of switchings for upper and lower devices of chosen MLI is much more than that of intermediate switches in SHPWM using constant frequency carriers. In order to equalize the number of switchings for all the switches, variable frequency PWM strategy is used as illustrated in which the carrier frequency of the intermediate switches is properly increased to balance the numbers of switching for all the switches (Fig.8).

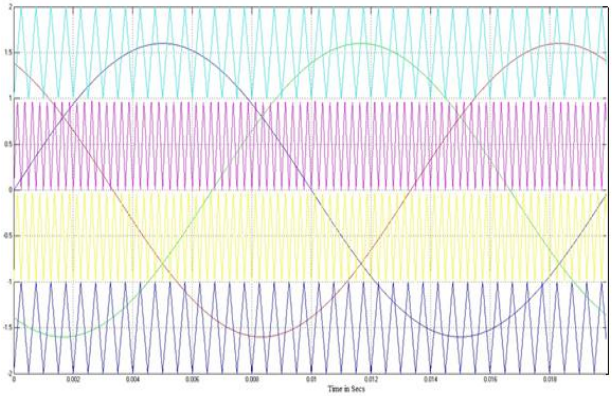

Figure 8 Carrier arrangement for VFPWM strategy (m_a=0.8 and m_f=40)

IV. Simulation Results

The three phase diode clamped five level inverter is modeled in SIMULINK using power system block set. Simulations are performed for different values of m_a ranging from 0.6 to 1 and the corresponding %THD are measured using the FFT block and their values are shown in Table 2. Figs.9 – 23 show the simulated output voltage of DCMLI fed IM and their harmonic spectrum, speed and torque characteristics of Induction Motor (IM) with above strategies but for only one sample value of m_a = 0.8. Fig. 10 shows the five level output voltage generated by PDPWM strategy and its FFT plot is shown in Fig. 11. From Fig. 11, it is observed that the PDPWM strategy produces significant 30th, 32nd, 36th and 38th harmonic energy. Fig 13 shows the five level output voltage generated by PODPWM strategy and its FFT plot is shown in Fig. 14. From Fig. 14 it is observed that the PODPWM strategy produces significant 33rd and 35th harmonic energy. Fig 16 shows the five level output voltage generated by APODPWM strategy and its FFT plot is shown in Fig. 17. From Fig. 17 it is observed that the APODPWM strategy produces significant 33rd, 35th and 37th harmonic energy. Fig 19 shows the five level output voltage generated by COPWM strategy and its FFT plot is shown in Fig. 20. From Fig. 20 it is observed that the COPWM strategy produces significant 38th harmonic energy. Fig 22 shows the five level output voltage generated by VFPWM strategy and its FFT plot is shown in Fig. 23. From Fig. 23 it is observed that the VFPWM strategy produces significant 34th and 38th harmonic energy. The following parameter values are used for simulation : V_{dc} = 440V , induction motor load – 50HP(37 KW), 400V, 50Hz, 1480rpm, T_m = 4Nm, f_c = 2000Hz, f_m = 50Hz. Figs. 9, 12, 15, 18, 21 show speed torque characteristics of IM fed by chosen MLI for PD, POD, APOD, CO, VF PWM strategies.

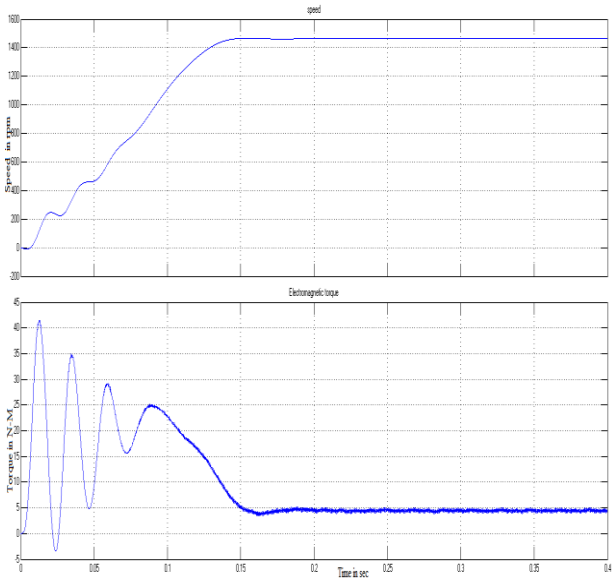

Figure 9 Speed and torque characteristics of IM for PDPWM strategy

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1273-1279 ISSN: 2249-6645

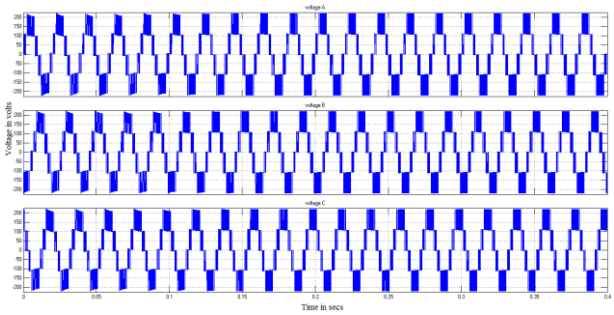

Figure 10 Output voltage generated by PDPWM strategy for IM load

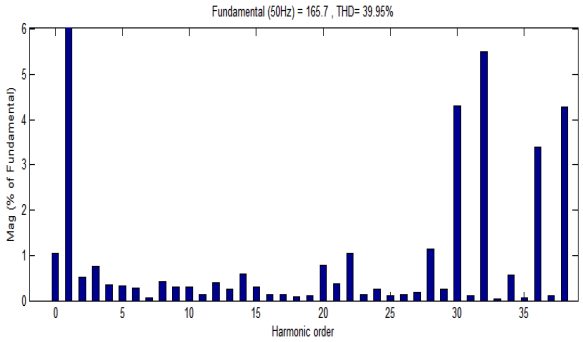

Figure 11 FFT plot for output voltage of PDPWM strategy for IM load

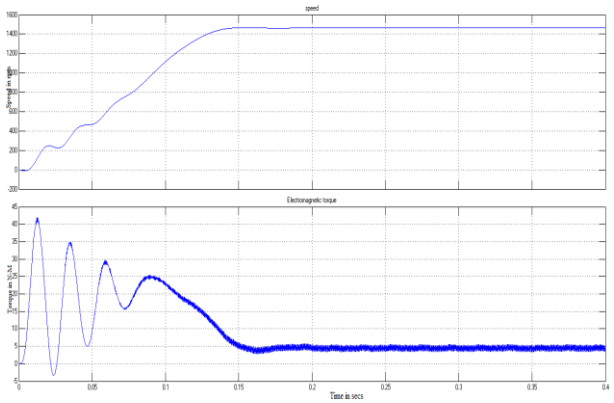

Figure 12 Speed and torque characteristics of IM for PODPWM strategy

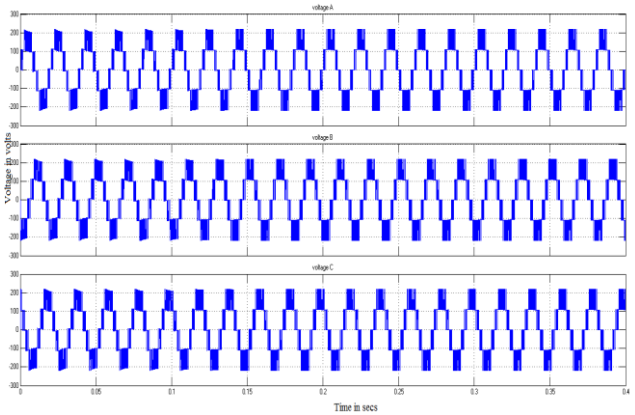

Figure 13 Output voltage generated by PODPWM strategy for IM load

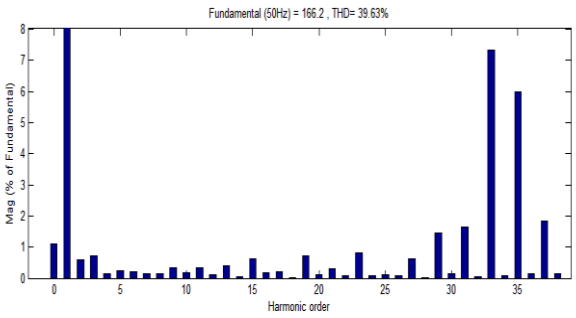

Figure 14 FFT plot for output voltage of PODPWM strategy for IM load

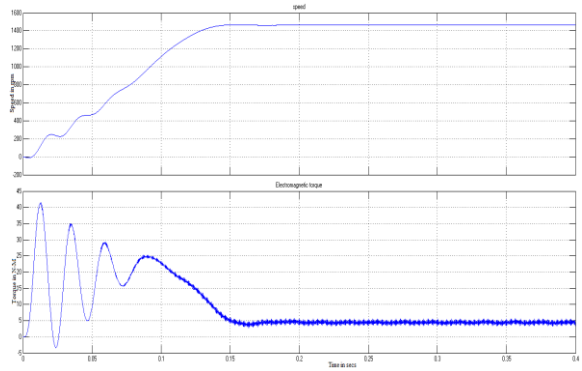

Figure 15 Speed and torque characteristics of IM for APODPWM strategy

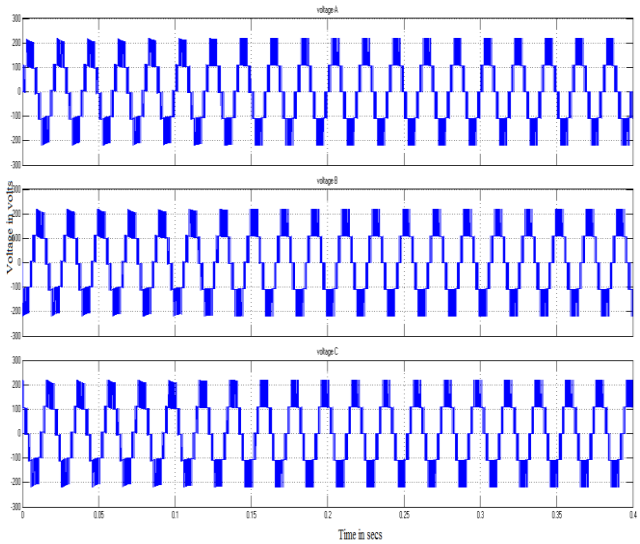

Figure 16 Output voltage generated by APODPWM strategy for IM load

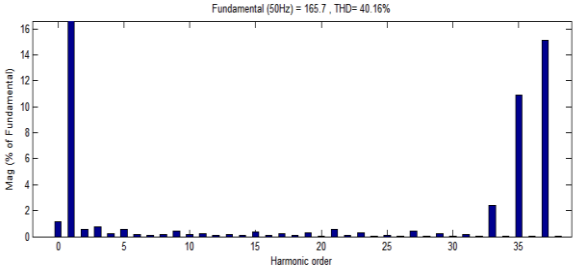

Figure 17 FFT plot for output voltage of APODPWM strategy for IM load

www.ijmer.com Vol.2, Issue.3, May-June 2012 pp-1273-1279 ISSN: 2249-6645

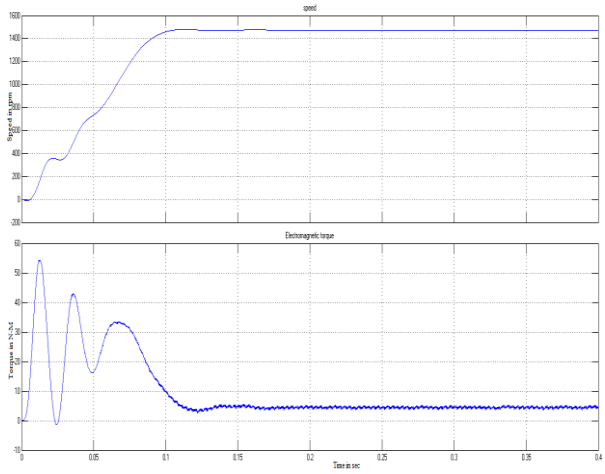

Figure 18 Speed and torque characteristics of IM for COPWM strategy

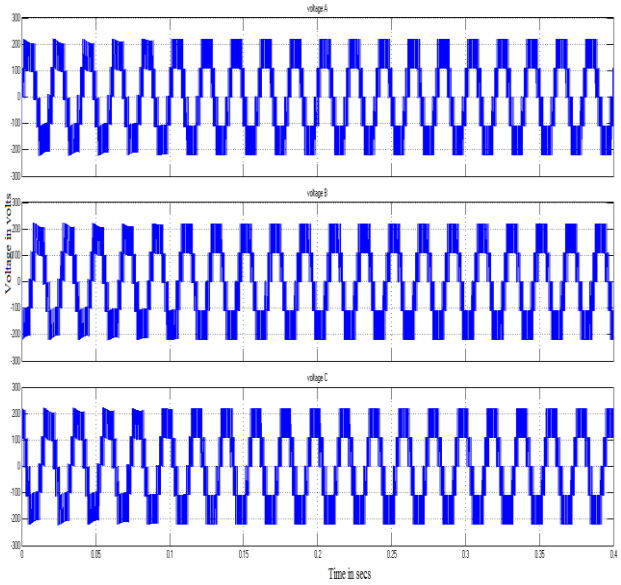

Figure 19 Output voltage generated by COPWM strategy for IM load

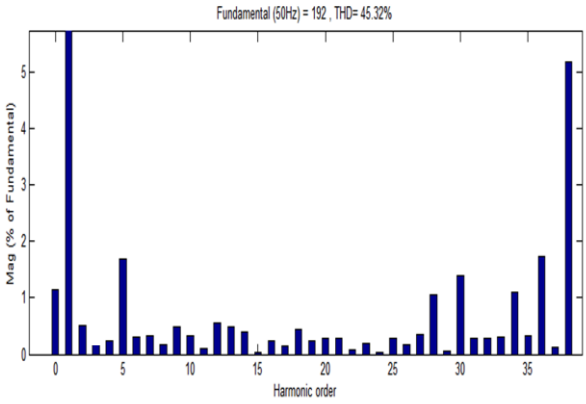

Figure 20 FFT plot for output voltage of COPWM strategy for IM load

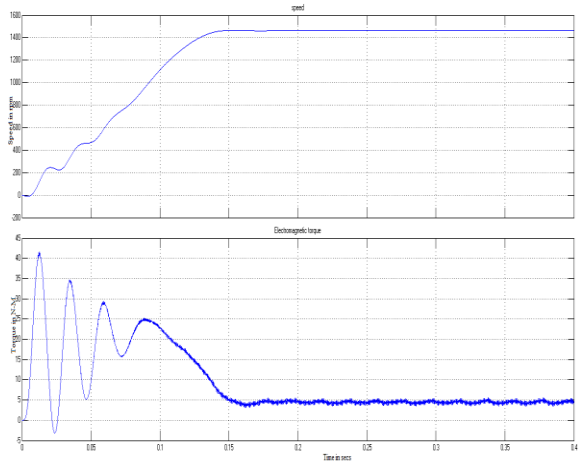

Figure 21 Speed and torque characteristics of IM for VFPWM strategy

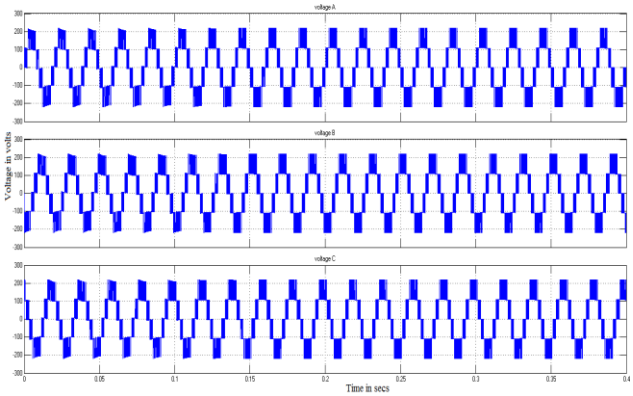

Figure 22 Output voltage generated by VFPWM strategy for IM load

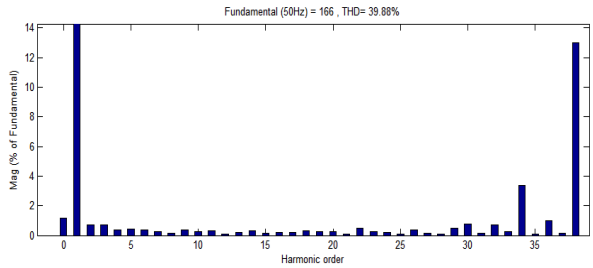

Figure 23 FFT plot for output voltage of VFPWM strategy for IM load

TABLE 2 % THD comparison for different modulation indices for IM load

m_a	PD	POD	APOD	CO	VF
1	27.99	27.78	28.43	34.72	28.05
0.9	34.9	34.89	35.32	34.72	34.89
0.8	39.95	39.63	40.16	45.32	39.88
0.7	43.67	43.53	43.77	52.09	44.14
0.6	46.22	46.48	46.26	60.68	46.33

TABLE 3 V_{RMS} (fundamental) for different modulation indices for IM load

m_a	PD	POD	APOD	CO	VF
1	146.1	146.3	146.2	156.5	146.1
0.9	131.8	131.5	131.6	146.5	131.6
0.8	117.2	117.5	117.2	135.8	117.3
0.7	102.6	102.5	102.7	123.4	102.4
0.6	88.08	87.68	88.06	110.6	88.3

TABLE 4 Form factor for different modulation indices for IM load

m_a	PD	POD	APOD	CO	VF
1	120.74	125.04	121.83	126.20	137.83
0.9	104.60	112.39	110.58	135.64	112.47
0.8	111.61	107.79	104.6	119.12	102.89
0.7	77.14	101.48	96.88	113.2	83.93
0.6	74.01	81.19	84.67	97.87	80.27

TABLE 5 Crest factor for different modulation indices for IM load

m_a	PD	POD	APOD	CO	VF
1	1.414	1.4156	1.414	1.4144	1.4142
0.9	1.4139	1.4143	1.4145	1.414	1.4142
0.8	1.414	1.414	1.4142	1.414	1.4143
0.7	1.414	1.4137	1.414	1.414	1.4140
0.6	1.4141	1.4146	1.4144	1.4139	1.4140

TABLE 6 Distortion factor for different modulation indices for IM load

m_a	PD	POD	APOD	CO	VF
1	0.1494	0.1306	0.1444	0.856	0.0955
0.9	0.1588	0.1543	0.1597	0.7711	0.1407
0.8	0.1611	0.1694	0.1682	0.5953	0.2
0.7	0.1811	0.16	0.1533	0.2876	0.1759
0.6	0.1796	0.226	0.1949	0.1485	0.1841

V. CONCLUSION

In this work the simulation results of three phase five level diode clamped multilevel inverter fed Induction Motor load with various modulating strategies are obtained through MATLAB/SIMULINK. The output quantities like phase voltage, THD spectrum for phase voltage, and torque-speed characteristics of induction motor are obtained. It is observed from Table 2 that PODPWM method provides output with relatively low distortion. COPWM is found to perform better since it provides relatively higher fundamental RMS output voltage. Table 3, 4 and 5 show the crest factor, form factor and distortion factor.

REFERENCES

[1] Xiaoming Yuan and Ivo Barbi "Fundamentals of a New Diode Clamping Multilevel Inverter**",** *IEEE Trans. on Power Electronics, Vol.15, No.4,* 2000, pp.711-718.

[2] O. Bouhali, B. Francois, E. M. Berkouk, and C. Saudemont, **"**DC Link Capacitor Voltage Balancing in a Three-Phase Diode Clamped Inverter Controlled by a Direct Space Vector of Line-to-Line Voltages**",** *IEEE Trans. on Power Electronics, Vol.22, No.5,* 2007, pp.1636-1648.

[3] Anshuman Shukla, Arindam Ghosh and Avinash Joshi, **"**Control Schemes for DC Capacitor Voltages Equalization in Diode-Clamped Multilevel Inverter Based DSTATCOM**",** *IEEE Trans. on Power Delivery, Vol.23, No.2,* 2008, pp.1139-1149.

[4] Sergio Busquets Monge, Joan Rocabert Pedro Rodriguez, Salvador Alepuz and Josep Bordonau, **"**Multilevel Diode Clamped Converter for Photovoltaic Generators With Independent Voltage Control of Each Solar Array"**,** *IEEE Trans. on Industrial Electronics, Vol.55, No.7,* 2008, pp.2713-2723.

[5] Mohan M. Renge and Hiralal M. Suryawanshi**,** **"**Five-Level Diode Clamped Inverter to Eliminate Common Mode Voltage and Reduce dv/dt in Medium Voltage Rating Induction Motor Drives**",** *IEEE Trans. on Power Electronics, Vol.23, No.4,* 2008, pp.1598-1607.

[6] Hideaki Fujita, and Naoya Yamashita, **"**Performance of a Diode-Clamped Linear Amplifier**",** *IEEE Trans. on Power Electronics, Vol.23, No.2,* 2008, pp.824-831.

[7] Natchpong Hatti, Kazunori Hasegawa and Hirofumi Akagi**,** **"**A 6.6-KV Transformer less Motor Drive Using a Five-Level Diode-Clamped PWM Inverter For Energy Savings of Pumps and Blowers"**,** *IEEE Trans. on Power Electronics, Vol.24, No.3,* 2009, pp.796-803.

[8] S.Srinivas, **"**Uniform Overlapped Multi-Carrier PWM for a Six-Level Diode Clamped Inverter**",** *International Journal of Electrical and Electronics Engineering* , 2009, pp.763-768.

[9] Engin Ozdemir, Sule Ozdemir and Leon M. Tolbert, **"**Fundamental-Frequency-Modulated Six-Level Diode-Clamped Multilevel Inverter for Three-Phase Stand-Alone Photovoltaic System**",** *IEEE Trans. on Power Electronics, Vol.56, No.11,* 2009, pp.4407-4415.

[10] Berrezzek Farid and Berrezzek Farid, **"**A Study of New Techniques of Controlled PWM Inverters**",** *European Journal of Scientific Research, ISSN 1450-216X, Vol.32, No.1*, 2009, pp.77-87.

[11] Anshuman shukla, Arindam Ghosh and Avinash Joshi, "Flying-Capacitor-Based Chopper Circuit for DC Capacitor Voltage Balancing in Diode-Clamped Multileverl Inverter", *IEEE Trans. on Industrial Electronics, Vol.57*, 2010, pp 2249-2261.